A PVT-tolerant Dual-loop Injection-locked PLL for Clock Generation

東京工業大学 理工学研究科， ○ウェイ デン，ムサ アハマド，シリブラーノン ティーラショート，宮原正也，岡田健一，松澤昭
Tokyo Institute of Technology, ○Wei Deng, Ahmed Musa, Teerachot Siriburanon, Masaya Miyahara, Kenichi Okada, and Akira Matsuzawa
deng@ssc.pe.titech.ac.jp

This paper proposes a dual-loop injection-locked PLL with synthesizable all-digital PVT calibration system for SoC clock generation[1]. This circuit is implemented in a standard 65nm CMOS technology. The die micrograph is shown in Fig.1. The measured phase noise maps to a 0.7 ps jitter when integrated from 10 kHz to 40 MHz. The proposed dual-loop IL-PLL has an operating range of 0.5-to-1.6 GHz, and it consumes a total power consumption of 0.97 mW excluding output buffer, from a 1 V power supply. The measured reference spur is -57 dBc. The reference clock can be varied from 40 to 300 MHz. All the above-mentioned measurements are performed at the room temperature.

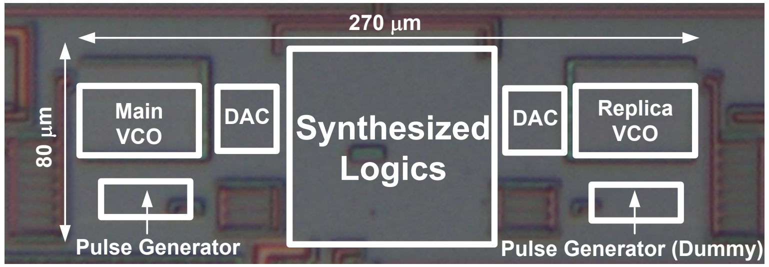

Fig. 1. Chip microphotograph.

[1] Wei Deng, Ahmed Musa, Teerachot Siriburanon, Masaya Miyahara, Kenichi Okada, and Akira Matsuzawa, "A 0.022 mm^2 970 μW Dual-Loop Injection-Locked PLL with -243 dB FOM Using Synthesizable All-Digital PVT Calibration Circuits," *IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers,* pp.248-249, 2013.