A 12-bit Interpolated Pipeline ADC using Body Voltage Controlled Amplifier

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***Abstract*—This paper presents a 12-bit interpolated pipeline analog to digital converter (ADC) using body voltage controlled amplifier for current biasing and common mode feedback loop (CMFB). The proposed body voltage control method allows the amplifier to achieve small power consumption and large output swing. The proposed amplifier has a power consumption lower than 15.6 mW, almost half of the folded cascode (FC) amplifier satisfying 12-bit, 400 MS/s ADC operation. Moreover, the proposed amplifier secures 600 mV output swing, which is 1-V_{DS} wider compared with the telescopic amplifier. The 12-bit interpolated pipeline ADC using proposed amplifier is demonstrated by 1P9M 90 nm process with 1.2 V supply voltage. The ADC achieves ENOB of about 10-bit at 300 MS/s and an FoM of 0.2 pJ/conv. when the frequency of the input signal is sufficiently low.**

I. INTRODUCTION

Advancements on high data-rate and high performance telecommunication systems are significant reasons of the leading parts in the recent system-on-chip area. To increase the data-rate of the telecommunication system, high resolution and high speed ADC is mandatory. However, recent scaled CMOS technology makes analog circuit design difficult because of low intrinsic gain and narrow signal swing. Among those problems, the low intrinsic gain is more serious for the pipeline ADC because it utilizes operational amplifiers in need of high gain. Recently published pipeline ADCs address this problem by using digital calibration techniques [1-5]. However, it often increases the test cost and the difficulty for the guarantee of the product quality. Lately, pipeline ADCs using interpolation technique are introduced [6-7], which can achieve high resolution (> 10-bit) and high speed (> 300 MS/s) with relatively low gain amplifiers. For example, the work in [6] realizes 10-bit, 320 MS/s ADC with only 9.5-dB gain amplifier. Another ADC in [7] achieves 12-bit, 800 MS/s with 40-dB gain pseudo differential amplifier with 4-times interleaving. The use of an open-loop amplifier in [6] looks attractive due to its simplicity. Nevertheless, even though the interpolation technique relaxes the requirement of the amplifier's gain, the linearity is still crucial for the ADC's performance. Especially higher 12-bit resolution, an open-loop amplifier consumes too much power to satisfy the linearity requirement. For this case, a relatively high gain op-amp with feedback loop is one of the good candidates for the amplifier's topology such as in [7]. In this paper, 12-bit interpolated pipeline ADC which is based on [6] is introduced. An amplifier with body voltage control technique is proposed to realize high gain (> 45-dB) with small power consumption and large signal swing. The proposed amplifier with closed-loop shows sufficiently high performance for the 12-bit resolution and 400 MS/s operation.

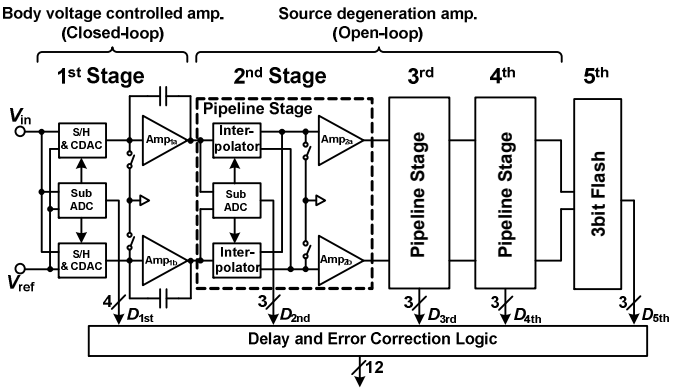

Figure 1. Block diagram of proposed ADC.

II. 12-BIT INTERPOLATED PIPELINE ADC STRUCTURE

A 12-bit ADC utilizing interpolation technique to relax the gain requirement of the amplifier and with using the body voltage controlled amplifier is proposed and implemented. Fig. 1 shows a block diagram of the proposed ADC, in which it can be observed that the ADC consists of 5-stages. The 1st stage converts 4-bit and other four stages convert 3-bit. The ADC employs 1-bit redundancy in 1st to 4th stages to reduce the effect of the comparator's offset voltage. The ADC in [6] utilizes only open-loop amplifiers with source degeneration. However, as explained in Section I, the power consumption of the amplifier increases so much by using open-loop topology. In the proposed 12-bit ADC, the 1st stage uses the proposed amplifier with 45-dB gain and feedback loop. The amplifier is explained in Section III. The single stage open-loop amplifiers are used for the 2nd to 4th stages, since the linearity requirement is not so much severe. The feedback loop gain of the 1st stage is 12-dB and the open-loop gain of the other stages is 9.5-dB. There is no calibration circuit for linearity or gain mismatch in the stages; which are properties

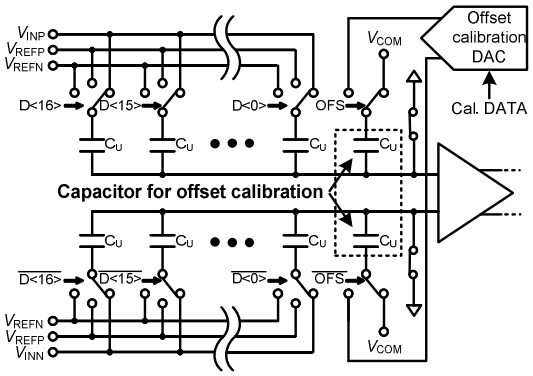

Figure 2. Structure of CDAC with amplifier's offset cancellation in 1st stage.

of the interpolation technique. Offset voltage of the open-loop amplifiers, which have small gain in the 2nd to 4th stages can be cancelled by using capacitors in the following stage. However, the amplifier with capacitive closed-loop topology in the 1st stage cannot use the same approach. Therefore, the other technique has to be applied for the 1st stage amplifier. Fig. 2 illustrates the proposed amplifier's offset calibration method. As mentioned before in this section, the proposed ADC utilizes 1-bit redundancy structure in 1st to 4th stages. Because ADC utilizes capacitive digital to analog converter (CDAC) for the reference selection in the 1st stage, the redundancy can be realized by the extra capacitor in the CDAC as shown in Fig. 2. If there is no offset in the amplifier, the capacitor charges and discharges via V_{COM} and reference voltages, i.e. V_{REFP} or V_{REFN}, accordingly. The ADC controls reference voltage for the amplifier's offset calibration. During the offset calibrating phase, the ADC input is connected to V_{COM}. If there is no offset, the ADC's output becomes the middle value. On the other hand, if the amplifier has an offset, the output goes high or low from the middle value. The ADC verifies this value and adjusts the reference voltage to calibrate the amplifier's offset. This function can be realized by simple comparison of the ADC's output with middle value and an extra DAC for the calibrated reference voltage generation.

III. Body Voltage Controlled Amplifier

A. Amplifier Topology

A body voltage controlled amplifier for the 1st stage is used for this work, as noted before. Fig. 3 demonstrates the topology of the proposed amplifier. The amplifier incorporates cascode topology to increase the gain. Furthermore, the amplifier has a CMOS input to increase the transconductance for the settling requirement. There are two additional MOS transistors (M_{NB1} and M_{NB2}) in the proposed amplifier, used for current biasing. There are two-feedback loop in the amplifier. One is for the CMFB and the other is for the current biasing. This might cause unstable operating point for the amplifier if the feedback loop values are chosen to be incorrect. In order to prevent this issue, a large capacitance (C_{FB}) is inserted in the CMFB feedback loop for the stabilizing. There is only one differential current path in the proposed amplifier. In addition, the amplifier stacks only four MOS transistors, which means that the proposed amplifier has the advantages of the telescopic amplifier topology in the small power consumption and the FC amplifier topology in the large output signal swing. These characteristics are accomplished by body voltage control which is detailed in the following sub-sections.

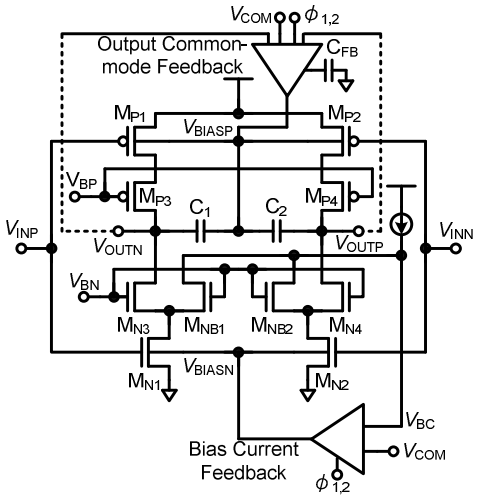

Figure 3. Schematic of body voltage controlled amplifier.

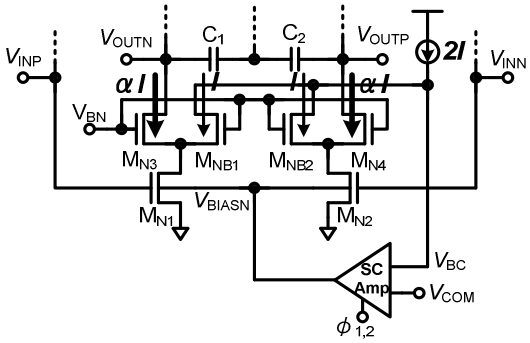

Figure 4. Current biasing method of proposed amplifier.

B. Body Voltage Controlled Current Biasing

To achieve small power consumption with high gain, the telescopic topology is a good choice. The telescopic amplifier employs MOS transistor as a current source for the current biasing. On the contrary, telescopic amplifier decreases the amplifier's output swing which results in decrease of SNR. In order to prevent the SNR degradation, the proposed amplifier removes current source. Instead of current source, the current mirroring in NMOS cascode transistor by body voltage control technique is applied. Because the current of the MOS transistor is a function of g_m and g_{mb}, the current can also be adjusted by body voltage control. The g_{mb} can be defined as below;

$$g_{mb} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})\left(-\frac{\partial V_{TH}}{\partial V_{BS}}\right). \quad (1)$$

Fig. 4 shows the detailed current biasing method in the proposed amplifier. In Fig. 4, the current of 2*I* flows from the current bias circuit to the amplifier. These current's paths are connected to the bias NMOS transistors (M_{NB1} and M_{NB2}). These two transistors and NMOS cascode transistors (M_{N3} and M_{N4}) of the amplifier have the same gate-source voltages which result in current mirroring from NMOS bias transistors to NMOS cascode transistors. The current of the amplifier can be defined as below,

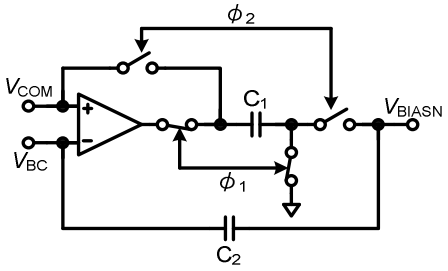

Figure 5. Feedback loop for current bias.

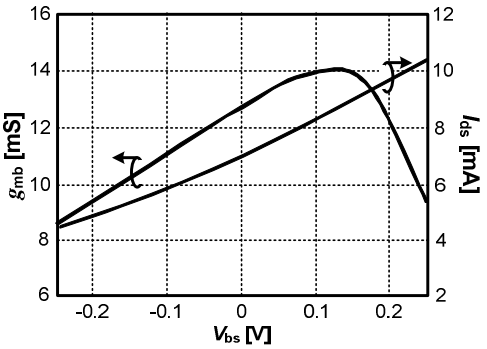

Figure 6. Simulation results of g_{mb}, I_{ds} vs. V_{bs}.

$$W_{NB1,2} : W_{N3,4} = I : \alpha I \quad (2)$$

where W means MOS transistor's size and α means the size ratio of $M_{NB1,2}$ to $M_{N3,4}$. Equation (2) means that the current can be controlled by the size. Nonetheless, if the drain voltages of the input NMOS transistors (M_{N1} and M_{N2}) vary, the current changes also. To keep the current in constant, a feedback loop is organized from current bias circuit to the body of the input NMOS transistors. When there is a current changing in the bias NMOS transistor, the feedback loop senses its variation and adjusts the body voltage of the input NMOS transistors. Fig. 5 depicts the structure of the current bias feedback loop that works as a switched capacitor circuit. In the feedback loop, C_2 charges current from the bias circuit. During ϕ_1, C_1 charges the difference between V_{BC} and V_{COM} by the amplifier. During ϕ_2, the charged difference is applied to the body voltage. The amplifier in the feedback loop utilizes single stage amplifier because the feedback loop does not require high gain amplifier. It is necessary to figure out the current control ability of the body voltage control. Fig. 6 presents the simulation results of g_{mb}, I_{ds} vs. V_{bs}. The range of V_{bs} is determined by the actual control range of the feedback loop. The current variation range is 10.5 / 4.5 mA with 7 mA default current, which is wide enough for the current adjustment.

C. Body Voltage Controlled CMFB

The proposed amplifier utilizes body voltage control of the PMOS input transistors for CMFB. The structure of the feedback loop for CMFB is depicted in Fig. 7. V_{OUTP} and V_{OUTN} of the feedback loop are connected to the amplifier's output as shown in Fig. 3. The C_1 and C_2 charge the output voltages of the amplifier. After that, the feedback loop averages the output voltages and senses the difference from V_{COM}. Finally, the output of the feedback amplifier is applied to the body of the PMOS input transistors in the amplifier. By this operation, the amplifier realizes the CMFB function without current source transistor.

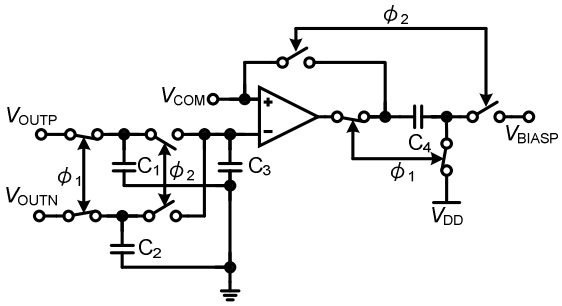

Figure 7. Feedback loop for CMFB.

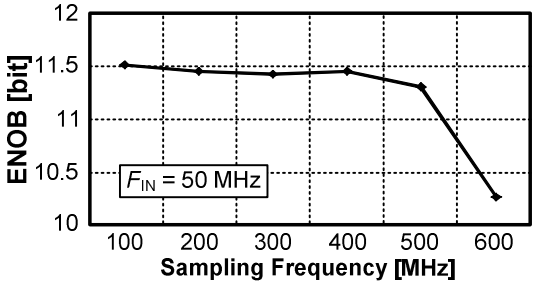

Figure 8. Simulation result of ENOB vs. sampling frequency.

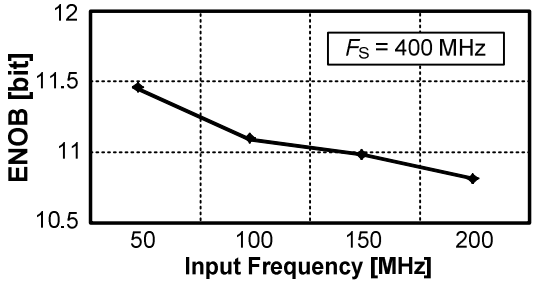

Figure 9. Simulation result of ENOB vs. input frequency.

IV. Simulation and Experimental Results

The proposed ADC was designed in 1P9M 90 nm CMOS technology. The ADC operates in 1.2 V supply voltage. The simulation result of the ENOB vs. sampling frequency at 50 MHz input signal is provided in Fig. 8. The ENOB keeps above 11.4-bit until 400 MHz sampling frequency. Above 500 MHz, the performance of the ADC degraded. At that point, the ENOB is 11.3-bit. Fig. 9 provides simulation result of the ENOB vs. the input signal frequency at the sampling frequency of 400 MHz. The ENOB degrades from 11.5-bit where the input frequency is 50 MHz, with increasing input signal frequency. When the input frequency becomes Nyquist frequency, the ENOB degrades to 10.8-bit. Fig. 10 shows DNL / INL measurement results at 300 MS/s and 100 kHz input. The DNL / INL results are +1.4 / -1 and +3.1 / -4.5, respectively. Measured output spectrum at 300 MHz sampling frequency and 100 kHz input frequency are given in Fig. 11. At the mentioned setting, the ENOB becomes 10-bit. The performance degradation of the measurement results is due to the parasitic components (capacitance, inductance, and resistance) in the package and the test board. These parasitics cause reference voltage ringing and input signal distortion. It is expected that the measurement results will be improved if the ADC input driver and the reference driver is inserted in the package. Table I points out the simulation performance characteristics of the proposed body voltage controlled amplifier. The power consumption and the settling time are

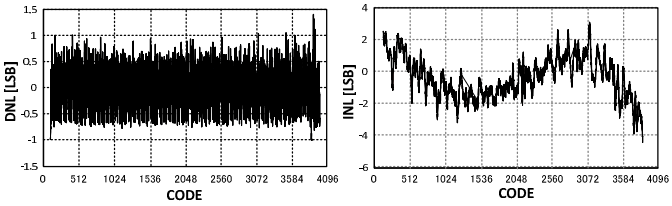

Figure 10. DNL / INL measurement results at 300 MS/s and 100 kHz input.

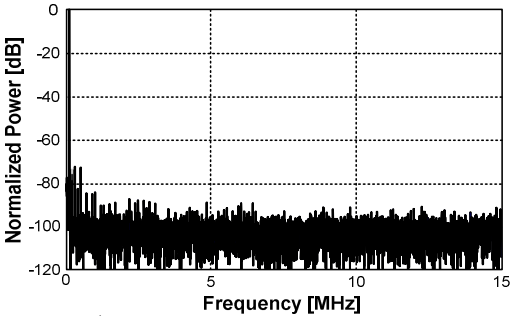

Figure 11. Measured output spectrum at 300 MS/s and 100 kHz input.

determined to achieve 12-bit 400 MS/s interpolated pipeline ADC. The proposed amplifier achieves 40% reduction of the power consumption in comparison with FC amplifier. Furthermore, in comparison with telescopic amplifier the output signal swing is increased by 12.5%. Considering the output signal swing for telescopic amplifier, the power consumption would increase to acquire the same SNR with the proposed amplifier. The power consumption can be reduced by a factor of 58% by using the proposed amplifier. The results indicate that the proposed amplifier is a good candidate for the ADC's target specification even though it utilizes the body voltage control. The performance comparison data between several ADCs with the proposed ADC are given in Table II. The values in this table are all measurement data. It can be observed that [8] and [9] achieved very high speed conversion frequency. However, the power consumptions are very high. The work in [7] shows a good balance in the sampling frequency and the power consumption. Considering the figure of merit (FoM), the proposed ADC can compete with other ADCs at the low input frequency range. Therefore, when the problems related with the parasitic components are solved, desired higher input signal frequency can be achieved and it can demonstrate reasonable performance to be used.

V. CONCLUSION

In this paper, a 12-bit interpolated pipeline ADC with body voltage controlled amplifier is demonstrated. Even though the interpolation technique relaxes the DC gain requirement of the amplifier, a relatively high gain amplifier with feedback loop is required to obtain higher linearity. The proposed body voltage controlled amplifier achieves the required gain with small power consumption and large output swing. The amplifier's current biasing and CMFB are realized with body voltage control. The 12-bit interpolated pipeline ADC using proposed amplifier shows a good performance in the simulation, such as the ENOB of 10.8-bit at 400 MS/s and Nyquist input frequency. The measured ADC's performance is degraded due to the parasitic components in the package and the test board. Thus, by solving the parasitic problems, the proposed ADC can become an attractive candidate for the high performance communication systems.

TABLE I. AMPLIFIER PERFORMANCE CHARACTERISTICS

Topology	Body voltage control
DC Gain [dB]	45
Power Consumption [mW]	15.6 (↓ 40 % from FC amp)
Settling Time [ps]	500
Output Swing Range [mV_{pp}]	600 (↑ 12.5 % from Telescopic amp)

TABLE II. RECENTLY PUBLISHED 12-BIT ADCS

	This work	[7]	[8]	[9]
Resolution [bit]	12	12	12	12
F_{sample} [MS/s]	300	800	1000	3000
V_{DD} [V]	1.2	1 / 2.5	1.8 / 3.3	1 / 2.5
Power [mW]	60	105	550	500
$ENOB_{peak}$ [bit]	9.96 (100 kHz)	9.5	9.5 (by SNR)	9.5
FoM [pJ/conv.]	0.2	0.18	0.76	0.23
Technology [nm]	90	40	180 (SiGe)	40
Core Area [mm^2]	0.48	0.88	2.35	0.4
Linearity Compensation	No	Yes	Yes	Yes
Interleave	No	4-times	No	2-times

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