A 12-bit Interpolated Pipeline ADC using Body Voltage Controlled Amplifier

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Outline

- Background
- Body voltage controlled amplifier
- 12-bit, 300 MS/s interpolated pipeline ADC
- Simulation and measurement results
- Conclusion

- **Background**
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- **12-bit, 300 MS/s interpolated pipeline ADC**
- **Simulation and measurement results**
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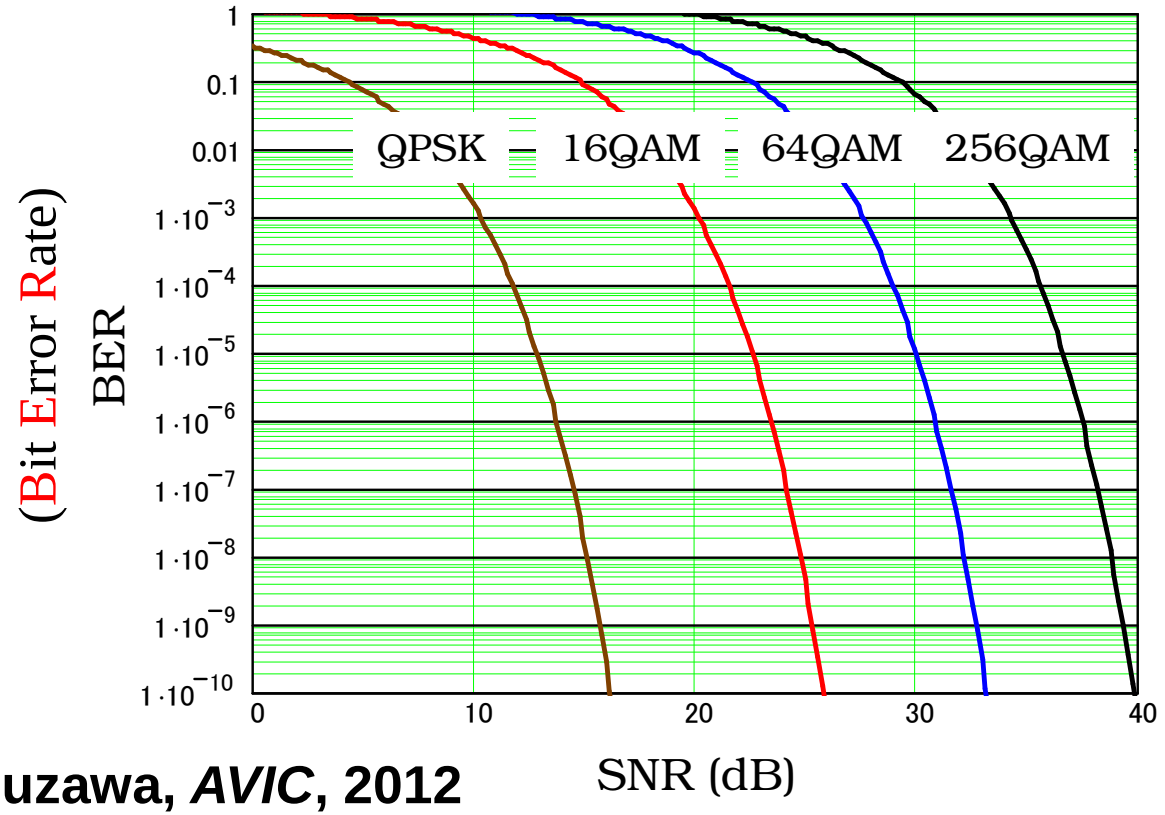
Background

- **To realize high order modulation, high performance ADC is required**

$$D_{\text{rate}} \approx N \cdot F_{\text{s}}$$

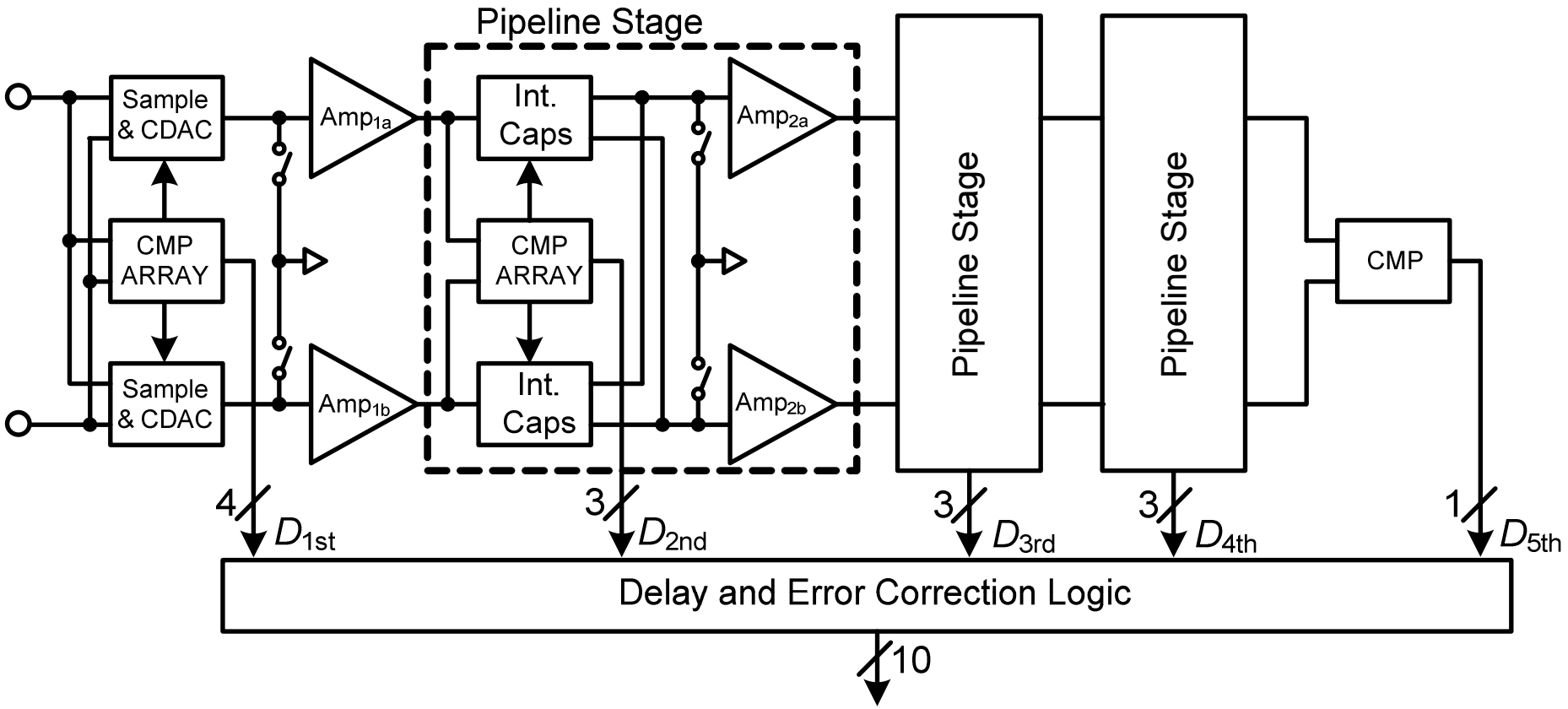
D_{rate}: Data rate
N: ADC's resolution
F_s: Sampling frequency



[1] A. Matsuzawa, *AVIC*, 2012

Interpolated Pipeline ADC

- **10-bit, 320 MS/s with low-gain amplifier**
  - **–No calibration for MDAC stage**

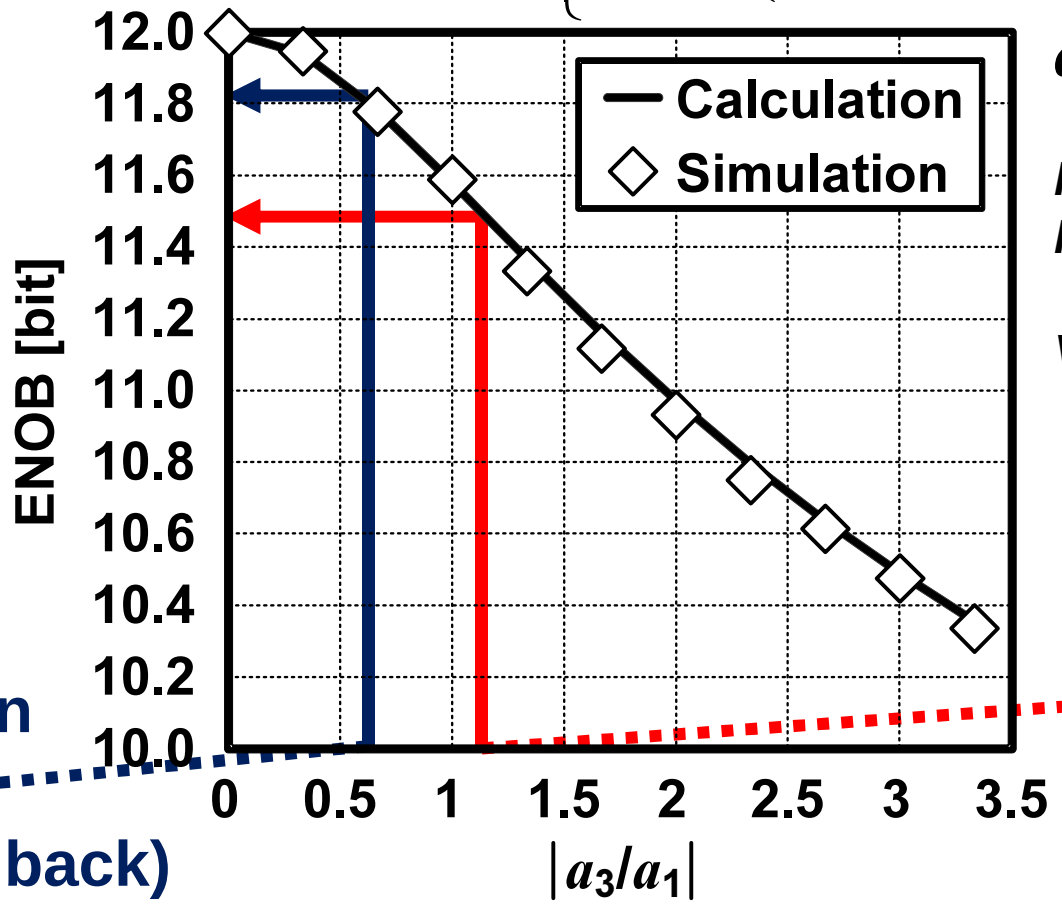


[2] M. Miyahara, *et al.*, *VLSI Circuits*, 2011.

Amplifier's Linearity Issue

- **Open-Loop SD-amp is not enough for 12-bit**

$$\mathrm{ENOB} \approx N - \frac{1}{2}\log_2\left\{1 + 2.9\left(\frac{a_3}{a_1}V_{\mathrm{FS}}^2\, 2^{N-3N_{1\mathrm{st}}}\right)^2\right\}$$



a_3/a_1: Amplifier's non-linearity

N: ADC resolution (12)

N^{1st}: 1st stage resolution (4)

V_{FS}: full-scale reference range (+/- 75 mV)

45-dB gain op-amp (with feedback)

Source Degeneration (SD) amplifier (Open-loop)

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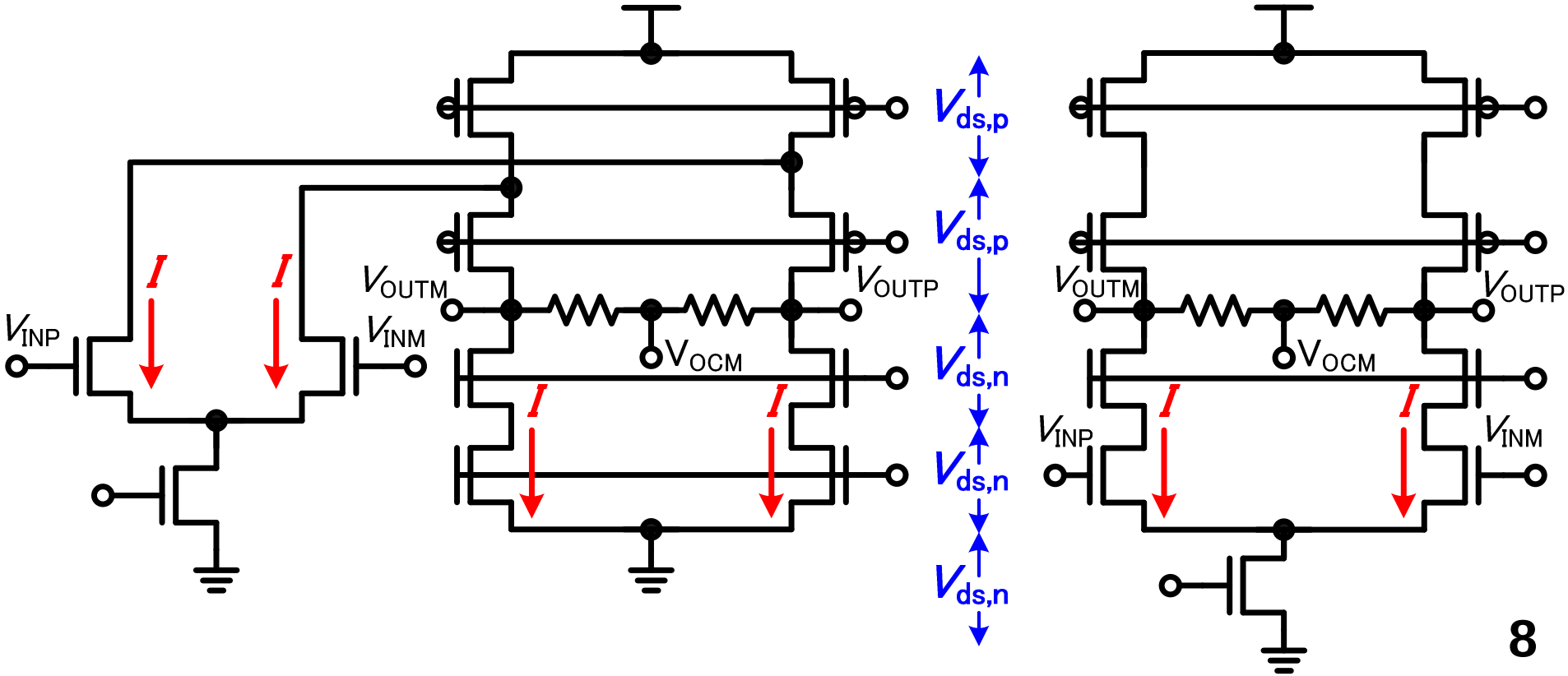
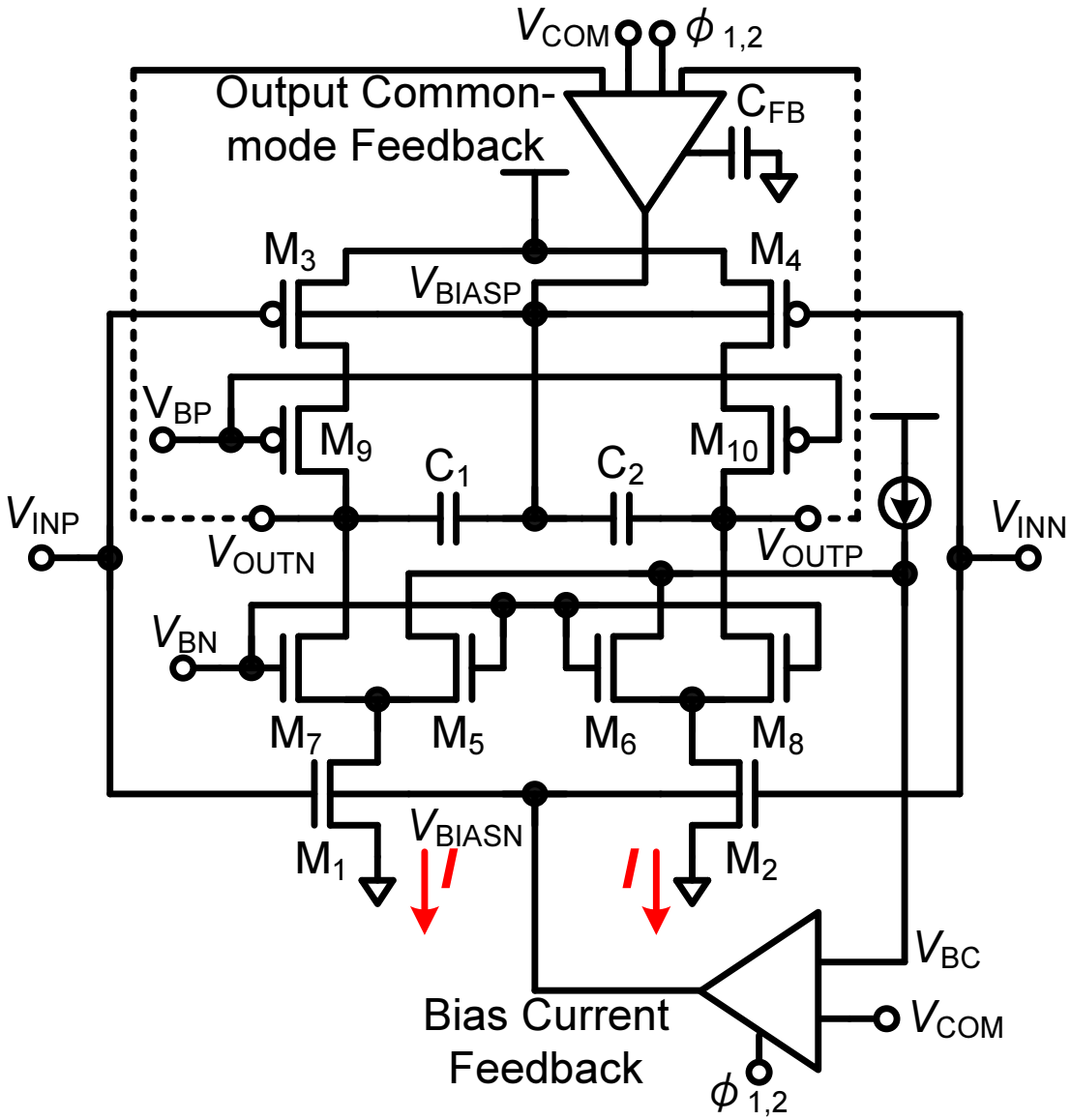
Conventional Amplifier Topologies

	Folded Cascode	Telescopic
Power	High (4*I*)	Low (2*I*)
Swing Range	Wide (V_{DD}-4V_{ds})	Narrow (V_{DD}-5V_{ds})



Body Voltage Controlled Amplifier

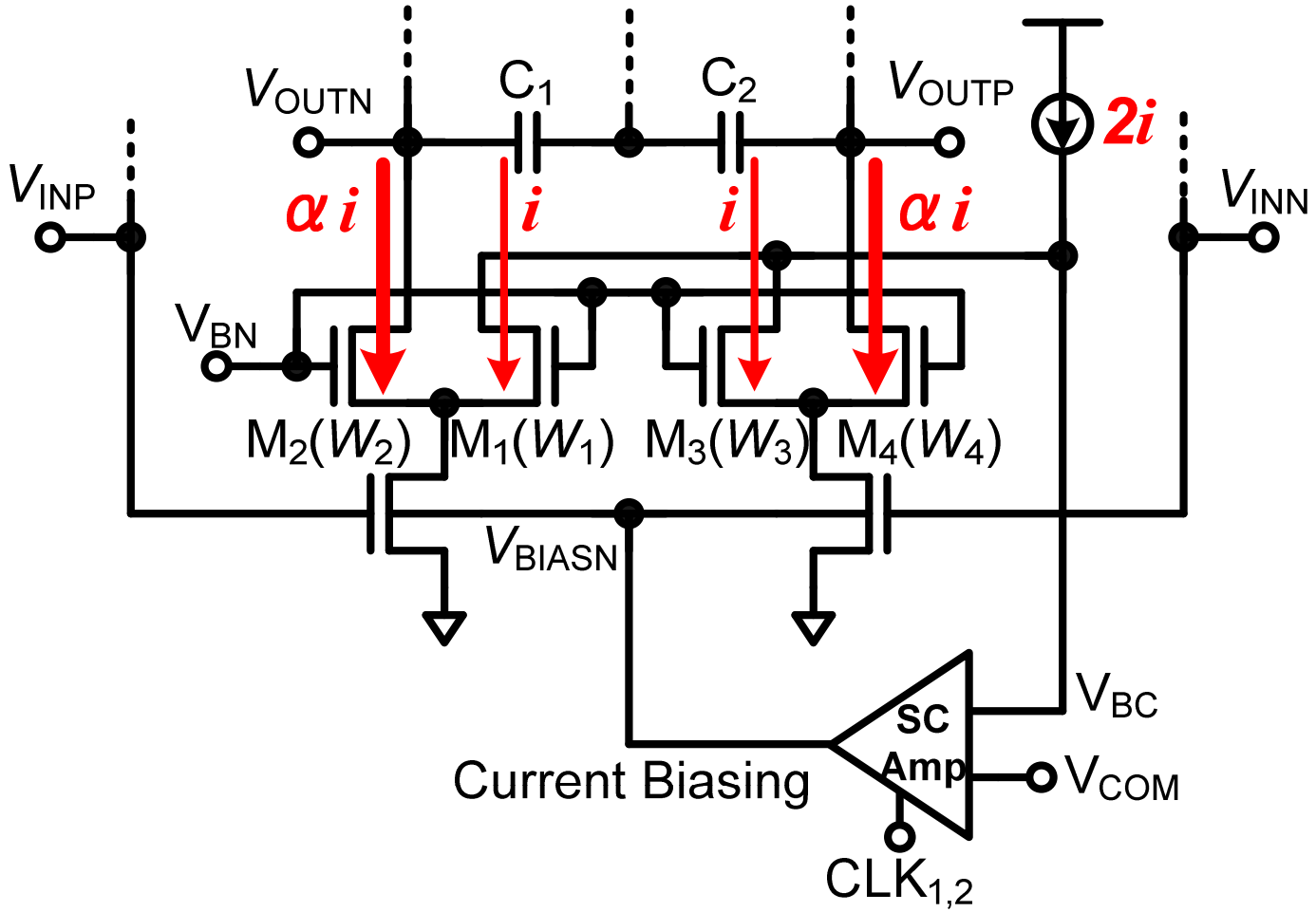


- **Only 2*I* flows**
- **No tail current source**

- **M_1~M_4: Input**
- **M_5~M_6: Current mirroring**
- **M_7~M_{10}: Gain enhancement**

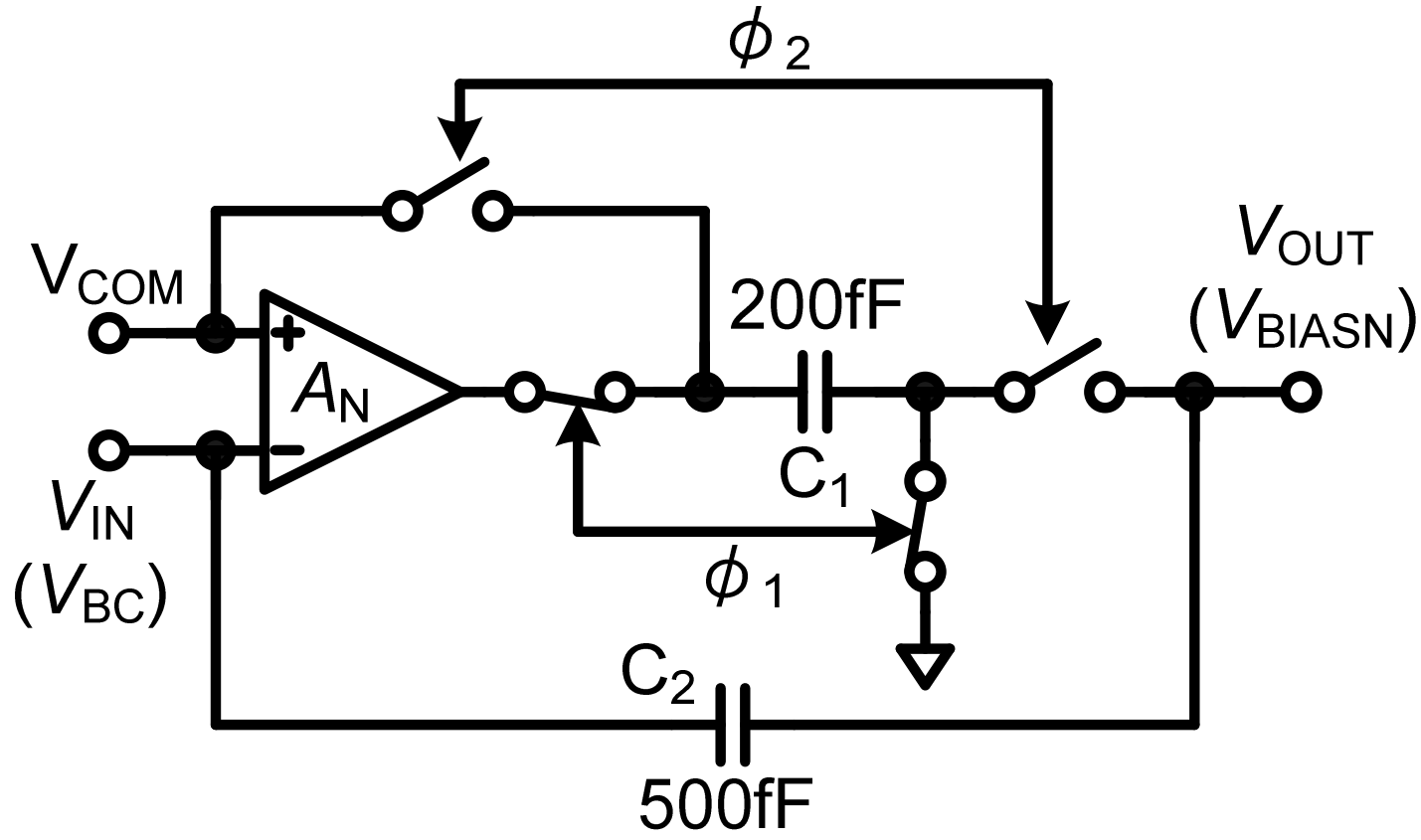
Current Biasing Method

- $W_1 : \alpha W_2 = i : \alpha i \Rightarrow$ Current mirroring
- Current biasing by NMOS body bias control



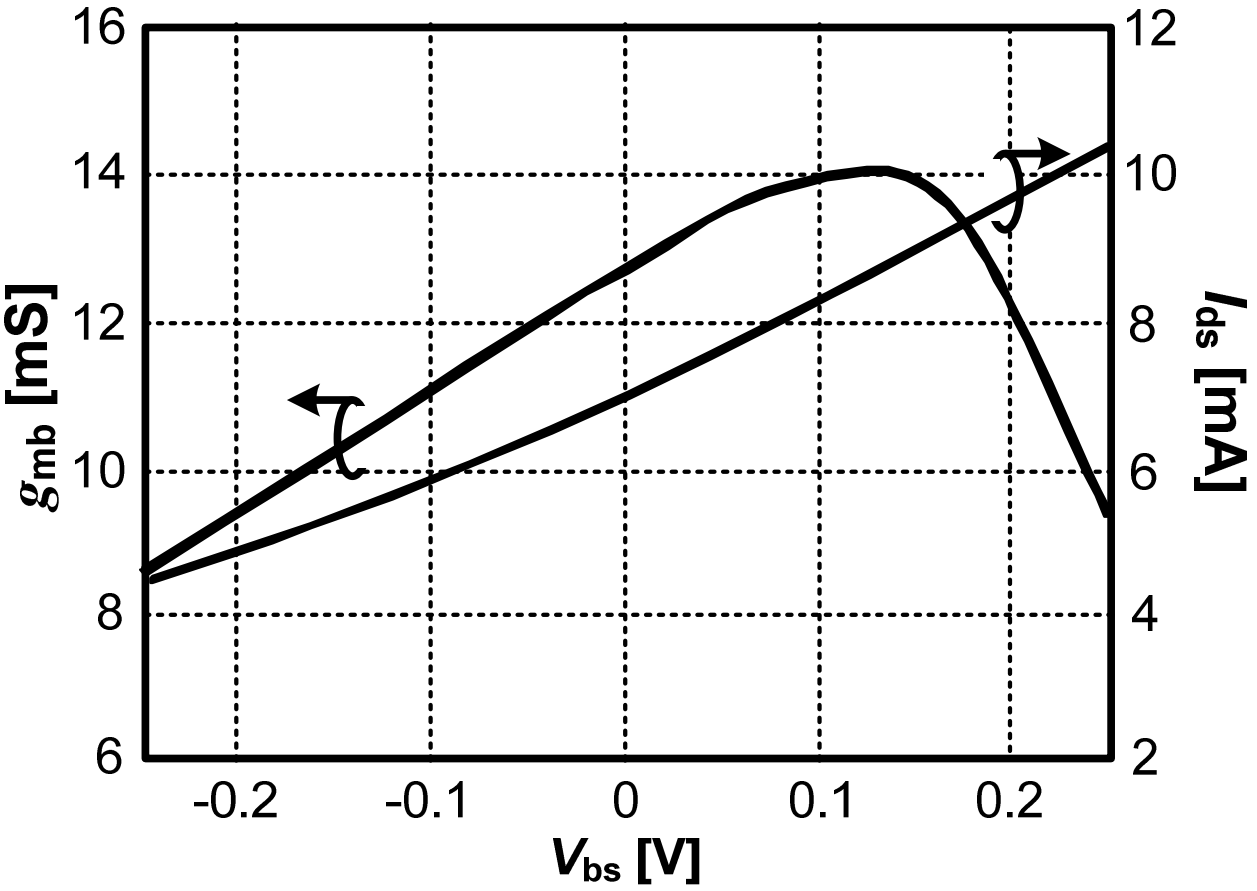
Amplifier for Current Biasing

- Current variation transferred via C_1
- C_2 for generating DC voltage for feedback



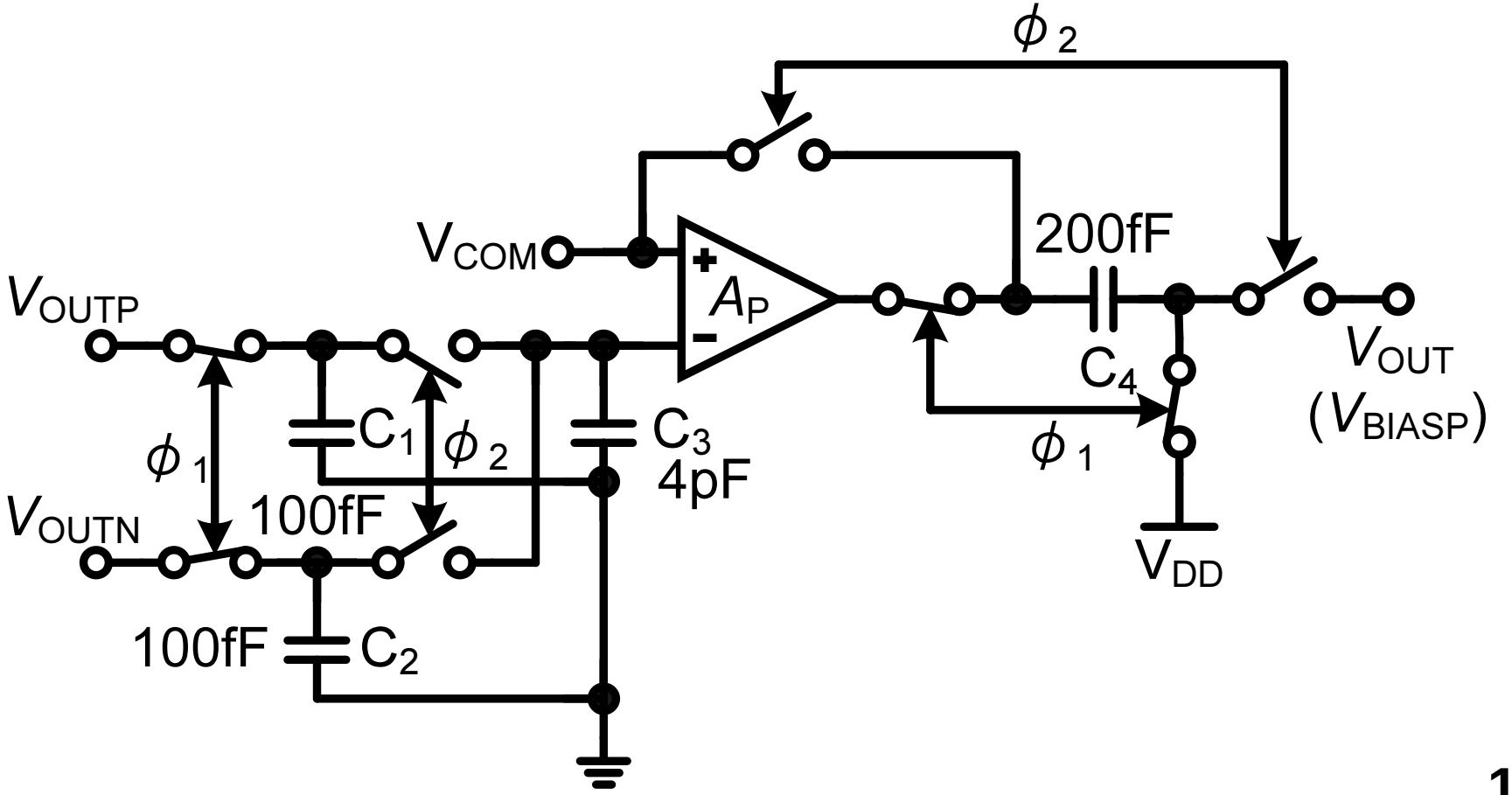
Current Biasing Range

- **Current biasing range : 5.5 ~ 10.5 mA**
- **g_{mb} is maintained higher than 8.5 mS**



Amplifier for CMFB

- Outputs are averaged in C_3
- Averaged voltage is transferred via C_4



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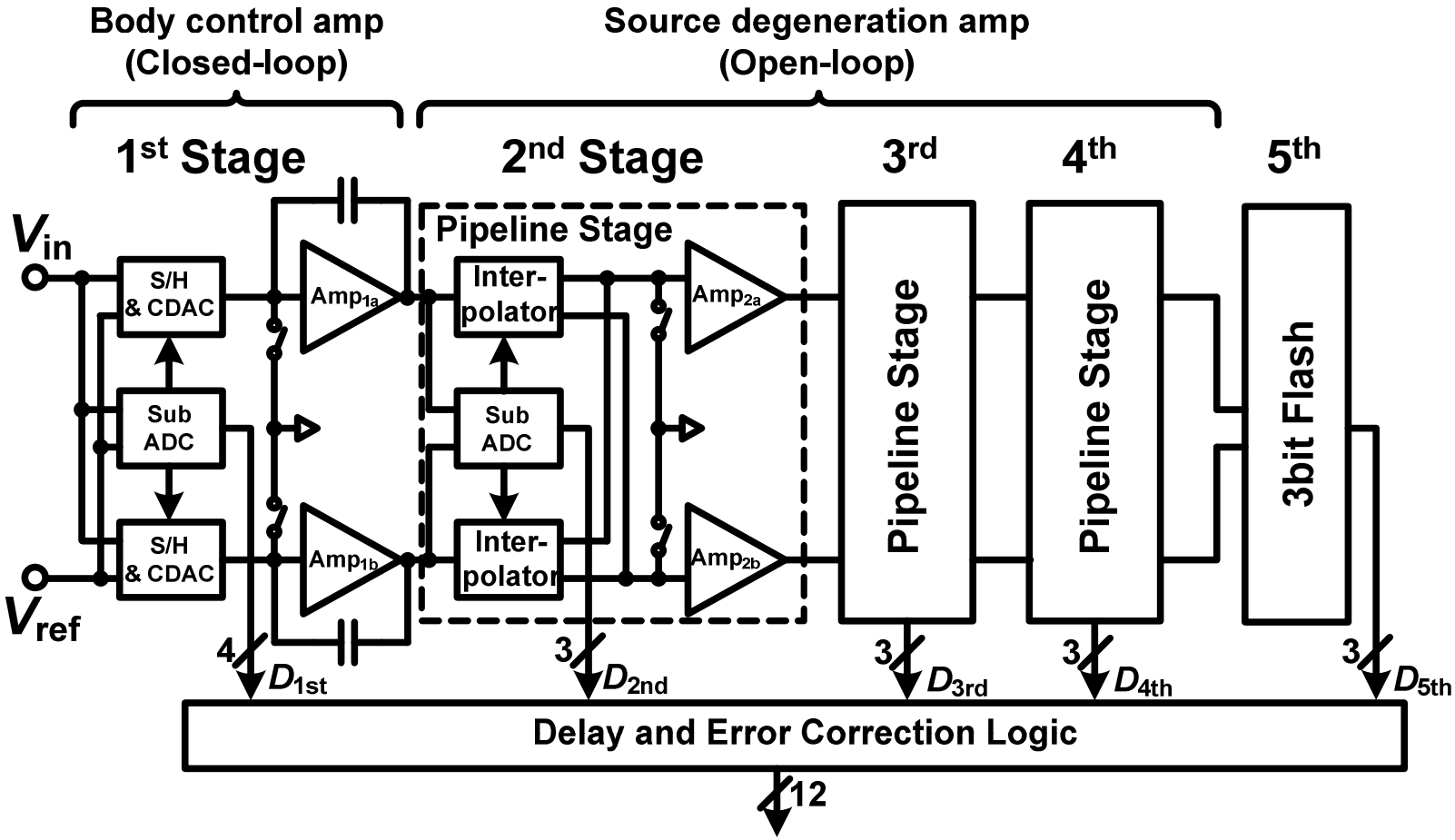
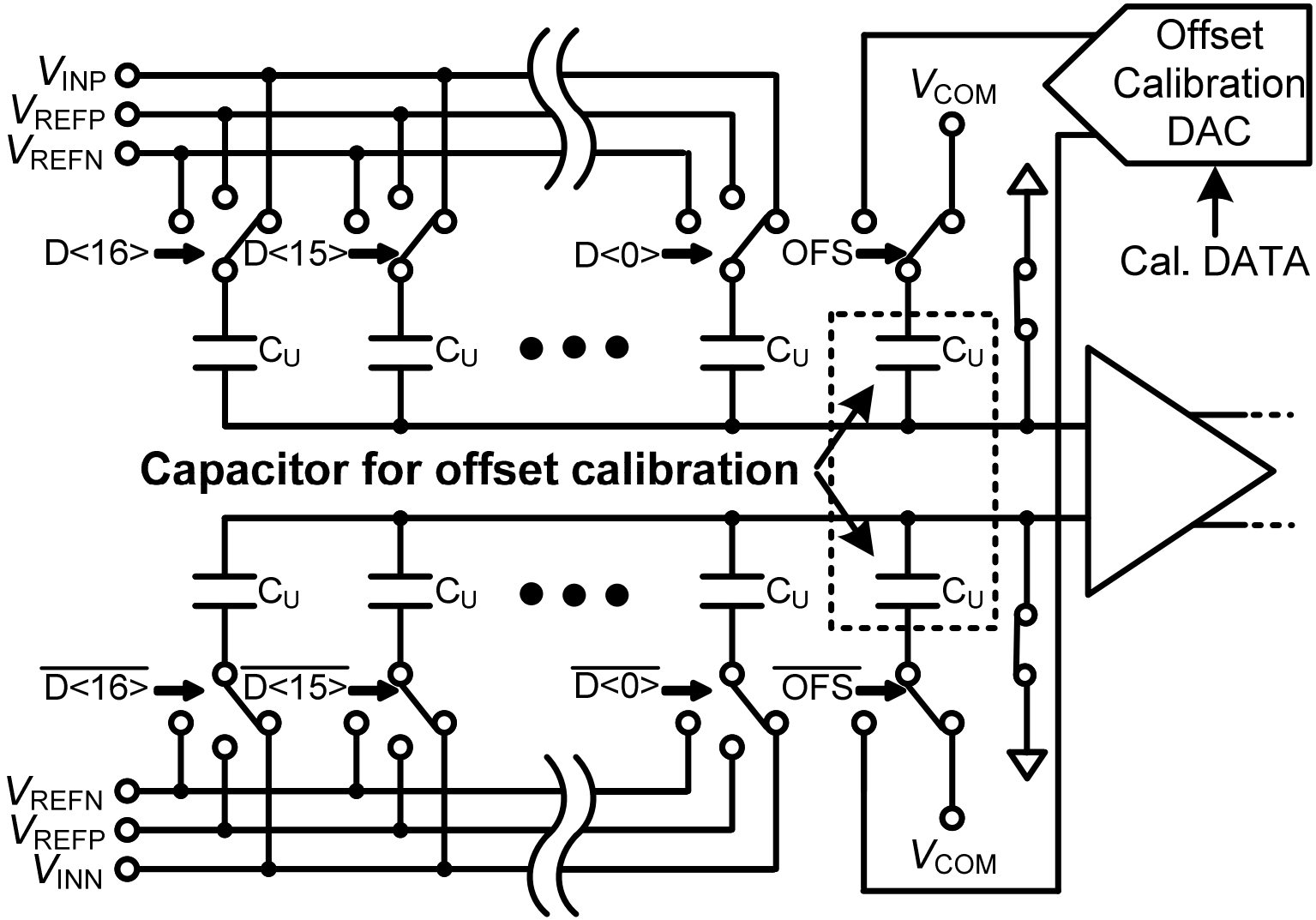
ADC Architecture

- 5 stages (1-bit redundancy in 1st ~ 4th)
- 1st stage utilizes closed-loop topology



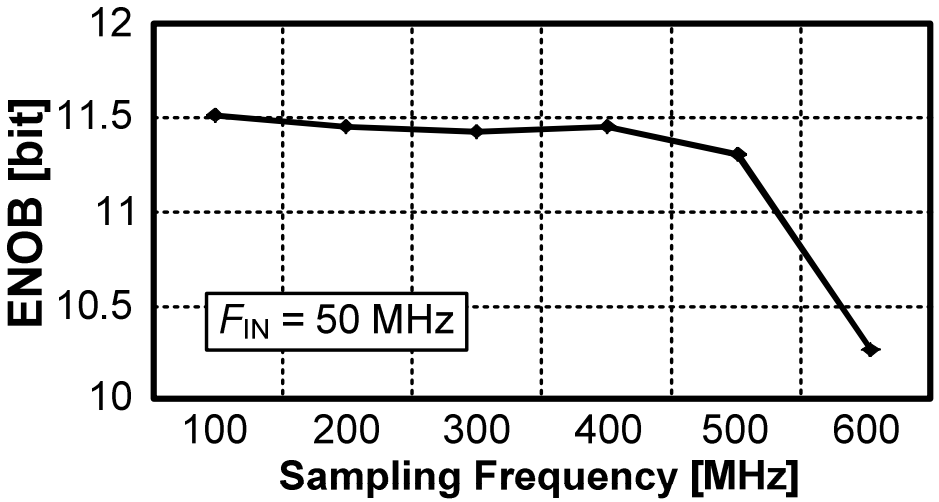
Amplifier's Offset Calibration

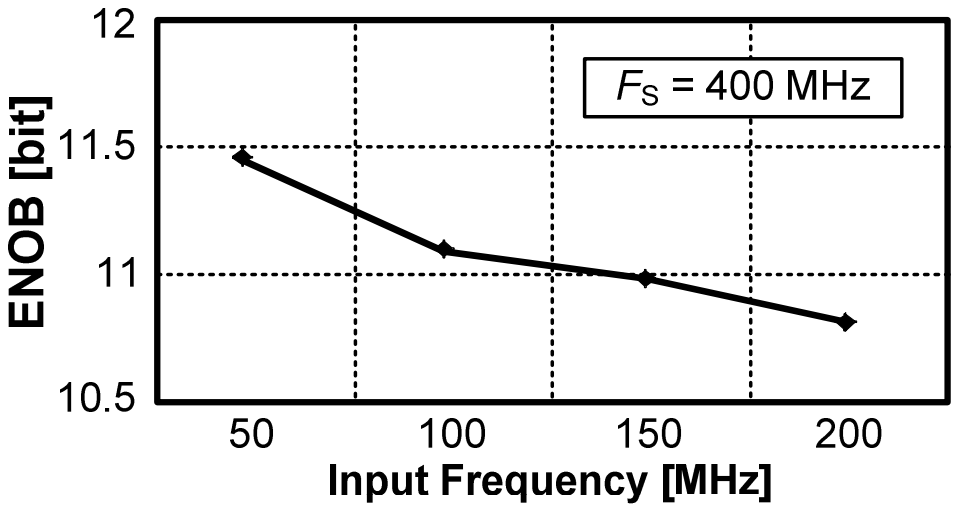
- **Amplifier's offset is cancelled by DAC**



AC Simulation Results

- ENOB keeps higher than 11.5-bit until 400 MS/s @ 50 MHz input
- 10.8-bit of ENOB is achieved @ 400 MS/s and Nyquist input

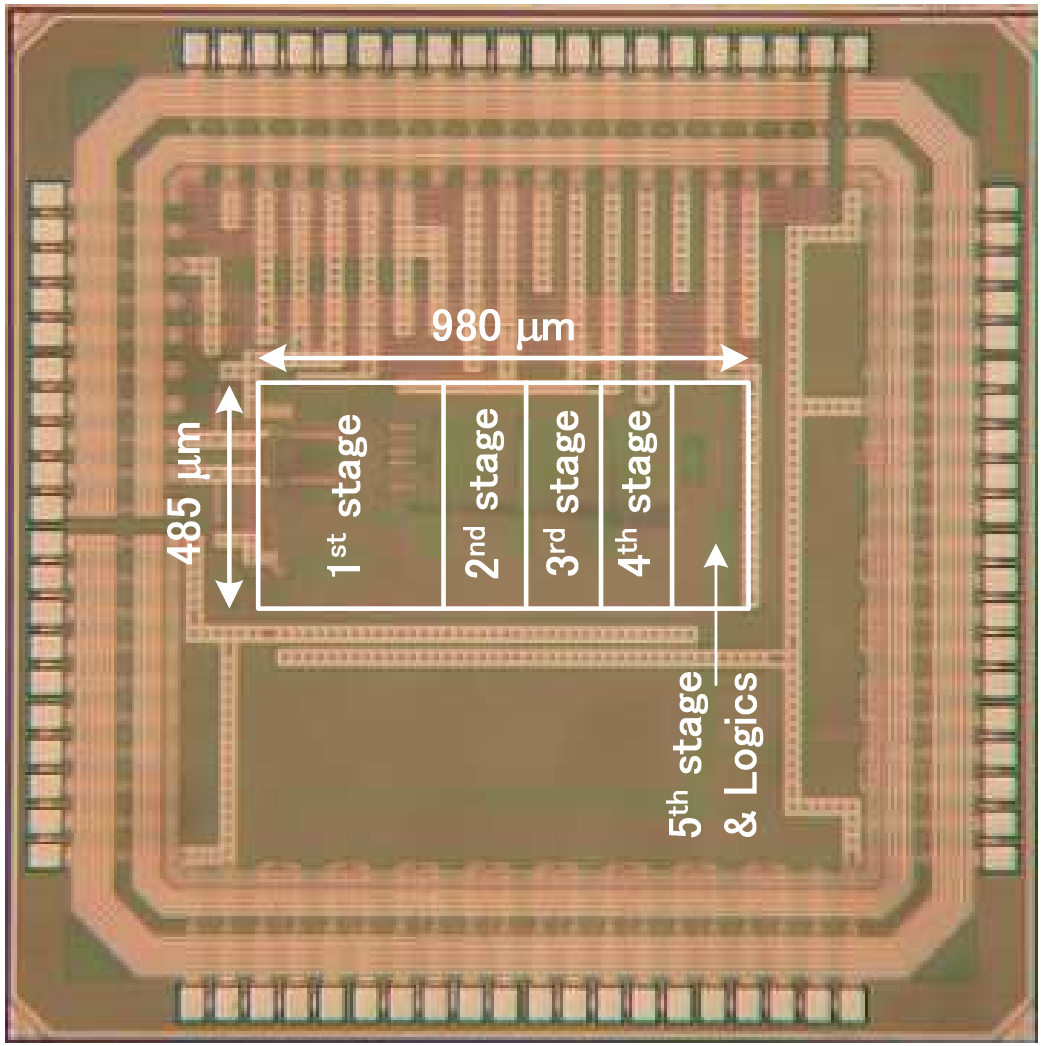




- All transistor model
- Room temperature
- Without transient noise and component mismatch

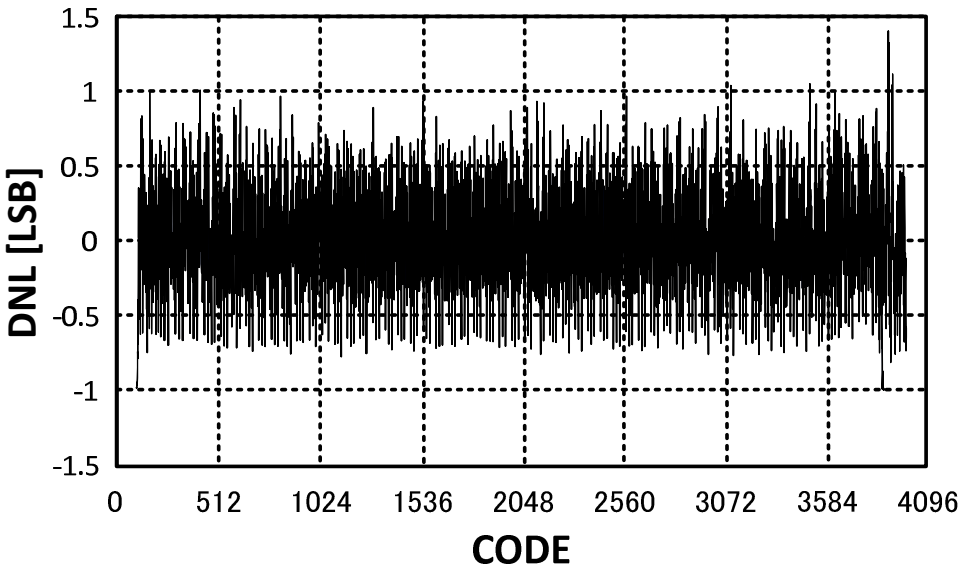
ADC Chip Photo

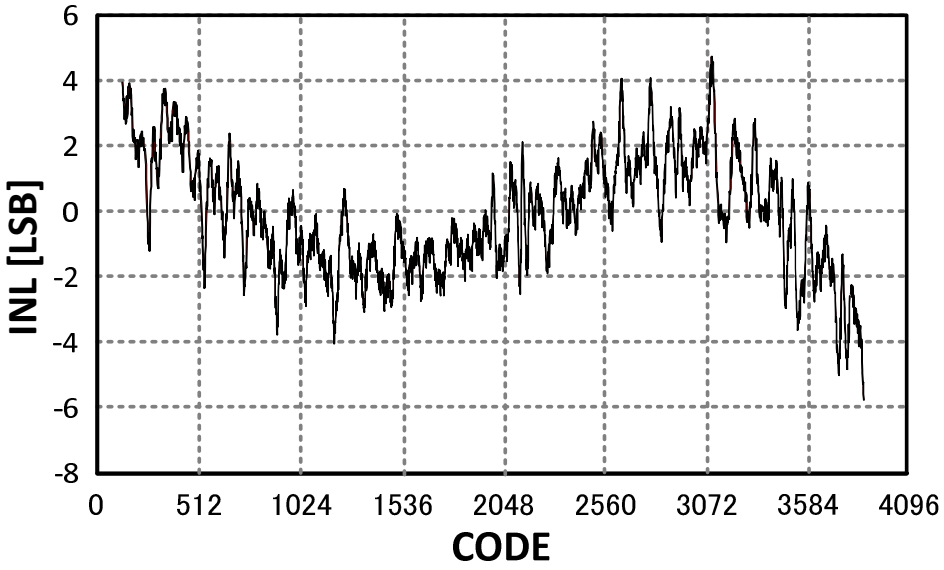
- 1P9M 90 nm CMOS, Core area is **0.48 mm^2**



DC Measurement Results

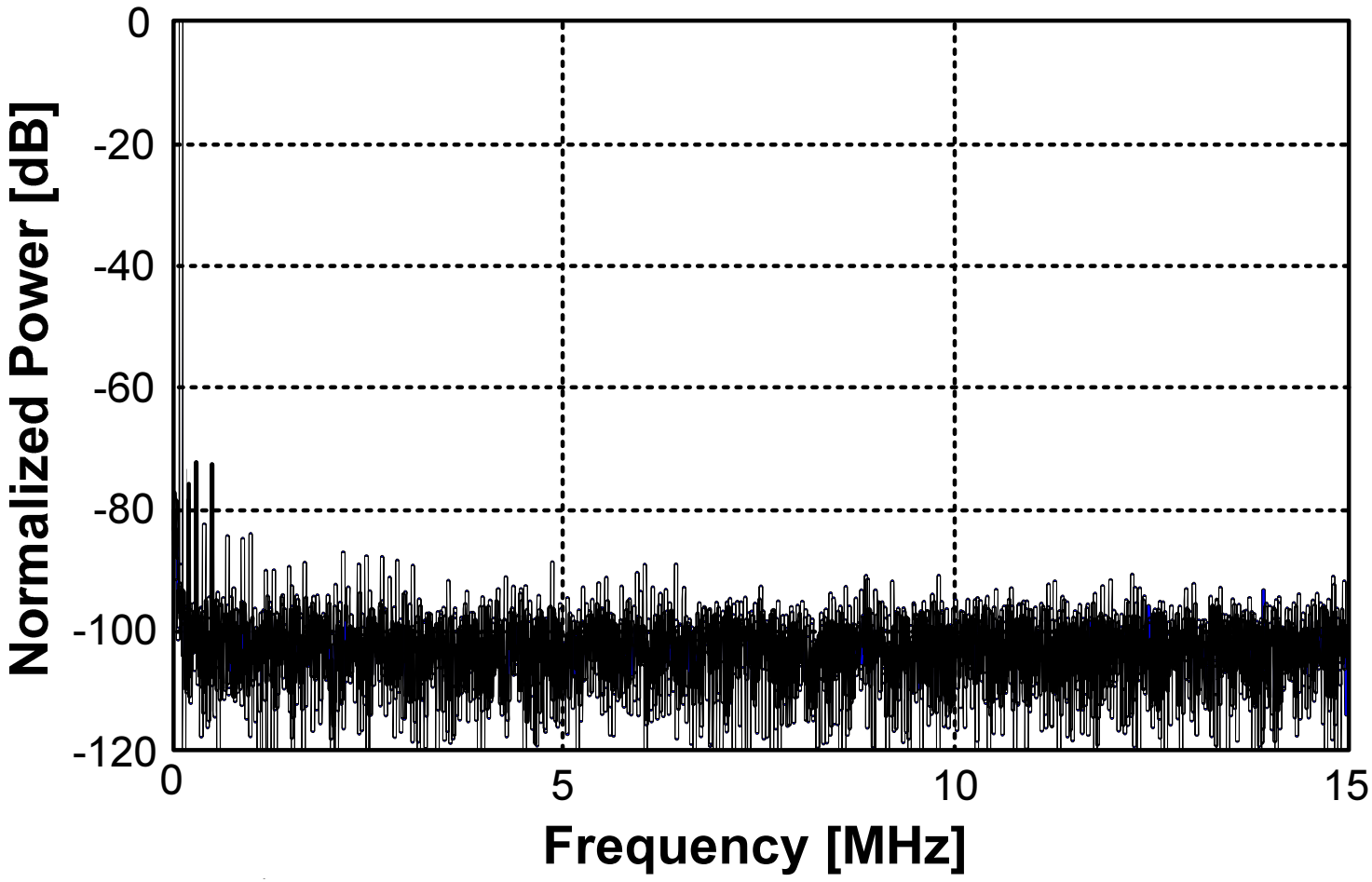
- DNL: + 1.4 / - 1
- INL : + 4.5 / - 5.8
- DC characteristic is degraded by parasitic components in input and ref. nodes





Measured FFT Spectrum

- 300 MS/s and 100 kHz input
  - 10-bit of ENOB is achieved



Amplifier Performance Table

- To achieve 12-bit, 400 MS/s ADC operation,

Topology	Body voltage control
DC Gain [dB]	45
Power Consumption [mW]	15.6 (↓40 % from Folded-Cascode)
Settling Time [ps]	500
Output Swing Range [mV_{pp}]	600 (↑12.5 % from Telescopic)

ADC Performance Table

	This work	[3]	[4]	[5]
Resolution [bit]	12	12	12	12
F_{sample} [MS/s]	300	800	1000	3000
V_{DD} [V]	1.2	1 / 2.5	1.8 / 3.3	1 / 2.5
Power [mW]	60	105	550	500
$ENOB_{peak}$ [bit]	9.96 (100 kHz)	9.5	9.5 (by SNR)	9.5
FoM [pJ/conv.]	0.2	0.18	0.76	0.23
Technology [nm]	90	40	180 (SiGe)	40
Core Area [mm^2]	0.48	0.88	2.35	0.4
Linearity Compensation	No	Yes	Yes	Yes
Interleave	No	4-times	No	2-times

[3] D. Vecchi, *et al*., JSSC 2011. [4] R. Payne, *et al*., ISSCC 2011.
[5] C. Y. Chen and J. Wu, VLSI Circuits, 2011.

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Conclusion

- **Body voltage controlled amplifier is proposed**
  - **Low power consumption & wide swing range**
- **12-bit, 300 MS/s interpolated pipeline ADC with proposed amplifier is demonstrated**
  - **No linearity calibration**
  - **ADC achieves 10-bit of ENOB with slow input**
- **Performance can be improved by elimination of input parasitic components**

Acknowledgement

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Thank you for your interest!

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