学生17

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積分器とSARADCを用いた1ps分解能の時間・デジタル変換器

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Abstract

- We propose a time-to-digital converter (TDC) that uses a Gm-C integrator to translate the time interval into voltage, and quantizes this voltage with a SAR-ADC. The proposed method is capable of achieving pico-second resolution, avoiding limitations in delay-chain-based TDCs, such as logic gate propagation delay, mismatches, and voltage surges. Furthermore, taking the advantages of SAR-ADC, small area and low power consumption of voltage quantization are attainable. The chip was fabricated in 90nm CMOS. Its measured DNL and INL are -0.6/0.7 LSB and -1.1/2.3 LSB, respectively, with 1ps per LSB in a 9-bit range.

Outline

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- Motivation and Previous Solutions
- Integrator-Based Time-to-Digital Converter
- Circuits Design
  - Level Shifter
  - Gm-C Integrator
  - SAR-ADC
- Implementation and Measurement
- Conclusion

Motivation

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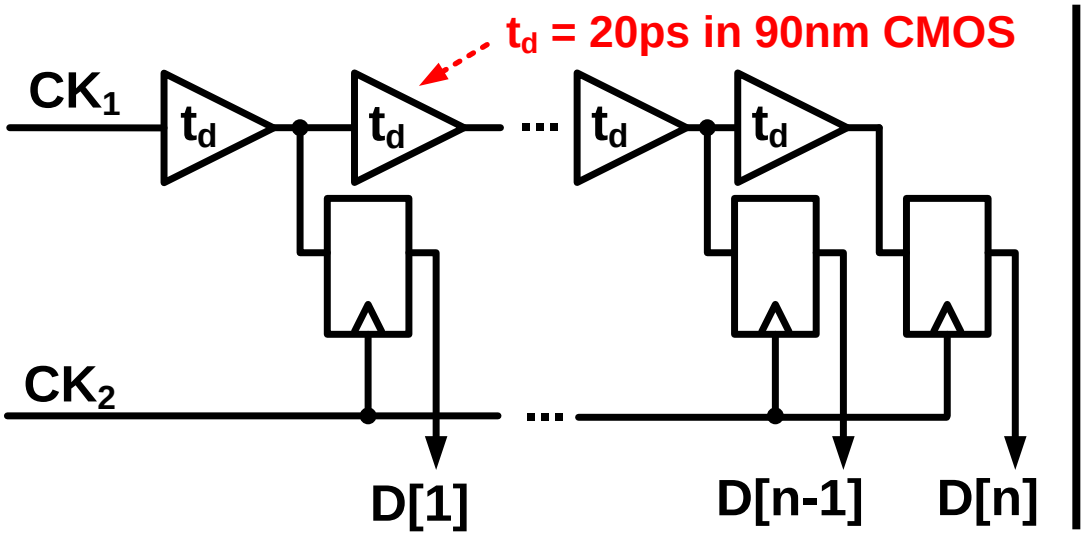
- **Pico second time resolution is challenging**
- **Delay-chain TDC does not serve for it**

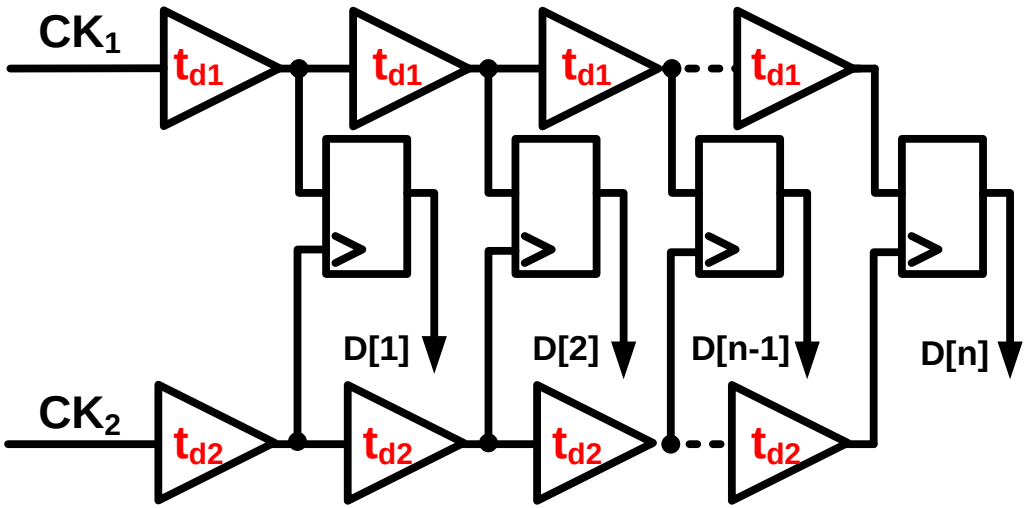


- **Systems that demand pico second resolution**
  - **ToF imaging**
  - **Laser range finder**
  - **Digital PLL, etc.**

Previous Solutions

- **Vernier TDC typically uses a DLL against PVT but consumes extra power**
- **Mismatch among stages still exists**

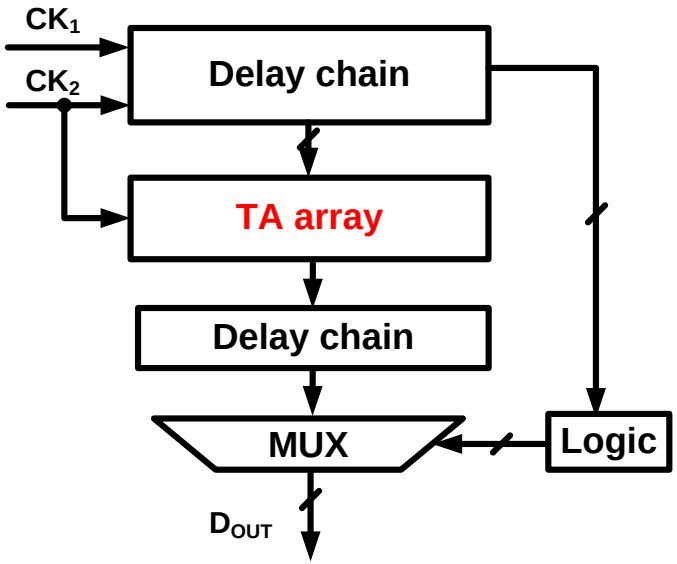
($t_{d1} - t_{d2}$) varies on each stage by PVT



Previous Solutions

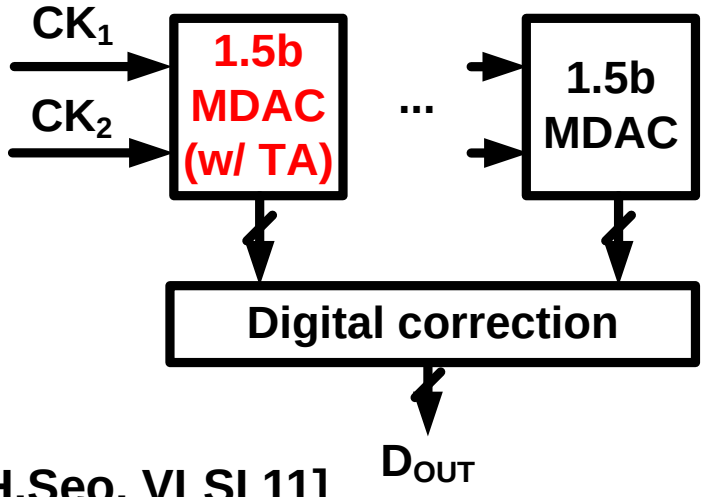
- **Time amplifiers (TA) suffer nonlinearity and mismatch**
- **Too many calibrations are required**

Coarse - fine



[M.Lee, JSSC 08]

Pipeline

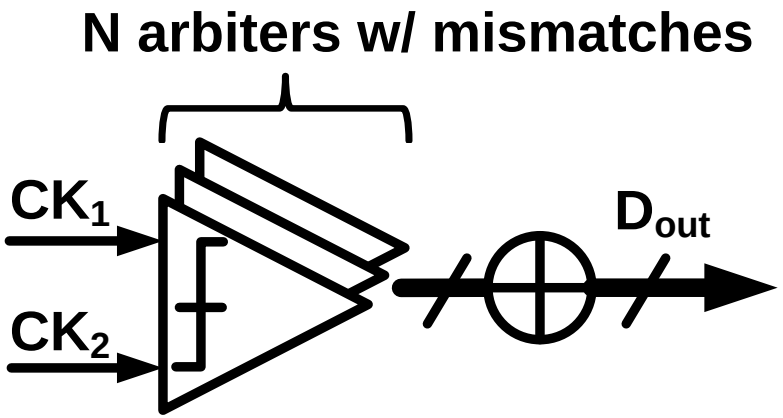


[Y.H.Seo, VLSI 11]

Previous Solutions

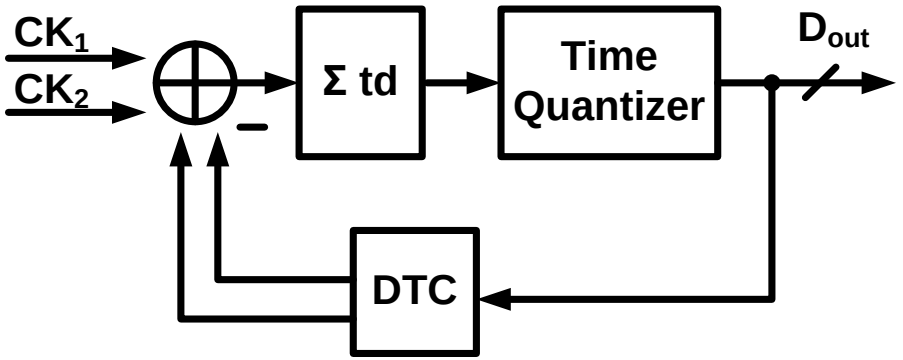
- Stochastic TDC suffers short range
- Delta-sigma TDC's input bandwidth is low

Stochastic



[V.Kratyuk, TCAS-I 09]

Delta-Sigma



[J.P.Hong, ISSCC 12]

Integrator-Based TDC

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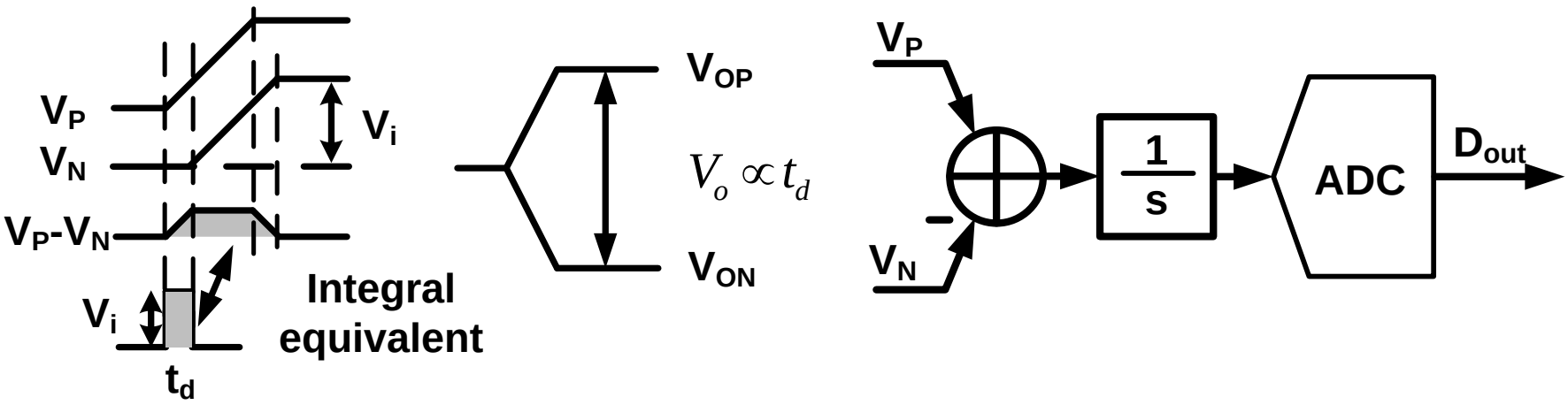
- **Integral is proportional to time**
- **No limitation of logic gate delay**
- **Few calibrations are required**



Integrator-Based TDC

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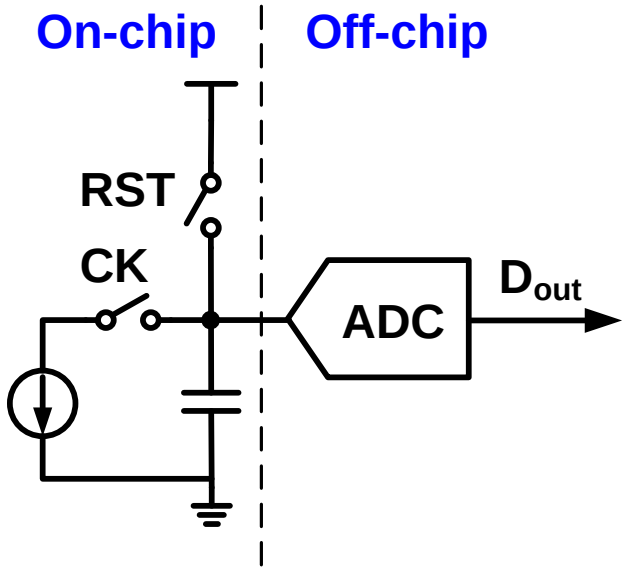
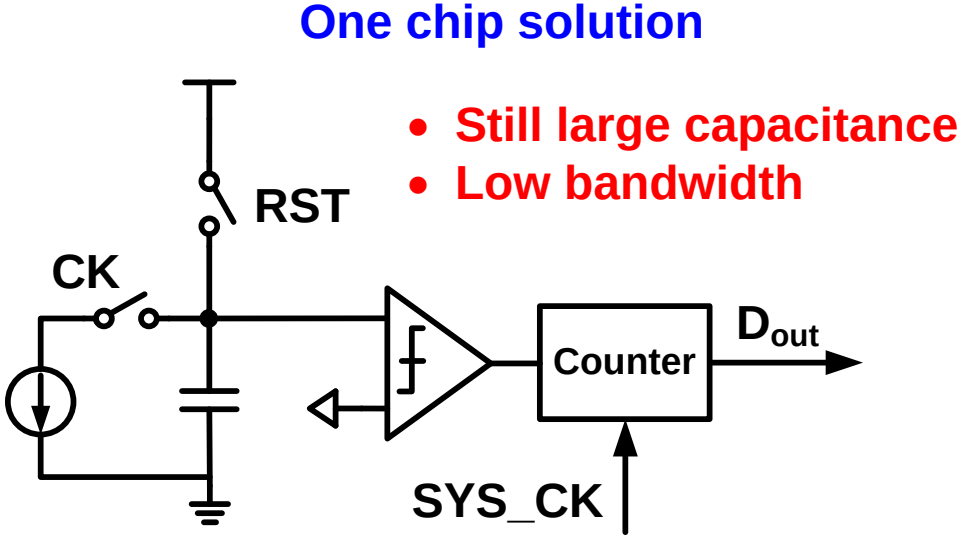
- **Solutions in old days…** $t = CV / I$
- **Large capacitance and ADC pose resolution, density and power issues**



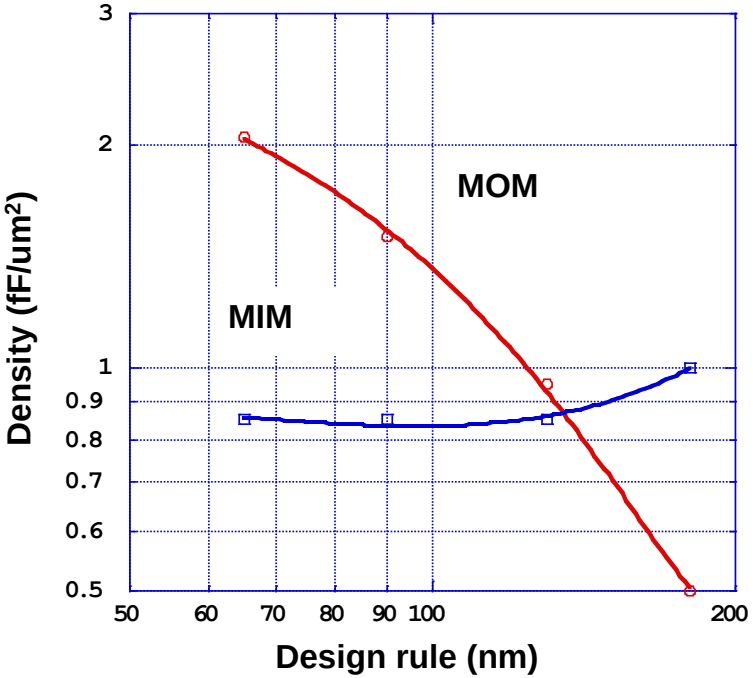


[E.R.Ruotsalainen, JSSC 00]

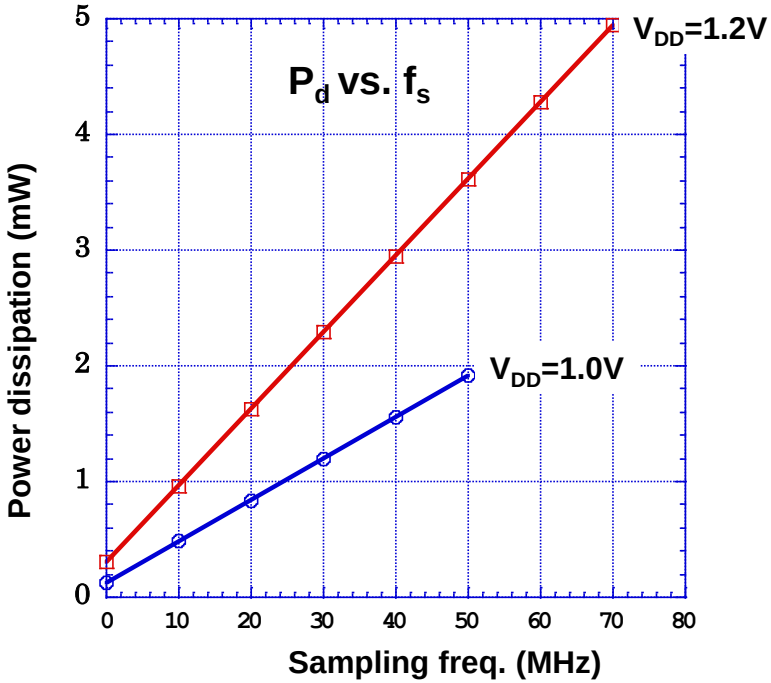
Integrator-Based TDC

- **Proposal: use MoM capacitors and SAR-ADC**

MoM: better density

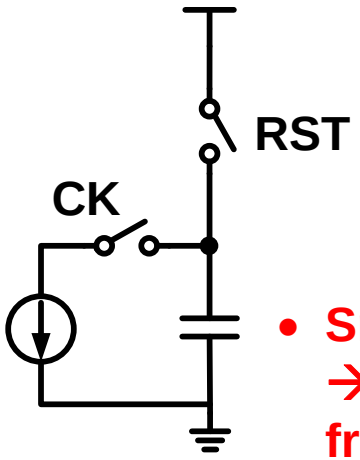


SAR-ADC: low and dynamic power

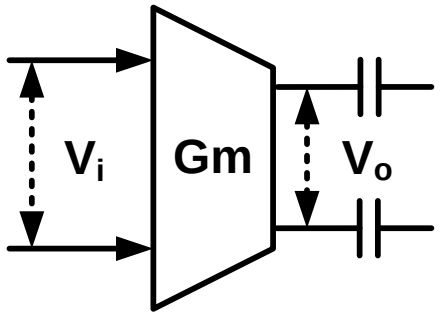


Integrator-Based TDC

- When capacitors become small → charge injection, charge sharing, and clock feed-through can be worse
- Solution: fully-differential Gm-C



- Small capacitor → more error from the switch



$$t = \frac{CV_o}{GmV_i}$$

- Differential and no switch controlled integration

Architecture

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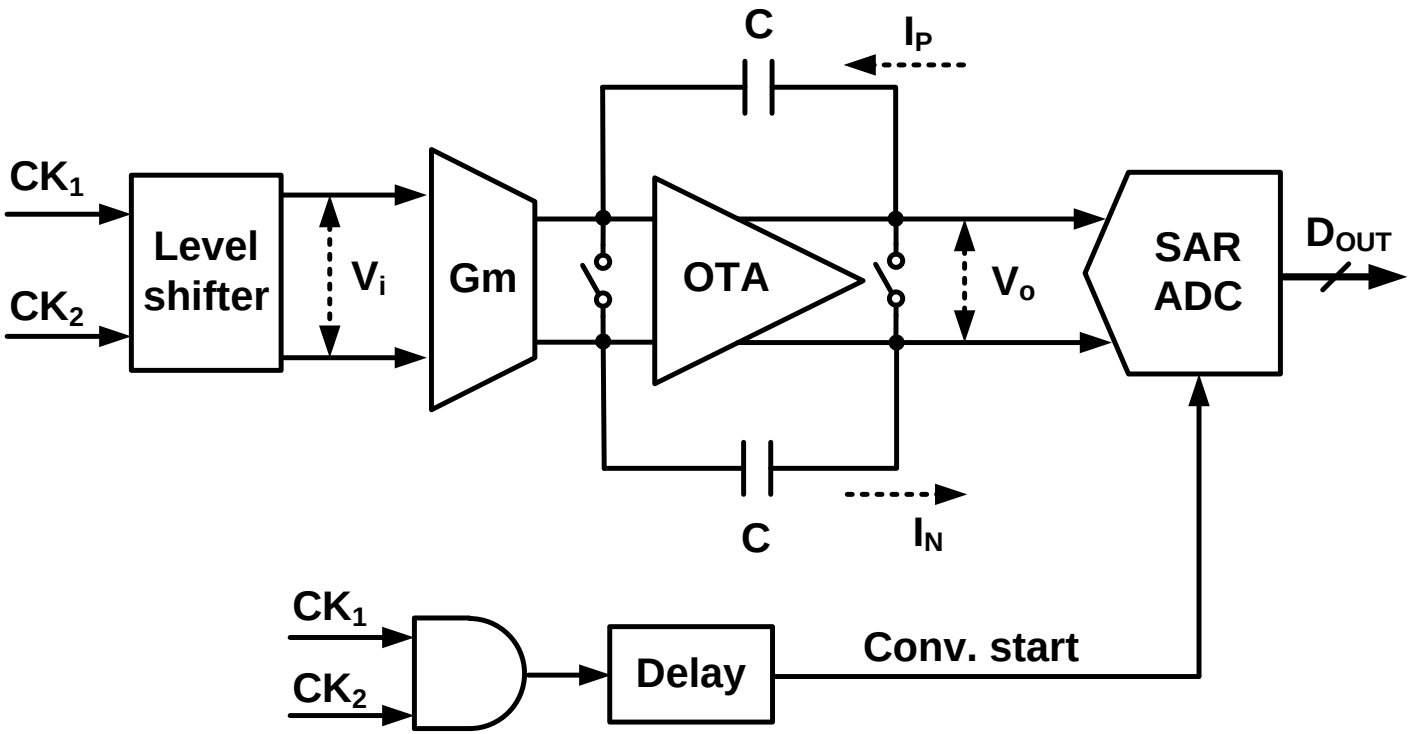
- Level shifter interfaces digital and analog
- OTA enhances Gm's output resistance



Level Shifter

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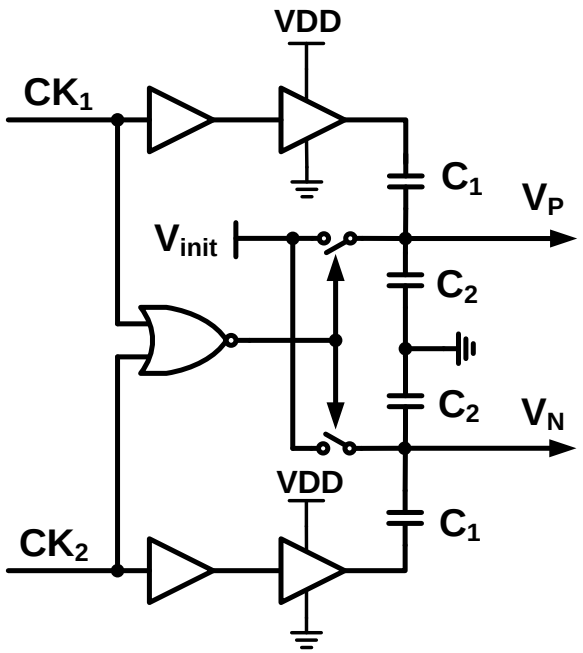
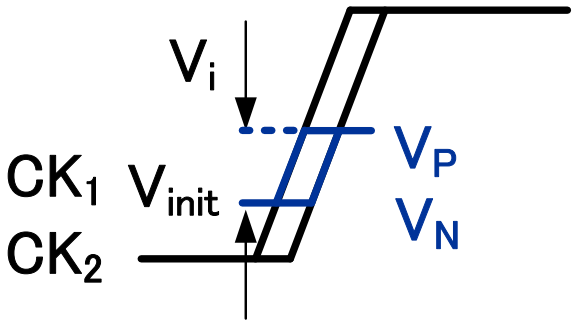
- Level shifting during rising of CK_1 and CK_2
- Larger amplitude (V_i) → finer resolution but poorer linearity

No static current





$$V_i = \frac{C_1}{C_1 + C_2} V_{DD}$$

Gm-C Integrator

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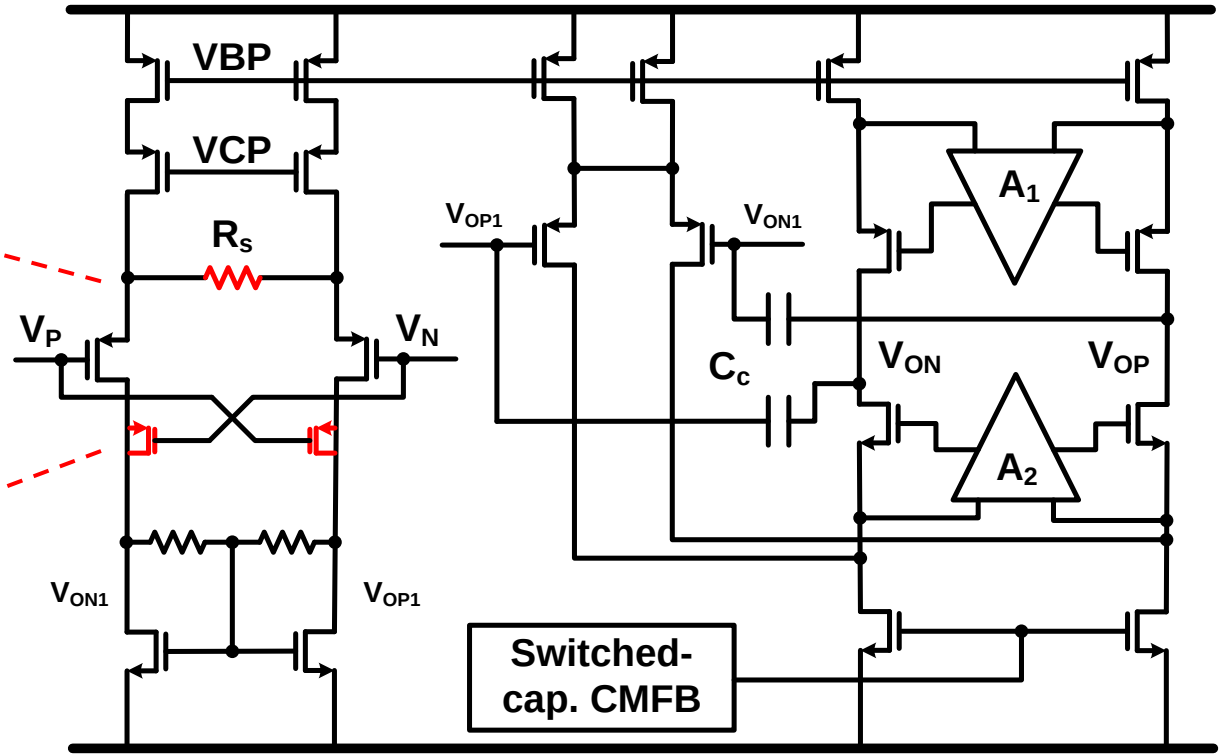
- **Source degeneration and neutralization capacitor**

To increase linearity

To balance kickback and input feed-through



SAR-ADC

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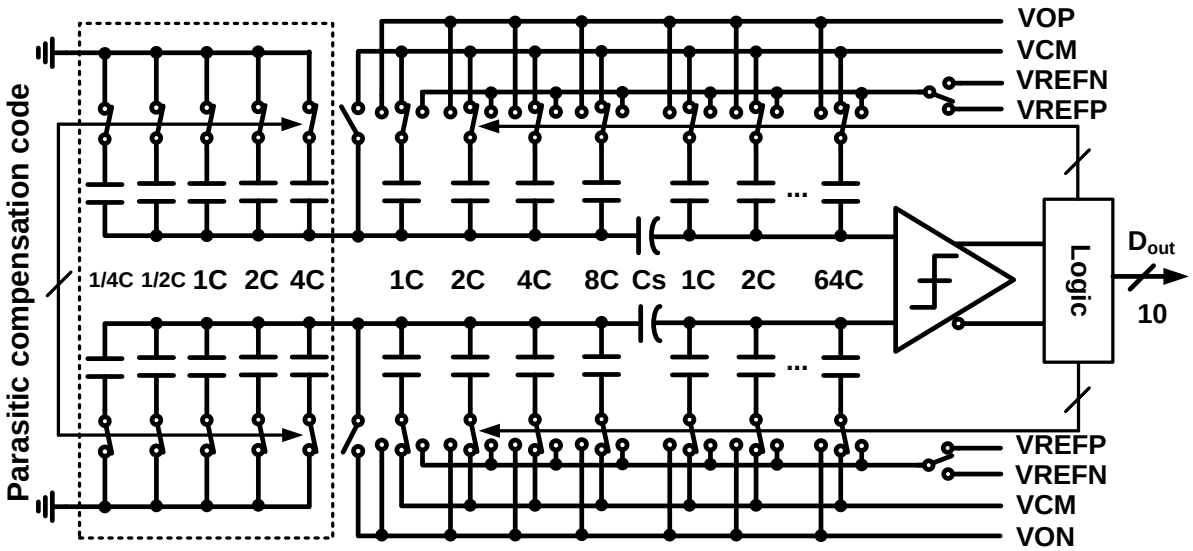
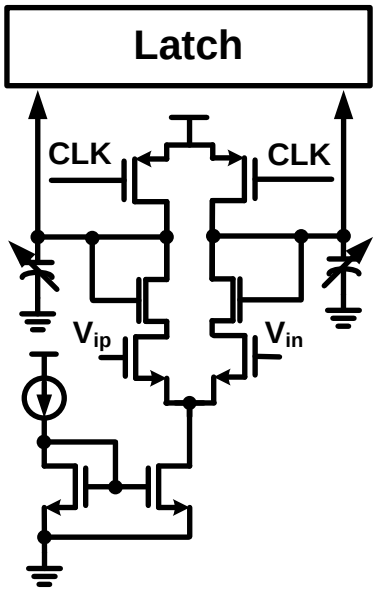
- **ENOB = 9.8-bit**
- **1mW@10MHz, 0.15mm²**

SAR-ADC (12-bit topology)



Dynamic comparator



Implementation

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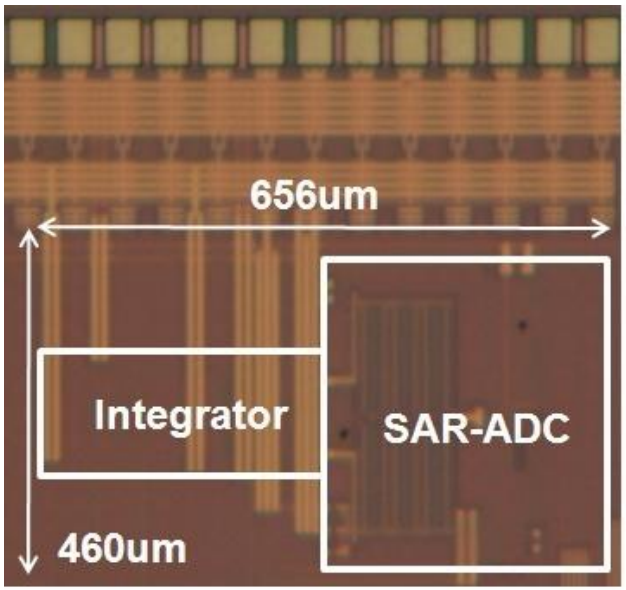
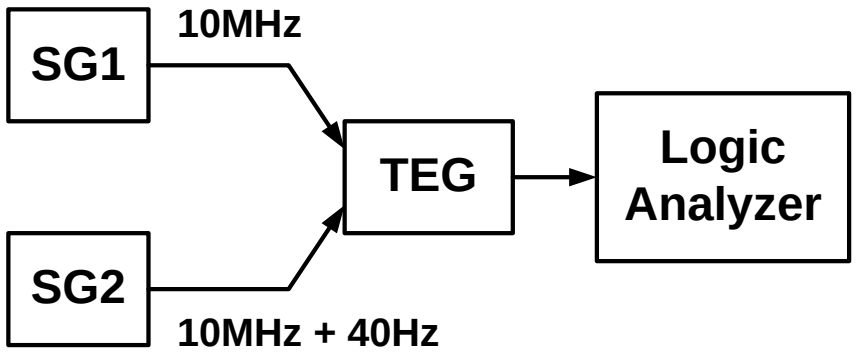
- CMOS 90nm, 0.31mm^2
- Area of SAR-ADC can be reduced to 1/8 if a 10-bit topology is designed



Measurement setup



Measurement

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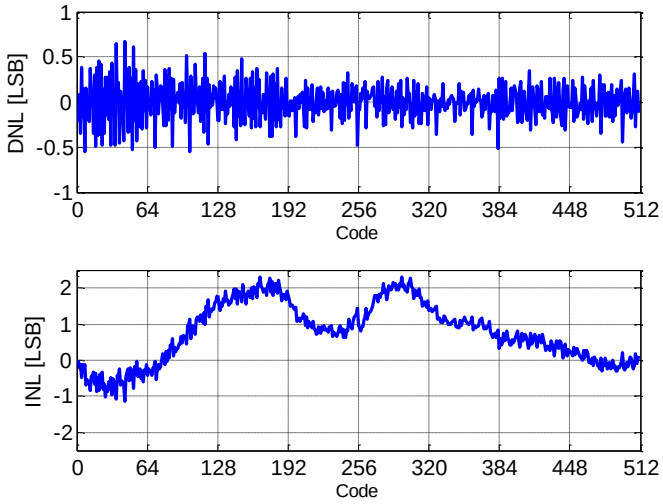
- **1ps LSB was obtained without calibrations**
- **Power can be reduced by improving the integrator**

DNL/INL



Performance comparison

	TNS'07	VLSI'11	ESSCIRC'10	**This work**
Type	Vernier	Pipeline	Stochastic	Integrator
CMOS [nm]	130	130	65	90
Supply [V]	3.3	1.3	1.2	1.2
Resolution [ps]	37.5	0.63	3	1
Range [ps]	2000	1300	52	±256
DNL [LSB]	0.2	0.5	1.4	-0.6/0.7
INL [LSB]	0.35	2	1.5	-1.1/2.3
Area [mm^2]	0.22	0.32	0.04	0.31
Frequency [MS/s]	0.1	65	40	10
Power [mW]	150	10.5	8	20.4

Conclusion

- **Voltage domain is still more resolvable for high resolution TDC**
- **SAR-ADC is a promising solution to integrator-based TDC**
- **Few calibrations are required comparing with time-domain solutions**
- **Power and area will be improved**