A Digitally-Calibrated 20-Gb/s 60-GHz Direct-Conversion Transceiver in 65-nm CMOS

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***Abstract*— This paper presents a digitally-calibrated 60-GHz direct-conversion transceiver. To improve the error vector magnitude (EVM) performance over the wide bandwidth, a digital calibration technique is applied. The 60-GHz transceiver implemented by 65 nm CMOS achieves the maximum data rates of 20 Gb/s in 16QAM mode. The transmitter and receiver consume 351 mW and 238 mW from 1.2V supply, respectively. As a 60-GHz transceiver, the best Tx-to-Rx EVM performance of -26.2 dB is achieved for 16QAM 7Gb/s data rate.**

***Index Terms*— CMOS, 60GHz, millimeter-wave, direct-conversion transceiver, calibration, IQ-mismatch**

I. Introduction

Due to the demand for multi-Gb/s wireless communication, the millimeter-wave wireless transceiver has been studied. The carrier frequency of 60 GHz is one of the most promising bands because there is up to 9-GHz unlicensed bandwidth. According to the IEEE 802.11ad standard [1], four 2.16- GHz bandwidth channels are defined around the 60-GHz, and it is capable of achieving 7 Gb/s per channel for 16QAM modulation.

The 60-GHz transceivers implemented by CMOS technology have been reported using the hetero-dyne architecture [2]–[4]. For lower power consumption and smaller chip area, direct-conversion transceivers have been also reported [5]–[8]. However, it is still challenging to achieve more than 10 Gb/s data rate due to (1) I/Q mismatch (2) gain flatness (3) phase noise, which degrade the error vector magnitude (EVM) performance. The direct-conversion transceivers in [6]–[8] employ a quadrature injection-locked oscillator for the phase noise improvement. The issues of I/Q mismatch and gain flatness are still remaining especially for achieving higher data rate with wider bandwidth. Thus, this paper proposes a 60-GHz direct-conversion transceiver using a digital calibration technique for improving I/Q mismatch with gain-peaking amplifiers. Three-step loop-back oscillator calibration for injection-locked oscillators, and loop-back I/Q mismatch calibration are applied.

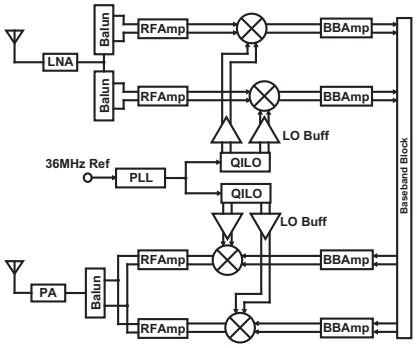
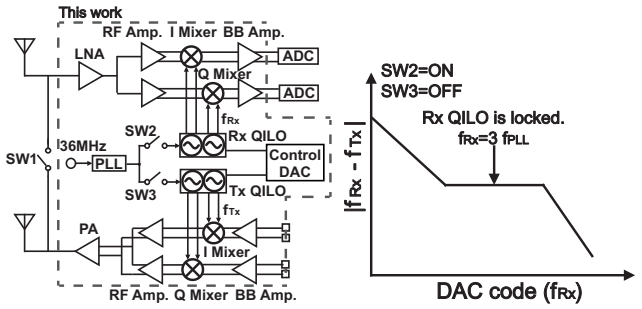


Fig. 1. Block diagram of the proposed 60-GHz direct-conversion transceiver.

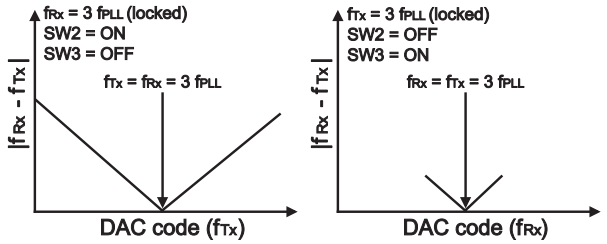
II. Proposed Digitally-Calibrated Direct-Conversion Transceiver

Fig. 1 shows the block diagram of the proposed transceiver, using a 65 nm CMOS process. The transmitter consists of a 4-stage PA, differential amplifiers [7], I/Q double-balanced Gilbert-cell mixers, quadrature injection-locked oscillator(QILO), and baseband amplifiers. The receiver consists of a 4-stage LNA, differential amplifiers [7], I/Q passive mixers, QILO, and baseband amplifiers. PLL generates 19.44 GHz, 20.16 GHz, 20.88 GHz, and 21.60 GHz. QILO works as a frequency tripler with 20-GHz injection from the PLL, and QILO generates a quadrature LO signal at 58.32 GHz, 60.48 GHz, 62.64 GHz and 64.80 GHz.

The calibration targets are *the free-running frequencies of Tx and Rx QILOs*, *LO leakage*, and *I/Q gain/phase mismatch* in this work. The locking range of QILO is limited and also related to I/Q phase mismatch. For improving the quadrature accuracy, the free-running frequency of QILO should be close to the locked frequency. Thus, a three-step look-back calibration using Rx down-conversion path is proposed to observe the free-running frequency indirectly without any additional frequency dividers. It consists of (1) coarse Rx QILO frequency (2) Tx QILO frequency, and (3) Rx QILO frequency. Firstly, Rx QILO is coarsely calibrated so that the Rx frequency f_{Rx} is locked to three

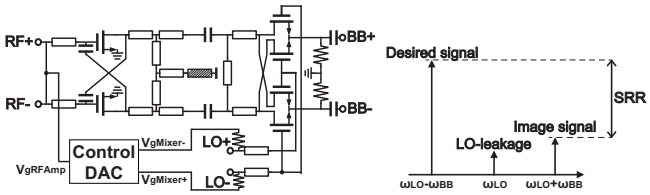


(a) QILO calibration circuit. (b) Rx QILO calibration (coarse).



(c) Tx QILO calibration. (d) Rx QILO calibration.

Fig. 2. Proposed QILO calibration.



(a) Down-conversion mixer with control DACs. (b) LO leakage and image calibration.

Fig. 3. I/Q mismatch calibration.

times of the PLL frequency f_{PLL}. For example, in case of channel 2, f_{PLL} is 20.16 GHz, and f_{Rx} can be locked at 60.48 GHz if the free-running frequency is roughly close to it. For the coarse calibration, SW1 and SW2 are turned on, and SW3 is turned off as shown in Fig. 2(a). The Tx is controlled to generate a strong LO leakage. The free-running frequency of Rx QILO is swept by the internal 10-bit control DAC as shown in Fig. 2(b). The loop-backed and down-converted LO leakage can be detected as a CW tone at $|f_{\mathrm{Tx}} - f_{\mathrm{Rx}}|$ by using an I-path ADC shown in Fig. 2(a). The locked state can be known as shown in Fig. 2(b), while the Tx frequency f_{Tx} is unknown this time. Next, the free-running frequency of Tx QILO is also swept by the internal 10-bit control DAC as shown in Fig. 2(c). In this case, the Tx QILO is not injection-locked, so the point where f_{Tx}=f_{Rx}=$3f_{\mathrm{PLL}}$ can be found. Then, SW2 is turned off, and SW3 is turned on. As shown in Fig. 2(d), the free-running frequency of Rx QILO is also swept for a fine calibration.

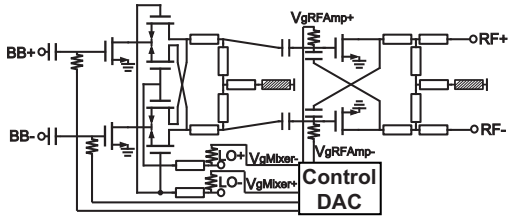
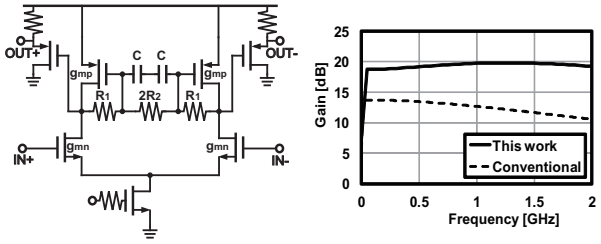
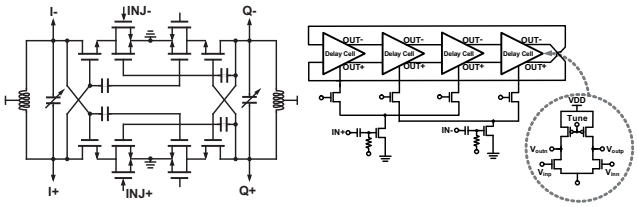


Fig. 4. Up-conversion mixer.



(a) Schematic. (b) Simulated gain.

Fig. 5. Gain peaking amplifier in Rx baseband.



(a) Schematic of QILO. (b) Divide-by-4 ILFD.

Fig. 6. QILO and divide-by-4 ILFD.

The LO leakage and I/Q mismatch are also calibrated by the loop-back method in order of (4) Tx LO leakage (5) Tx I/Q gain mismatch (6) Tx I/Q phase mismatch (7) Rx I/Q gain mismatch, and (8) Rx I/Q phase mismatch. The LO leakage is calibrated by $V_{\mathrm{gMixer+}}$ and $V_{\mathrm{gMixer-}}$ as shown in Fig. 3(a). The I/Q gain mismatch of Tx path is detected by the I-path ADC with an I-or-Q 10MHz CW tone, and is calibrated by I-side and Q-side of V_{gRFAmp}. The Tx I/Q phase mismatch is detected as the sideband rejection ratio (SRR) as shown in Fig. 3(b), and is calibrated by QILO. After the Tx calibration, Rx I/Q mismatch is detected with 10MHz-offset single-side tone from Tx, then calibrated by V_{gRFAmp} on Rx path and Rx QILO. In this case, SW1 is not implemented on a chip, and for every calibration the on-chip control DACs are controlled through a laptop PC.

III. Other Building Blocks

Fig. 4 shows the up-conversion mixer and differential amplifier using the capacitive cross-coupling neutralization, and LO leakage and gain mismatch are calibrated by the control DACs. LNA and PA are implemented by 4-stage common-source amplifiers with transmission-line-based matching blocks [7]. The gain flatness is one

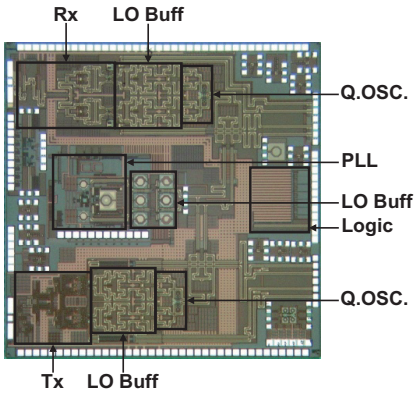


Fig. 7. Die micrograph.

of the most important design considerations because it detoriorates the EVM performance especially for this kind of open-loop wide-bandwidth system. Fig. 5 (a) shows the Rx baseband amplifier using a gain peaking technique, and the gain is derived as follows.

$$A_v = g_{\mathrm{mn}} \frac{R_1 + R_2}{1 + g_{\mathrm{mp}} R_2} \cdot \frac{1 + j\frac{\omega}{\omega_z}}{1 + j\frac{\omega}{\omega_\mathrm{p}}} \tag{1}$$

where $\omega_\mathrm{z} = \frac{R_1+R_2}{CR_1R_2}$, $\omega_\mathrm{p} = \frac{1+g_{\mathrm{mp}}R_2}{CR_2}$. The peaking frequency can be controlled by R_1, R_2 and C. Fig. 5(b) shows the simulated gain of the baseband amplifier.

Fig. 6(a) shows the detail schematics of QILO [7]. For saving the power consumption, a divide-by-4 injection-locked frequency divider (ILFD) is employed instead of power-consuming CML divider for 20 GHz-to-5 GHz division. Fig. 6(b) shows the schematic of ILFD, which realizes a wide locking range by using the progressive mixing [10].

IV. Experimental Results

Fig. 7 shows a die photo of the chip using a standard 65 nm CMOS process. The chip size is 4.2 mm × 4.2 mm. The 6-dBi antenna built in a package is used [7]. The transmitter and receiver including the PLL consume 351 mW and 238 mW from a 1.2 V supply, respectively.

Fig. 8 shows the measurement setup for the modulation performance. Two identical test boards are used. In Fig. 8, the left side is used as a transmitter, and the right side is used as a receiver. The arbitrary waveform generator (Agilent AWG M8190A) is used to generate a modulated signal, and the digital oscilloscope (Agilent DSA91304A) is used to evaluate the constellation.

Fig. 9 shows the measured Rx and Tx conversion gain, and the conversion gain achieves good flatness, suppressed under 1 dB for every channel, due to the gain peaking technique. Table I summarizes the measured Tx, Rx, and LO performances.

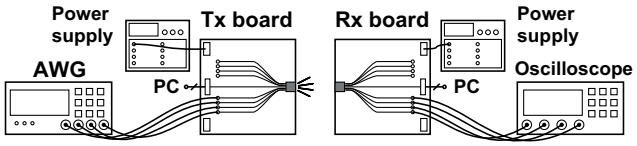
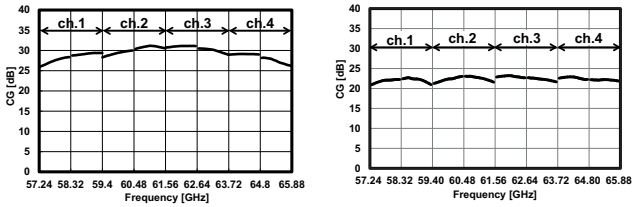


Fig. 8. Measurement setup.



(a) Rx conversion gain. (b) Tx conversion gain.

Fig. 9. Measured conversion gain of Tx/Rx.

TABLE I
Performance Summary of Tx, Rx, and LO.

Tx	
CG	30dB
OP1dB	4.4dBm (Ch. 2)
Psat	9.4dBm (Ch. 2)
Rx	
CG	24dB
NF	< 6.1dB (Ch. 1-4)
IIP3	> -23dBm (Ch. 1-4)
LO	
Inection PLL	19.44, 20.16, 20.88, 21.60GHz
Ref. spur	< -58dBc@20.16GHz
Locking range	0.63-2.04GHz
QILO	58.0-64.7GHz (free-run)
Phase noise@1MHz-offset	< -95dBc/Hz (Ch. 1-4)

TABLE II
Measurement Summary for 16QAM of RF front-end.

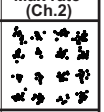
Channel	Ch.1	Ch.2	Ch.3	Ch.4	Max rate (Ch.2)
Constellation					
Spectrum					
Back-off	10 dB	8.4 dB	8.3 dB	5.7 dB	4.2 dB
Date rate	7.0Gb/s	7.0Gb/s	7.0Gb/s	7.0Gb/s	20.0Gb/s
SNR	23.7 dB	22.6 dB	22.5 dB	20.7 dB	17.6 dB
EVM	-26.2 dB	-25.2 dB	-25.2 dB	-23.4 dB	-20.2 dB

Table II shows the measurement results for 16QAM, showing the constellation, spectrum, back-off, RF data rate, SNR and EVM. The symbol rate is 1.76 Gs/s with a roll-off factor of 25 %, and the RF data rate with 2.16-GHz bandwidth are 7.04 Gb/s in 16QAM. The constellation is measured through both Tx and Rx, and the best Tx-to-Rx EVM of −26.2 dB is achieved. The maximum data rate measured with wider bandwidth and 25-% roll-off is

TABLE III
PERFORMANCE COMPARISON.

	RF data rate (modulation)	EVM (channels)	Integration	Digital cal.	Power consumption
Tokyo Tech[6]	11Gb/s (16QAM) 16Gb/s (16QAM)[9]	EVM < -17dB (Ch. 1-2)	Tx, Rx, LO, BGA package with antennas	N/A	252mW (Tx) 172mW (Rx)
Tokyo Tech[7]	11 Gb/s (16QAM)	EVM < -23dB (Ch. 1-4)	Tx, Rx, LO, BGA package with antenna	N/A	319mW (Tx) 223mW (Rx)
Toshiba[4]	2.62 Gb/s (QPSK)	N/A (Ch. 2 only)	Tx, Rx, LO, BGA package with antenna	N/A	160mW (Tx mode) 233mW (Rx mode)
SiBeam[2]	7.14 Gb/s (16QAM)	EVM < -19dB (Ch. 2-3)	Tx, Rx, LO for 32 antennas	N/A	1820mW (Tx) 1250mW (Rx)
IMEC[8]	7 Gb/s(16QAM)	EVM < -17dB (Ch. 1-4)	Tx, Rx, w/o PLL	N/A	167mW (Tx) 112mW (Rx)
This work	**20 Gb/s (16QAM)**	EVM < -25dB (Ch. 1-3) EVM < -23dB (Ch. 4)	Tx, Rx, LO, BGA package with antenna	Yes	351mW (Tx) 238mW (Rx)

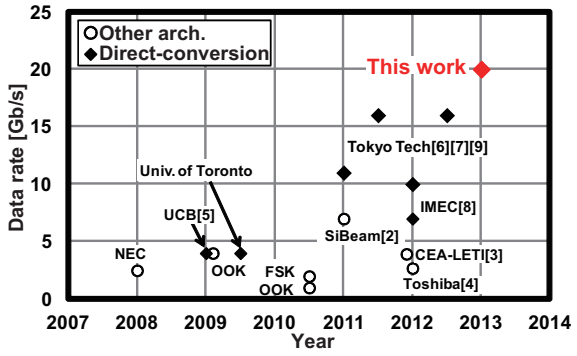


Fig. 10. Performance comparison.

20 Gb/s within a BER of 10^{-3}, which is limited by the maximum symbol rate of AWG.

Table III shows a performance comparison with the state-of-the-arts 60-GHz transceivers. The proposed transceiver integrates Tx, Rx, and LO including PLL, and is evaluated with the embedded antennas. This front-end covers all four channels of IEEE 802.11ad standard and achieves the highest data rate.

V. CONCLUSION

This paper presents a 60-GHz direct-conversion transceiver using the digital I/Q mismatch calibration. The transceiver realizes the maximum data rate of 20 Gb/s in 16QAM, which is the highest data rate among 60 GHz wireless transceivers. The transmitter and receiver consume 351 mW and 238 mW, respectively.

ACKNOWLEDGMENT

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