A 60 GHz up-conversion mixer using asymmetric layout with -41.1 dBc LO leakage

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***Abstract*— This paper presents a 60 GHz up-conversion mixer using asymmetric layout method. The asymmetric layout method contributes to decrease capacitor mismatch, so RF-LO isolation and LO leakage can be improved. The up-conversion mixer is fabricated in a 65 nm CMOS process. This up-conversion mixer achieves RF-LO isolation of -37.3 dBc, LO leakage of -41.1 dBc, conversion gain of 4.3 dB, output power of -8.7 dBm and saturated output power of -5.2 dBm at a power consumption of 5.4 mW.**

I. Introduction

Recently, wireless communications using 60 GHz ISM frequency band are actively studied. In the 60 GHz band, wide bandwidth can be used without license in many countries. Utilizing such wide bandwidth, high-speed wireless communications can be realized. Moreover, for the scaling of CMOS technology, the operating frequency of transistor increases. So, for 60 GHz transceiver, not only compound semiconductors but also CMOS can be used. By utilizing CMOS process, we can design low cost, small area and low power transceiver.

However, in 60 GHz band, it is difficult to take into account parasitics. Because parasitics have a large effect, it is difficult to identify simulation results with mesurement results. Highly precise amplifier design is realized by highly precise de-embedding method [1][2]. However, it is not enough for mixer design. This paper presents mixer layout method to decrease parasitic effects. Moreover, The difference between measurement and simulation results of designed mixer is analyzed.

In this paper, section II introduces 60 GHz CMOS RF transceiver developped by our research group. Section III desicribes L-2L de-embedding method to realize more precise mesurement results. Section IV desicribes asymmetric mixer layout. Section V desicribes mesurement results and section VI gives conclusion.

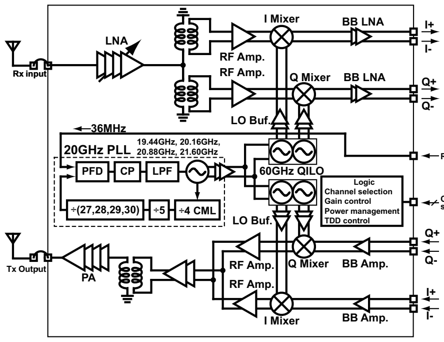

Fig. 1. The Block diagram of the 60 GHz transceiver [3][4].

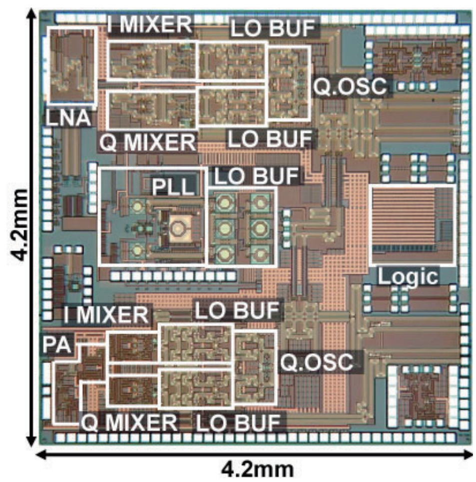

Fig. 2. The microphotograph of the 60 GHz transceiver [3][4].

II. A Full four-channel 60 GHz CMOS transceiver

The authors have reported digital assisted 60 GHz CMOS transceiver[3][4]. The transceiver employs a direct-conversion architecture in terms of power and chip area. Fig. 1 shows the block diagram of the transceiver, and Fig. 2 shows the microphotograph of the transceiver. The receiver consists of a 4-stage LNA, I/Q passive mixers and a quadrature injection-locked ocsillator (QILO). The transmitter consists of a 4-stage PA, I/Q active mixers and QILO. The 60 GHz QILO works as a frequency tripler with an integrated 20 GHz PLL. Low phase noise is achieved by the use of injection-locked oscillator. Moreover, the control logic is capable of channel selection, gain control, power managment and TDD control. 16QAM wireless communication is realized in full 4 channels based on IEEE 802.15.3c standard. Fig. 3 shows the spectrums and consterllations in 16QAM and performance summary. By utilizing wider bandwidth, the maximum data rates in QPSK and 16QAM are 8 Gbps and 10 Gbps, respectively.

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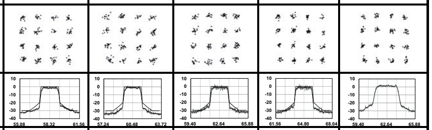

Channel	ch. 1	ch. 2	ch. 3	ch. 4	Max rate
Constellation					
Spectrum					
Back-off	4.4 dB	4.6 dB	5.0 dB	5.7 dB	5.0 dB (ch.3)
Data rate	7.0 Gb/s	7.0 Gb/s	7.0 Gb/s	7.0 Gb/s	10.0 Gb/s (ch.3)
EVM	-23.0 dB	-23.0 dB	-23.3 dB	-22.8 dB	-23.0 dB (ch.3)
SNR	20.4 dB	20.5 dB	20.7 dB	20.3 dB	20.4 dB (ch.3)

Tx	
CG	18dB
P_{sat}	5.6dBm
P_{DC}	257mW

Rx	
CG	23dB (high-gain mode) 9dB (low-gain mode)
NF	<4.9dB (high-gain mode)
IIP3	-14dBm
P_{DC}	161mW

LO	
Frequency	58.0-64.7GHz (free-run)
Phase Noise through Tx @60.48GHz	-95dBc/Hz @1MHz-offset
Ref. spur	<-58dBc
P_{DC}	61mW

Fig. 3. The performance summary [3][4].

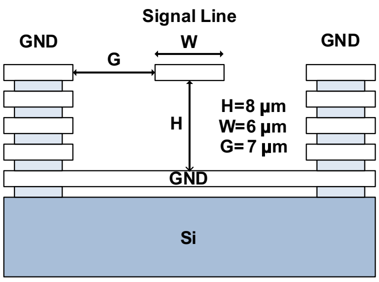

Fig. 4. The structure of transmission line.

III. L-2L DE-EMBEDDING METHOD

It is not easy to de-embed only the characteristic of DUT in 60 GHz because PADs and lead lines have large influence on the measurement results. In this paper, transmission line is used as lead lines as shown in Fig. 4. The matching blocks with small area is designed using this transmission line [5]. L-2L de-embedding method is used to get accurate characteristics of DUT [2][6]. Fig. 5 shows the modeling results of the transmission line. Attenuation constant α, phase constant β, quality factor Q and characteristic impedance Z_0 are used to identify measurement results with transmission line model. The modeling results agree with the measurement results.

IV. ASYMMTERIC UP-CONVERSION MIXER

Fig. 6 shows a circuit schematic of up-conversion mixer. The mixer employs a Gilbert-cell architecture since RF-LO isolation and LO leakage are small. By utilizing this architecture, 60 GHz leakage due to parasitic capacitor between gate and drain is cancelled. However, it is difficult to layout this architecture because RF-LO isolation and LO leakage is lager due to capacitor mismatch of layout. Fig. 7 shows layouts of mixer core parts. Fig. 7(a) is a mixer core used in the previous transceiver design [7]. Although this mixer core is symetric, the matching block needs crossing parts in both RF and LO paths as shown in Fig. 8(a). Because the capacitor between this crossing parts is large, RF-LO isolation and LO leakage is large. Moreover, it is difficult to characterize this crossing parts. On the other hand, by layouting an asymmetric mixer core as shown in Fig. 7(b), capacitor mismatch is smaller [4]. Because there is no crossing parts as shown in Fig. 8(b)

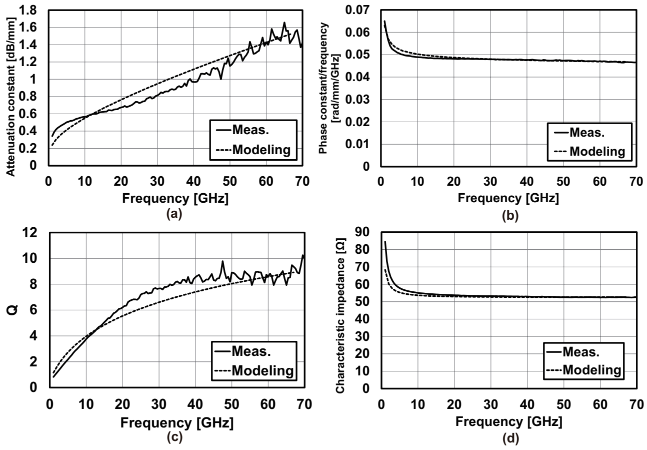

Fig. 5. The modeling results. (a)Attenuation constant (b)Phase constant/frequency (c) Q (d)Characteristic impedance.

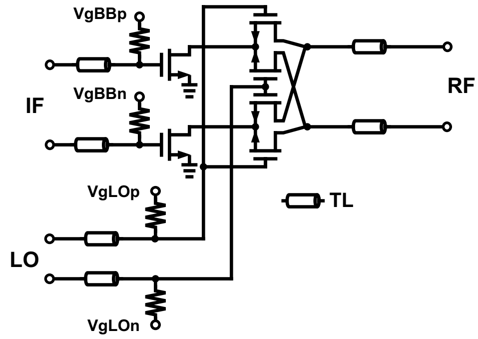

Fig. 6. The schematic of up-conversion mixer.

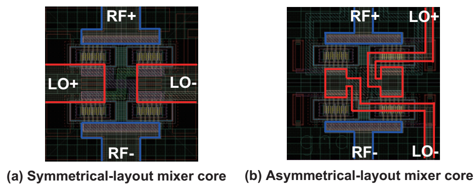

Fig. 7. The mixer core layouts [3][4].

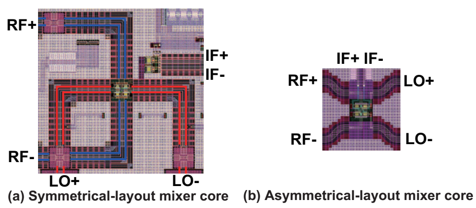

Fig. 8. The mixer layouts including matching blocks [3][4].

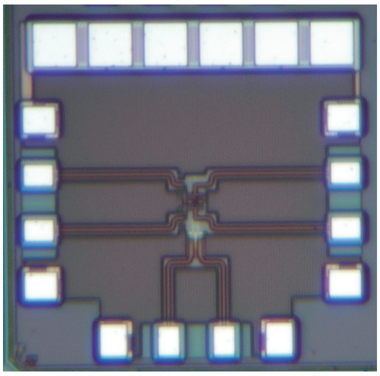

Fig. 9. The microphotograph of an asymmetric mixer.

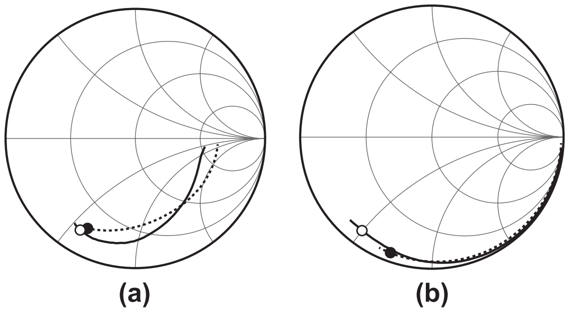

Fig. 10. The simth chart. (a)RF port (b)LO port

V. MESUREMENT RESULTS

Fig. 9 shows the microphotograph of the asymmetric mixer. The chip area is $630\,\mu\text{m} \times 630\,\mu\text{m}$. The area of mixer core is $160\,\mu\text{m} \times 50\,\mu\text{m}$. The impedance of RF and LO port and RF-LO isolation are measured using a network analyzer. Fig. 10 shows the simth charts of RF and LO port. Markers shows 60 GHz point. The measurement results are different from simulation results. This difference is due to parasitic inductance. Fig. 11 shows RF-LO isolation. By utilizing asymmetric layout, a RF-LO of $-37.3\,\text{dBc}$ isolation is achieved at 60 GHz.

Conversion gain and large-signal characteristic are measured by a measurement system as shown in Fig. 12. BB and LO signal are generated by signal generaters. RF signal is down-converted by a mixer and observed by using a spectrum analyzer. The measurement results are compared with simulation results using models. Fig. 13 shows conversion gain with respect to LO power. BB and LO frequency is 100 MHz and 62.64 GHz, respectively. LO frequency is based on IEEE802.15.3c standard. The measurement results are in good agreement with simulation results because parasitic capacitors have little influence on mixer switching operation. The difference between the impedance of simluation and that of measurement is too small to influence on conversion gain. The up-conversion mixer is precisely designed owing to the short wire line of mixer core as shown in Fig. 8(b). Fig. 14 shows large-signal charasteristic. When LO power is $5\,\text{dBm}$, the measured conversion gain, measured output power at $1\,\text{dB}$ compression point and measured saturated output power are $4.3\,\text{dB}$, $-8.7\,\text{dBm}$ and $-5.2\,\text{dBm}$, respectively. The measured power consumption is $5.4\,\text{mW}$.

Fig. 15 shows LO leakage when V_{gBB} on one side in Fig. 6 is fixed to 0.5 V and another side is swept. The minimum LO leakage is achived $-41.8\,\text{dBc}$. The influence by DC mismatch is larger than that by capacitor mismatch. Table I summarizes the performance of the 60 GHz up-conversion mixer and shows the comprison with other 60 GHz up-conversion mixers.

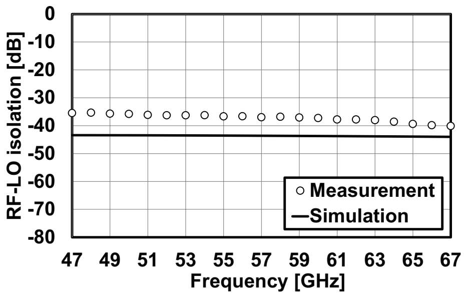

Fig. 11. RF-LO isolation.

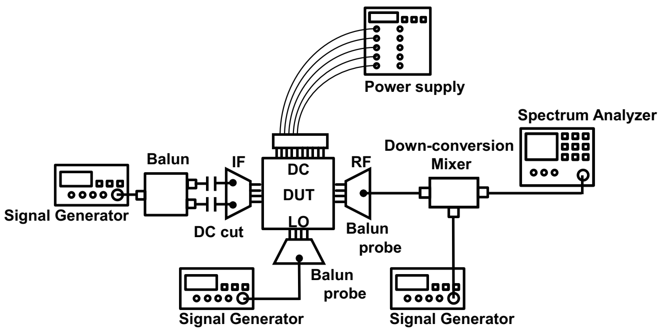

Fig. 12. The measurement system for CG and large-signal charasteristic.

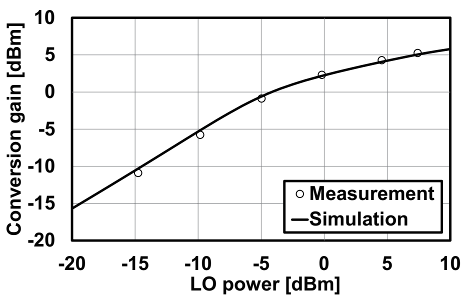

Fig. 13. Conversion gain vs LO power.

TABLE I

PERFORMANCE COMPARISON OF MILLIMETER-WAVE UP-CONVERSION MIXERS.

	Technology	Conversion Gain[dB]	P_{1dB}[dBm]	P_{sat}[dBm]	RF-LO isolation[dB]	LO leakage[dBc]	Power[mW]
[8]	130 nm	4.0	-5.6	-3	-37	-30	24.0
[9]	90 nm	4.5	NA	NA	-57.5	NA	15.1
[10]	130 nm	-5.6	-20	-15	NA	NA	2.7
This Work	65 nm	4.3	-8.7	-5.2	-37.3	-41.1	5.4

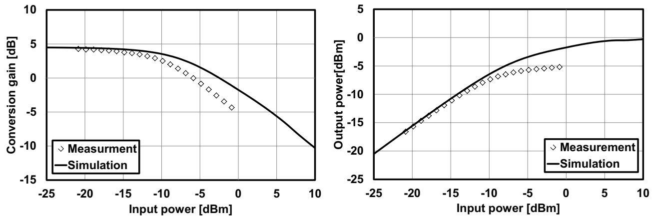

Fig. 14. Large-signal characteristic.

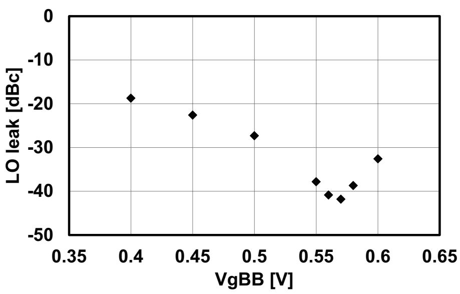

Fig. 15. LO leakage vs VgBB.

VI. CONCLUSION

This paper presents a 60 GHz up-conversion mixer using asymmetric layout method. The asymmetric layout method contributes to improve RF-LO isolation and LO leakage. Moreover, by short wire line for 60 GHz signal, parasitic inductance is small. Therefore, a precise design of up-conversion mixer in 65 nm CMOS is realized. This up-conversion mixer achieves RF-LO isolation of $-37.3\,\mathrm{dBc}$, LO leakage of $-41.1\,\mathrm{dBc}$, conversion gain of $4.3\,\mathrm{dB}$, output power of $-8.7\,\mathrm{dBm}$ and saturated output power of $-5.2\,\mathrm{dBm}$ at a power consumption of $5.4\,\mathrm{mW}$.

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