A proposal of "2R-R+ segment DAC" architecture and its design methodology

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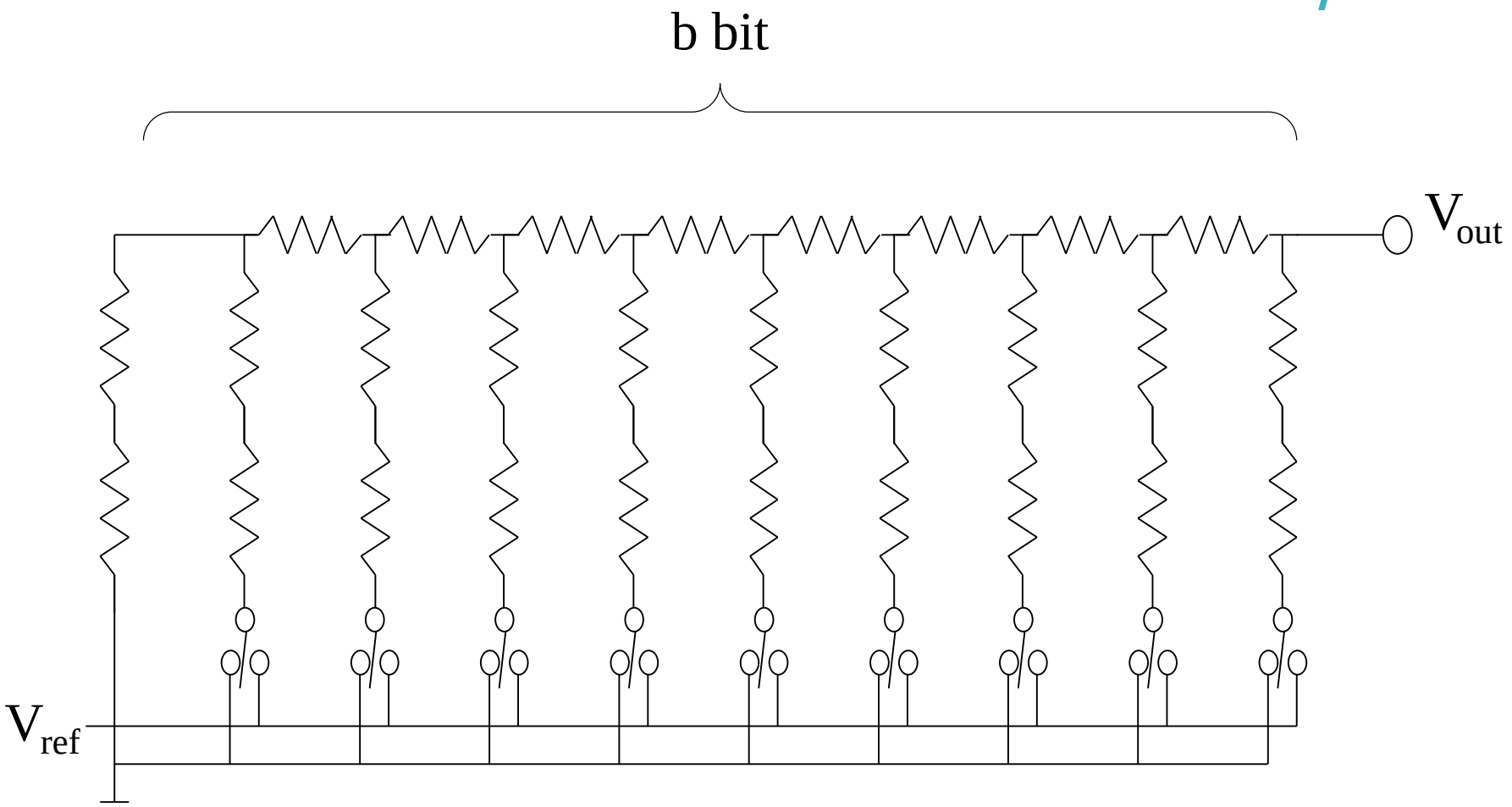
Abstract

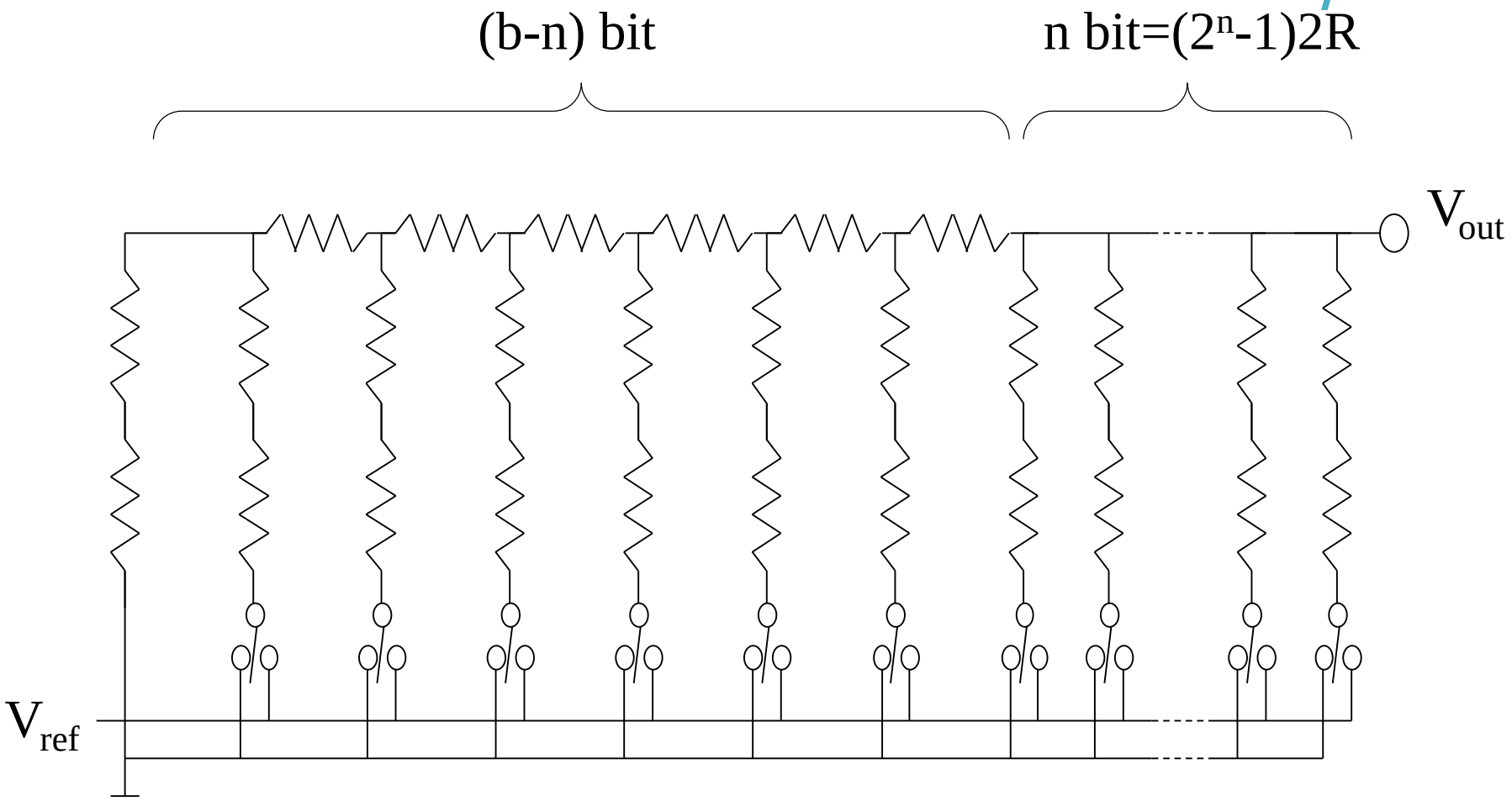
- Targeting design automation, we propose a general calculation methodology for “R-2R + segment DACs”
- We propose “2R-R + segment DAC” architecture

CBCM法を用い、0.001fF分解能、浮遊容量分離型、
400個の容量TEGマトリクス・テスト・ストラクチャの提案

R-2R DAC (previous)



R-2R DAC + segments (previous)



Previous issues

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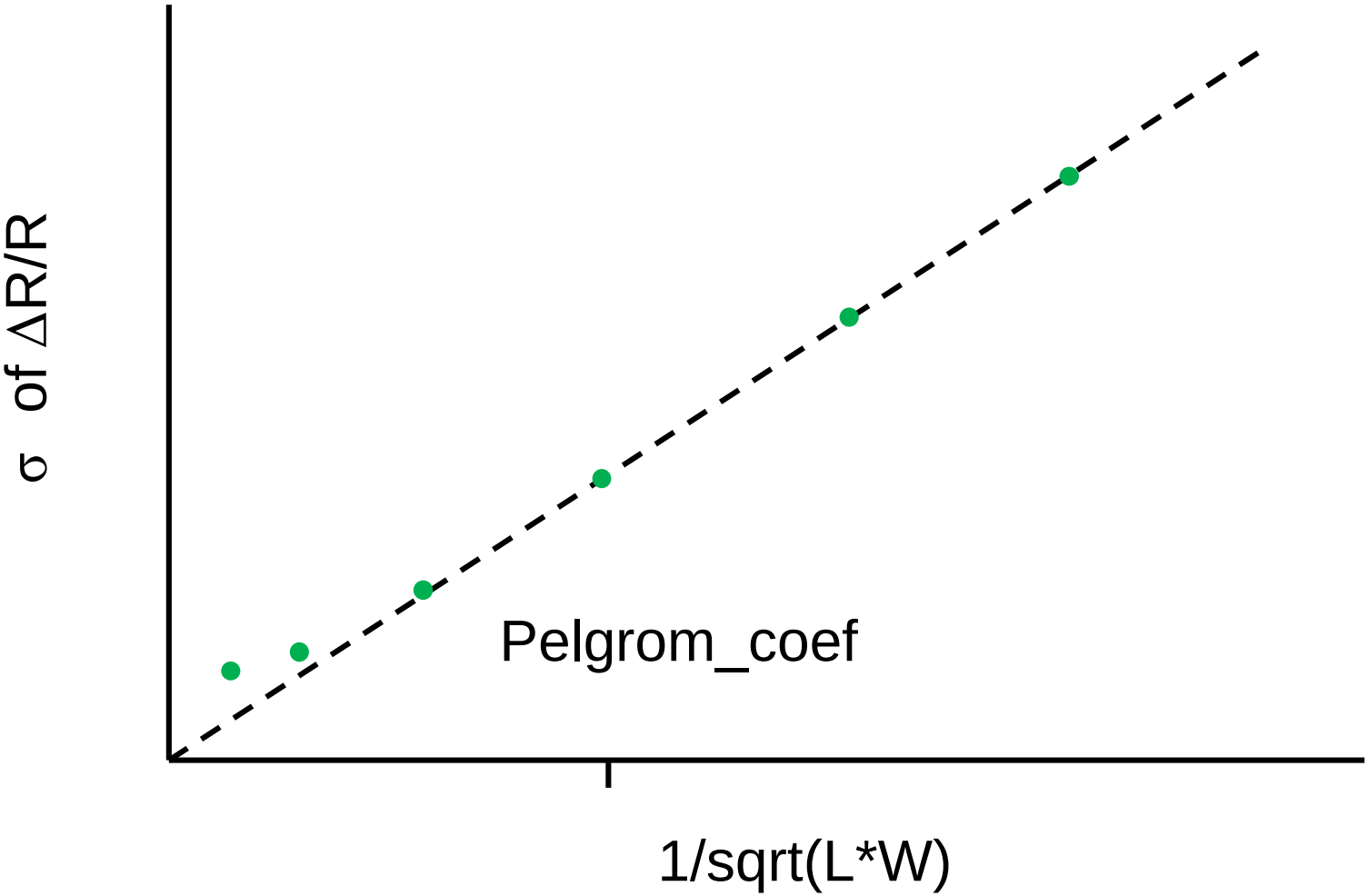
- How to select W of the unit resistor ?
- How to define n (bit of segment portion) ?

Pelgrom coefficient example



Proposed design method 1

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- A required accuracy of unit resistor is calculated as $m/2^{b-n}$, where m is margin
- Its standard deviation σ is given as $\sigma=pelgrom\_coef/sqrt(L*W)$.
  $m/2^{b-n}=k*pelgrom\_coef/sqrt(L*W)$ (1)
- $R=\rho_s(L+\Delta L)/(W+\Delta W)+2R_c$ (2)
  $R\sim\rho_s*L/W+2R_c$ (2')

Proposed design method 2

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- Where
  - b: total DAC bit (given)
    n: bit of segment portion (variable)
    R: unit resistor value (given)
  - m=1/4 (default)
    k=3 or 4 (default)
  - pelgrom_coef (from PDK)
    ρ_s (from PDK)
    ΔL (from PDK)
    ΔW (from PDK)
    R_c (from PDK)

Proposed design method 3

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- Hence,
  $W=(k^*\rho_s/m)2^{b-n}\mathrm{sqrt}(pelgrom\_coef/R)$ (3)
  If $W<W_{min}$(in PDK) then $W=W_{min}$
- $L=(R-2R_c)(W-\Delta W)/\rho_s+\Delta L$ (4)
  If $L<L_{min}$(in PDK) then $L=L_{min}$
  recalculate W

Proposed design method 4 (confidential)

- On_resistance of switch transistors is $R_{on}=1/[\beta(W_{sw}/L_{sw})(V_G-V_T)]$ per Nch,Pch
- By accuracy requirement $R_{on}=m'/2^{b-n}$, where m' is margin
- Use $L_{sw}=L_{min}$(in PDK) * analog_margin

- Considering spaces, total resistor area, total switch area & total area can be calculated as brown lines in next pages.

9bit DAC size vs n (proposed)

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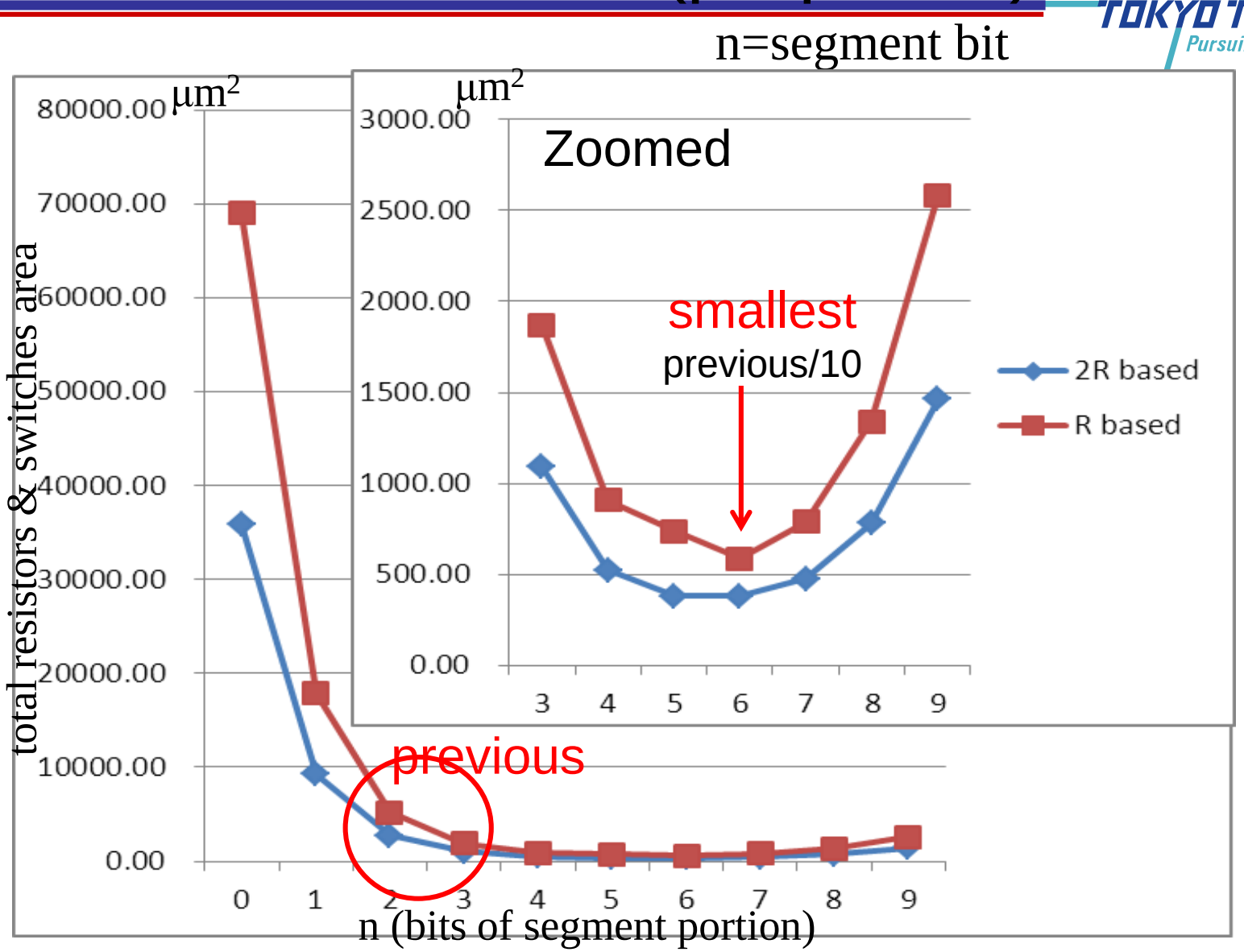

12bit DAC size vs n (proposed)

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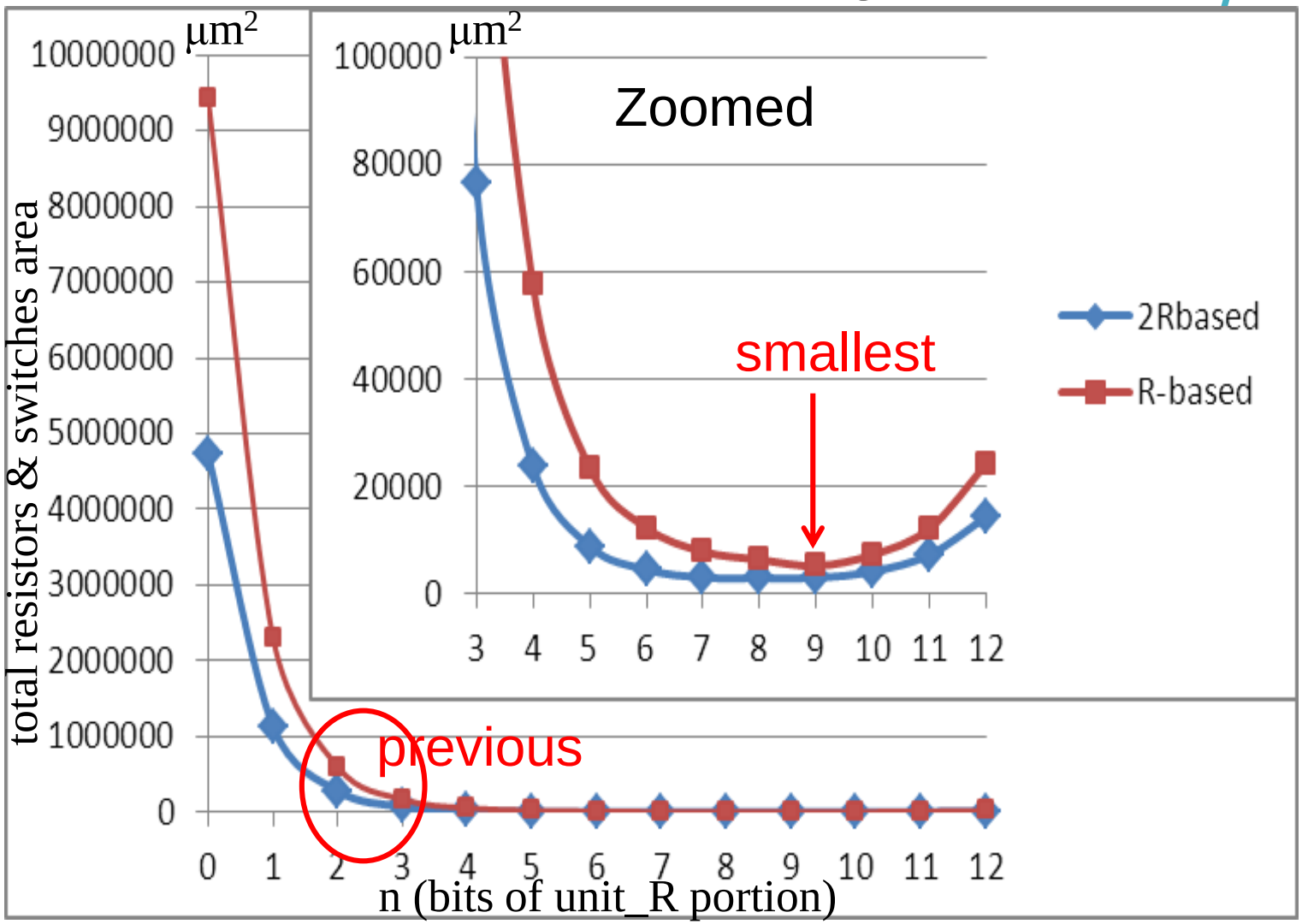
n=segment bit



Proposed 2R-R + segment DAC 1

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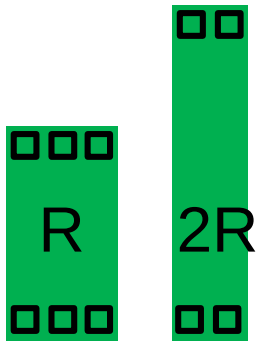
- See equation(1) again.
  $m/2^{b-n}=k*pelgrom\_coef/sqrt(L*W)$ (1)
- It means that unit resistor area L*W doesn't depend on its resistor value !
- We propose 2R as a unit resistor (2R based architecture), called "2R-R DAC" shown in next page
- Unit resistors either R or 2R are same size !
- See previous pages



Proposed 2R-R + segment DAC 2

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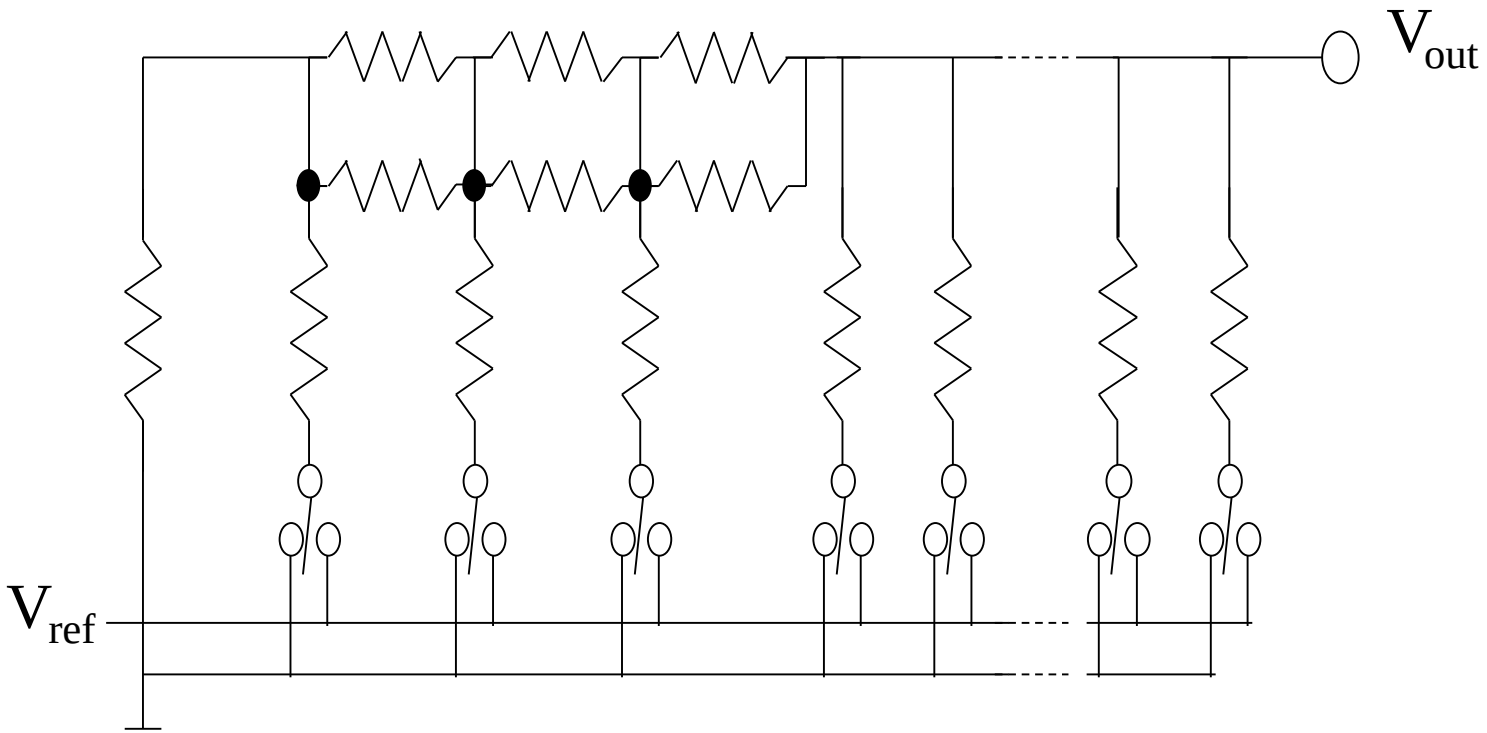
(b-n) bit
-1 than R based

n bit=(2^n-1)2R
Half number than R based



2R based

Design automation

- We wrote all equations in BASIC and C languages.
  - With given bit number, unit resistor value, the program generates unit resistor's L & W, P/N switch transistors' L & W, total area are automatically calculated par n (variable).
  - Automatically generated net list.
  - Free from process technologies. PDK table in it can be filled any processes.

Generated net list exsmple (confidential)


```
.subckt (OUT  VDD1 GND1
+DT63 DT62 DT61 DT60 DT59 DT58 DT57 DT56
+DT55 DT54 DT53 DT52 DT51 DT50 DT49 DT48
+DT47 DT46 DT45 DT44 DT43 DT42 DT41 DT40
+DT39 DT38 DT37 DT36 DT35 DT34 DT33 DT32
+DT31 DT30 DT29 DT28 DT27 DT26 DT25 DT24
+DT23 DT22 DT21 DT20 DT19 DT18 DT17 DT16
+DT15 DT14 DT13 DT12 DT11 DT10 DT9 DT8
+DT7 DT6 DT5 DT4 DT3 DT2 DT1 DT0 ) R-DAC

*thermo_meter_code part
RT63 OUT nett63    20000 L=3.19U W=0.22U
MNT63 nett63 DT63 GND1 GND1 nch L=0.12U W=0.52U M=2
MPT63 nett63 DT63 VDD1 VDD1 pch L=0.12U W=1.66U M=2
RT62 OUT nett62    20000 L=3.19U W=0.22U
MNT62 nett62 DT62 GND1 GND1 nch L=0.12U W=0.52U M=2
MPT62 nett62 DT62 VDD1 VDD1 pch L=0.12U W=1.66U M=2
    :
RT0 OUT nett0    20000 L=3.19U W=0.22U
MNT0 nett0 DT0 GND1 GND1 nch L=0.12U W=0.52U M=2
MPT0 nett0 DT0 VDD1 VDD1 pch L=0.12U W=1.66U M=2
```

```
*binary_code part
RD2 OUT OUT1    20000 L=3.19U W=0.22U
RE2 OUT OUT1    20000 L=3.19U W=0.22U
RB2 OUT netb2    20000 L=3.19U W=0.22U
MNB2 netb2 DB2 GND1 GND1
+ nch L=0.12U W=0.52U M=2
MPB2 netb2 DB2 VDD1 VDD1
+ pch L=0.12U W=1.66U M=2
RD1 OUT1 OUT0    20000 L=3.19U W=0.22U
RE1 OUT1 OUT0    20000 L=3.19U W=0.22U
RB1 OUT1 netb1    20000 L=3.19U W=0.22U
MNB1 netb1 DB1 GND1 GND1
+ nch L=0.12U W=0.52U M=2
MPB1 netb1 DB1 VDD1 VDD1
+ pch L=0.12U W=1.66U M=2
RD0 OUT0 OUTX    20000 L=3.19U W=0.22U
RE0 OUT0 OUTX    20000 L=3.19U W=0.22U
RB0 OUT0 netb0    20000 L=3.19U W=0.22U
MNB0 netb0 DB0 GND1 GND1
+ nch L=0.12U W=0.52U M=2
MPB0 netb0 DB0 VDD1 VDD1
+ pch L=0.12U W=1.66U M=2
RBX OUTX GND1    20000 L=3.19U W=0.22U
```

Conclusion

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- We proposed R-2R + segment DAC design methodology
- We have programmed it in BASIC & C
- We have found best combination of R-2R(b-n bit) and segment DAC(n bit)
  - In many cases, 3bit for R-2R is smallest
  - The size is ~1/10 of previous
- We proposed “2R-R + segment DAC”, and its area is almost half of previous.

References

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2. Xingfa Huani, et al “A poly-resistor 12-bit D/A converter”, ICSICT 2008, p.2000-2003
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4. N.C.Horta, et al “FRAMEWORK FOR ARCHITECTURE SYNTHESIS OF DATA CONVERSION SYSTEMS EMPLOYING BINARY-WEIGHTED CAPACITOR ARRAYS”, ISCAS 1991, p.1789-1792 vol.3