A proposal of “2R-R + segment DAC” architecture and its design methodology

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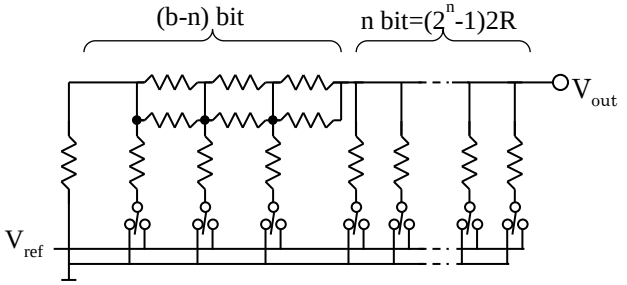
Abstract: It is well known that b bit R-DAC consisting of R-2R type for upper b-n bits and 2R segments for lower bits.

Targeting design automation, we propose a general calculation methodology for the DACs including n=0 and n=b. A required accuracy of unit resistor is calculated as $m*2^{-b+n}$, where m is margin. Its standard deviation σ is given as Pelgrom_coef/sqrt(L*W). As well known, W/L comes from given resistor value. L,W can be easily calculated from the equations.



The equation above mentions that same area value L*W for either R or 2R, due not to depend on area. Hence we propose “2R-R+segment DAC” shown in above figure, consisting of 2R as unit resistor and R as a parallel of two 2Rs. Because of bigger number of 2R than R in the figure, it is realized in almost half size of previous “R-2R+segment DAC”.