A Dual-Loop Injection-Locked PLL with All-Digital PVT Calibration System

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1. Introduction

For modern SoC systems, stringent requirements on on-chip clock generators include small-area, low-power consumption, PVT-insensitive, and the lowest possible jitter performance. Sub-harmonically injection-locked technique can significantly improve random jitter characteristic of a clock generator. To compensate the free-running frequency shift caused by temperature and voltage variations, this paper proposes the use of a dual-loop topology with one free-running VCO (Replica VCO) placed inside a FLL for tracking temperature and voltage drift. The other VCO (Main VCO) is injection-locked for producing a low-jitter clock, while the free-running frequency shift can be compensated by the replica loop.

2. Circuit Design and Implementation

Block diagram of the proposed system is given in Fig.1. Aside from the VCO and the 10-bit DAC, all circuits that makeup the FLL are implemented using digital standard cells to have a synthesizable all-digital FLL (AD-FLL) design. Therefore, the proposed work can significantly scale down in area due to the absence of a passive loop filter. The oscillation frequency of replica VCO is measured by a digital counter. This counted number is compared to a predefined frequency control word (FCW) that maps to the expected number of pulses during one cycle for a certain division ratio. Depending on the sign of the output, the 10-bit up/down counter adjusts both the main and replica VCO frequency.

After the initial frequency calibration of the replica VCO is carried out, the counter connected to the replica VCO is disabled and the multiplexer control lines are set to choose the output of the main VCO counter for calibrating frequency offset. In phase II, an offset is added or subtracted from the main VCO counter to compensate frequency difference between it and the replica VCO that might arise from process variations. By comparing the number of pulse of main VCO to the predefined value and incrementing or decrementing the main VCO counter, the required offset to calibrate any difference in frequency will be added or subtracted. Finally, as both VCOs are having the same frequency, the loop is returned to its initial settings to maintain both VCOs frequency over temperature and voltage variations for robust operation.

3. Measurement results

The proposed circuit is fabricated in a 65 nm CMOS process. The die micrograph is shown in Fig.2. The phase noise before and after injection is measured by using a signal source analyzer (Agilent E5053A) and is given in Fig.3. This phase noise maps to a 0.7 ps jitter when integrated from 10 kHz to 40 MHz. The proposed dual-loop IL-PLL has an operating range of 0.5-to-1.6 GHz, and it consumes a total power consumption of 0.97 mW excluding output buffer, from a 1 V power supply. The measured reference spur is -57 dBc. The reference clock can be varied from 40 to 300 MHz. All the above-mentioned measurements are performed at the room temperature.

4. Conclusion

This paper [1] proposes a dual-loop injection-locked PLL with synthesizable all-digital PVT calibration circuits. With careful design, the proposed PLL can be suited for clock generation in wireline and wireless systems.

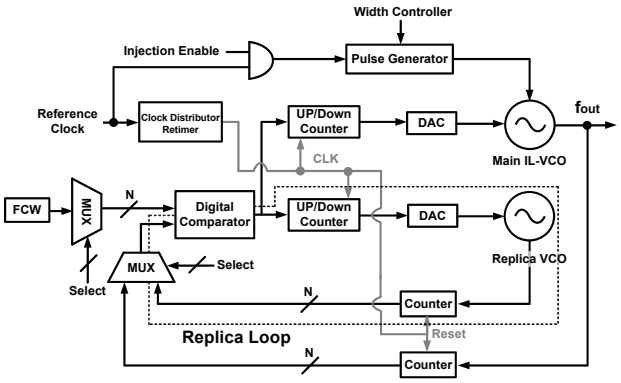

Figure 1: Block diagram of the proposed dual-loop IL-PLL with synthesizable all-digital PVT calibration circuits.

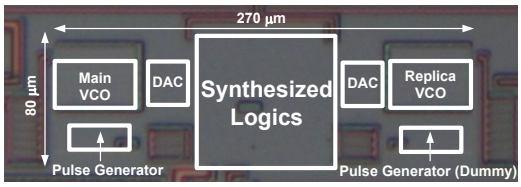

Figure 2: Chip microphotograph.

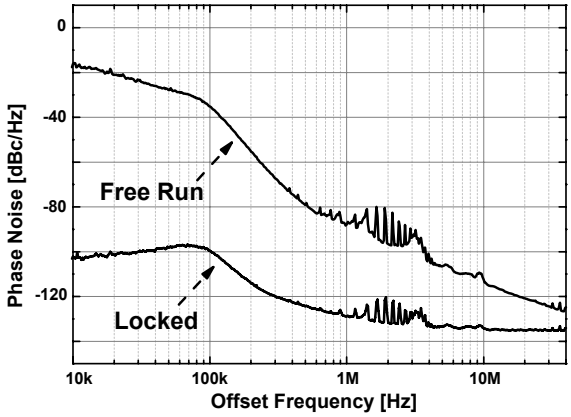

Figure 3: Measured phase noise characteristic at a carrier of 1.2 GHz

Acknowledgements

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References

[1] Wei Deng, Ahmed Musa, Teerachot Siriburanon, Masaya Miyahara, Kenichi Okada, and Akira Matsuzawa, "A 0.022 mm^2 970 µW Dual-Loop Injection-Locked PLL with -243 dB FOM Using Synthesizable All-Digital PVT Calibration Circuits,"*ISSCC Dig. Tech. Papers* , 2013.