A Scalable ADC for Green and Dependable Communications

Akira Matsuzawa

Tokyo Institute of Technology

Summary

- **Sigma-delta ADC is widely used for wireless communications, however it has a limitation.**

- **SAR ADC has attractive features for green and dependable wireless communications.**
  - **Low power**
  - **Low voltage ..0.7V**
  - **Scalable P_d for the sampling frequency**
  - **Can increase SNR by oversampling using digital filter**
  - **Can increase signal bandwidth by interleaving**
  - **Small occupied area**

- **Developed 12 bit SAR ADC using 90nm demonstrates low P_d of 2mW at 50MSps, P_d scalability with the sampling rate, and possibility of increase of SNR by over sampling.**

- **Developing 12bit SAR ADC using 65nm will realize a green and dependable ADC for wireless communication.**

Data rate is proportional to the product of f_s and N

$$D_{rate} \approx N \cdot f_s$$

If the signal bandwidth is fixed, increase of resolution is required to increase the data rate.

Shannon's theory to determine the communication capacity

$$C = BW \log_2\left(1 + \frac{P_S}{P_N}\right)$$

Higher data-rate can be realized by higher multi-level modulation. It results in increase of ADC resolution.
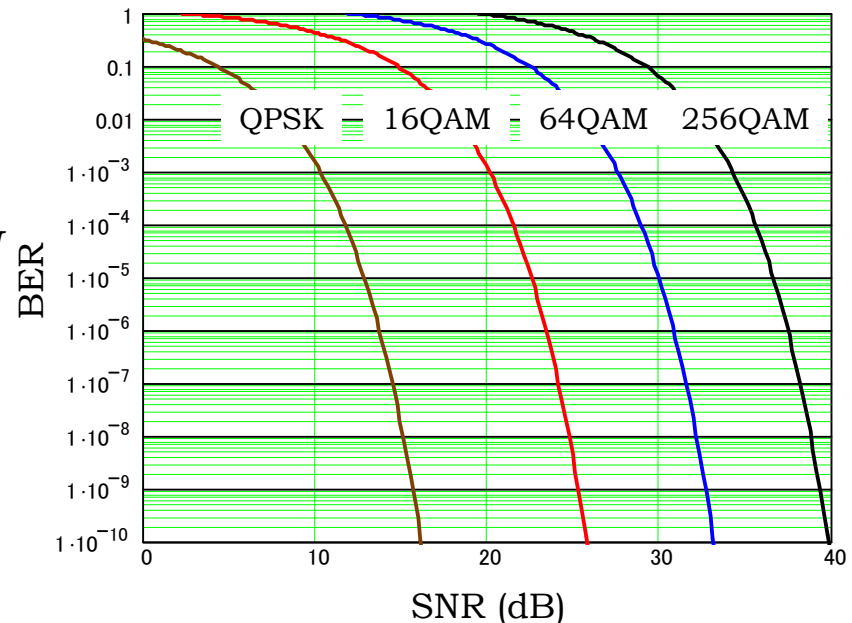
BW and SNR of ADC are

$$BW < \frac{f_s}{2} \qquad \left.\frac{P_S}{P_N}\right|_{ADC} = 1.5 \cdot 2^{2N}$$

Therefore

$$C \approx N f_s$$

f_s: Sampling frequency
N: Resolution

QPSK   16QAM   64QAM   256QAM

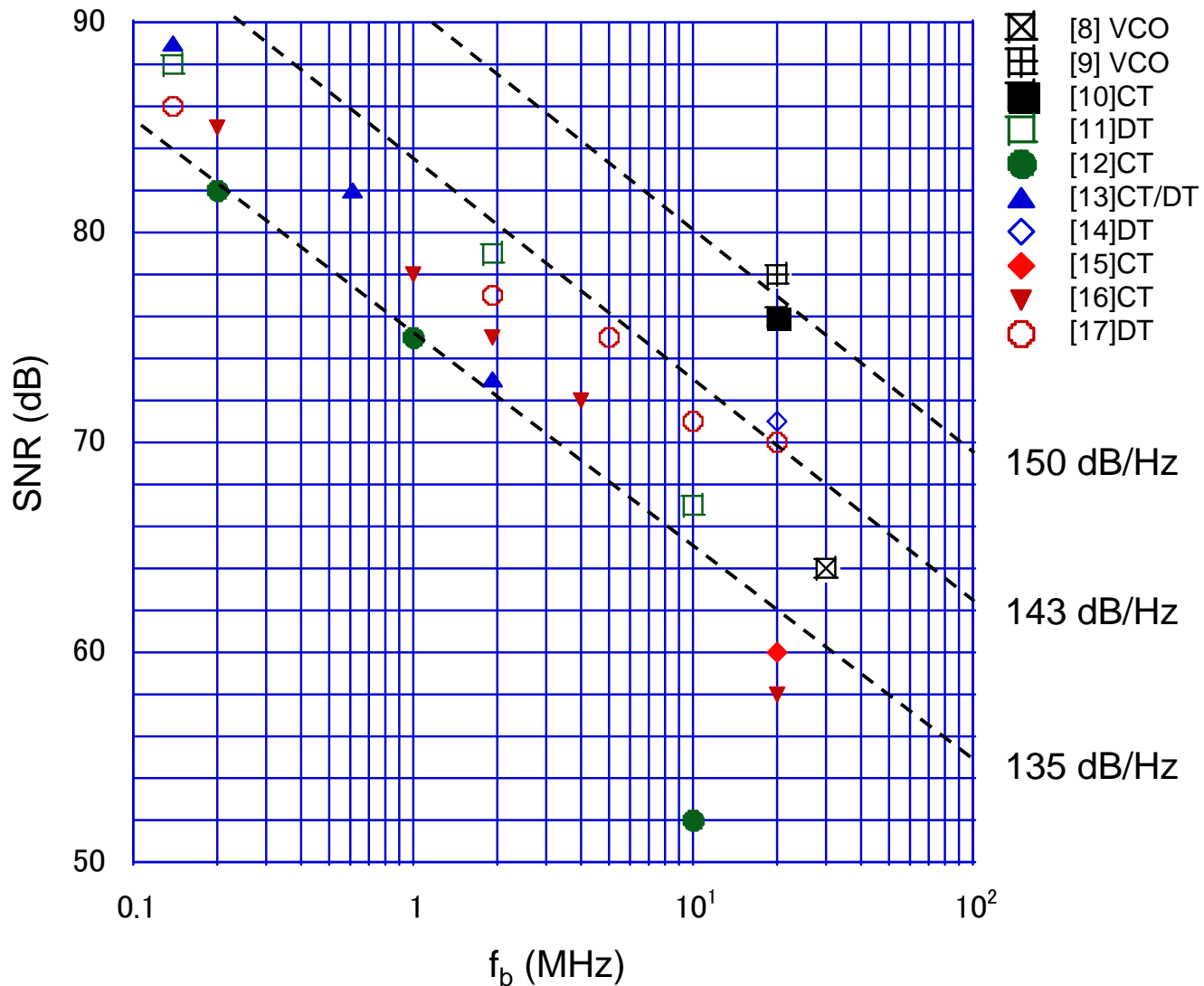BER vs SNR (dB)

SNR is inversely proportional to the signal bandwidth

SNR vs. signal bandwidth of ADCs for the wireless communications

$$SNR \approx SNR_0 - 10\log(BW)$$

Legend:
- ⊠ [8] VCO
- ⊞ [9] VCO
- ■ [10]CT
- □ [11]DT
- ● [12]CT
- ▲ [13]CT/DT
- ◇ [14]DT
- ◆ [15]CT
- ▼ [16]CT
- ○ [17]DT

SNR$_0$:SNR @1Hz

SNR$_0$:140dB

150 dB/Hz

143 dB/Hz

135 dB/Hz

P$_d$ vs. signal bandwidth

P$_d$ is proportional to the square root of the signal bandwidth

$$p_d(mW) = 8 \times \sqrt{f_b(MHz)}$$
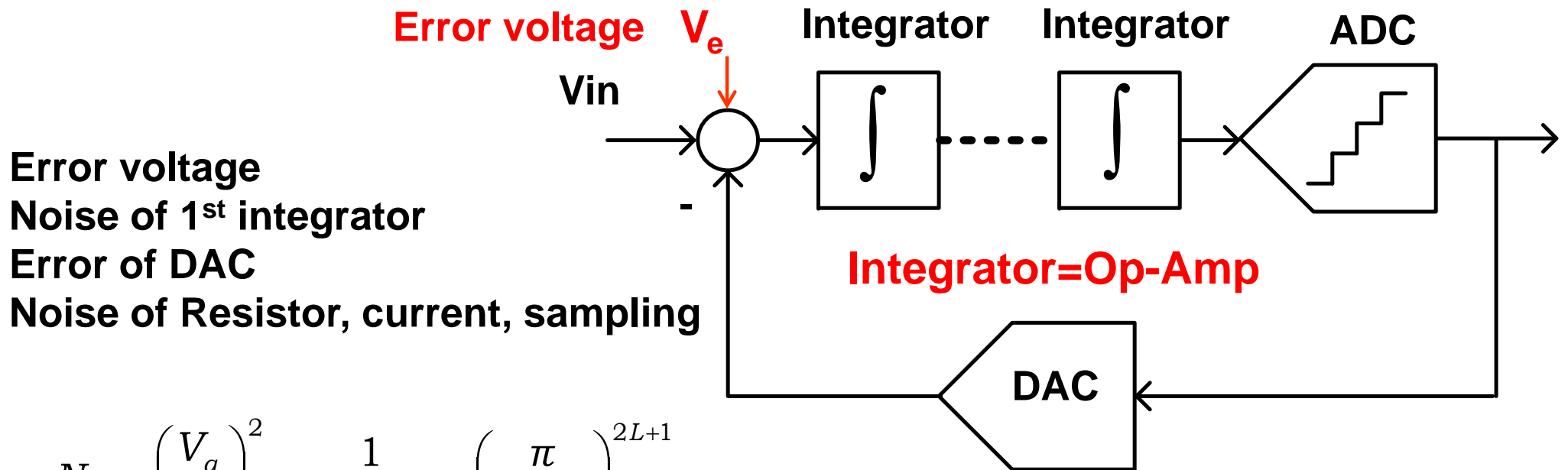
$$p_d(mW) = 2.5 \times \sqrt{f_b(MHz)}$$

Sigma-delta ADC

Sigma-delta ADCs are widely used for wireless communications. But….

Sigma delta ADC can suppress only the quantization noise of ADC.
The performance is limited by the input error voltage.
Op-Amp is needed for the integrator and consumes static power.

Error voltage V_e

Integrator   Integrator   ADC

Vin

Error voltage
Noise of 1st integrator
Error of DAC
Noise of Resistor, current, sampling

Integrator=Op-Amp

DAC

$$N_q = \left(\frac{V_q}{2}\right)^2 \frac{1}{3\pi(2L+1)}\left(\frac{\pi}{OSR}\right)^{2L+1}$$

Quantization noise can be suppressed so much

$$V_{e\_eff} \approx \frac{V_e}{OSR}$$

Error voltage at input summing node can't be suppressed
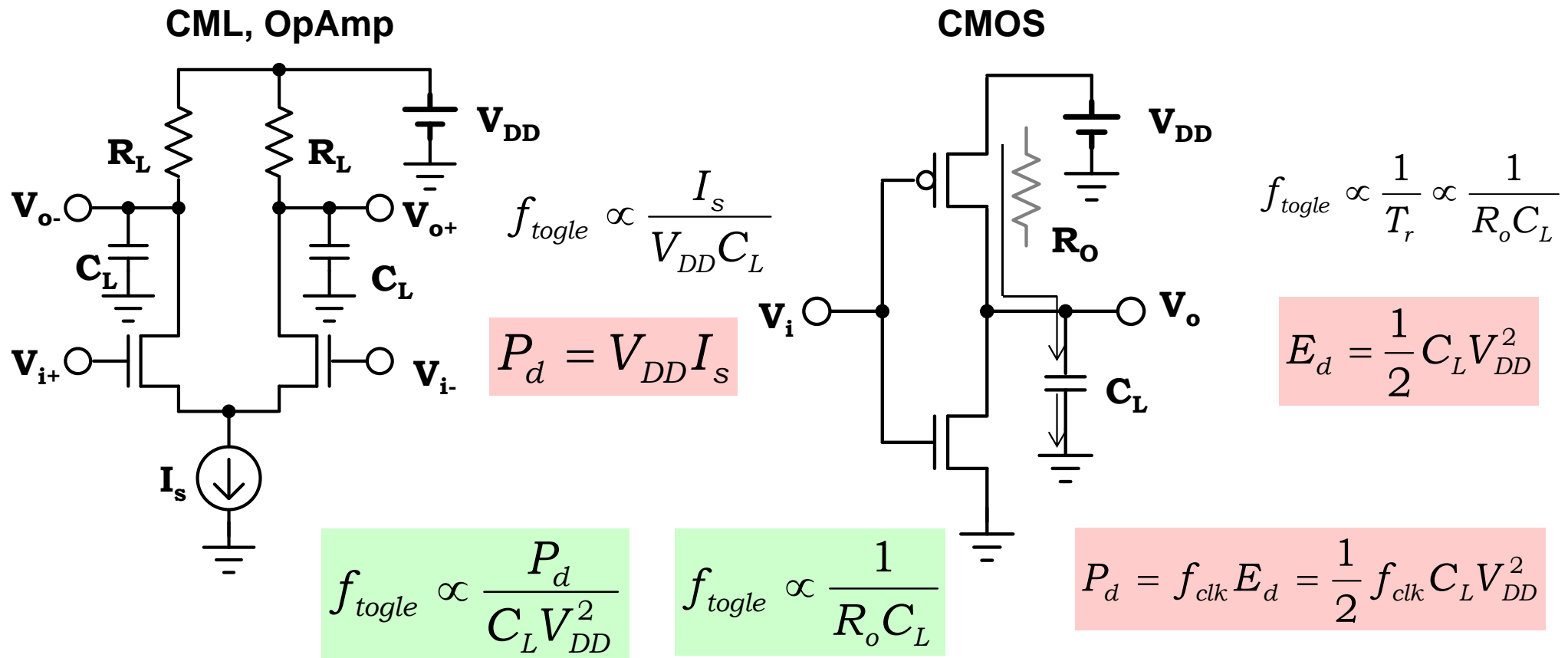**so much. Suppressed by only OSR.**

Conventional analog circuit consumes continuous current and results in larger energy consumption.   **Not scalable Pd** for operating frequency.
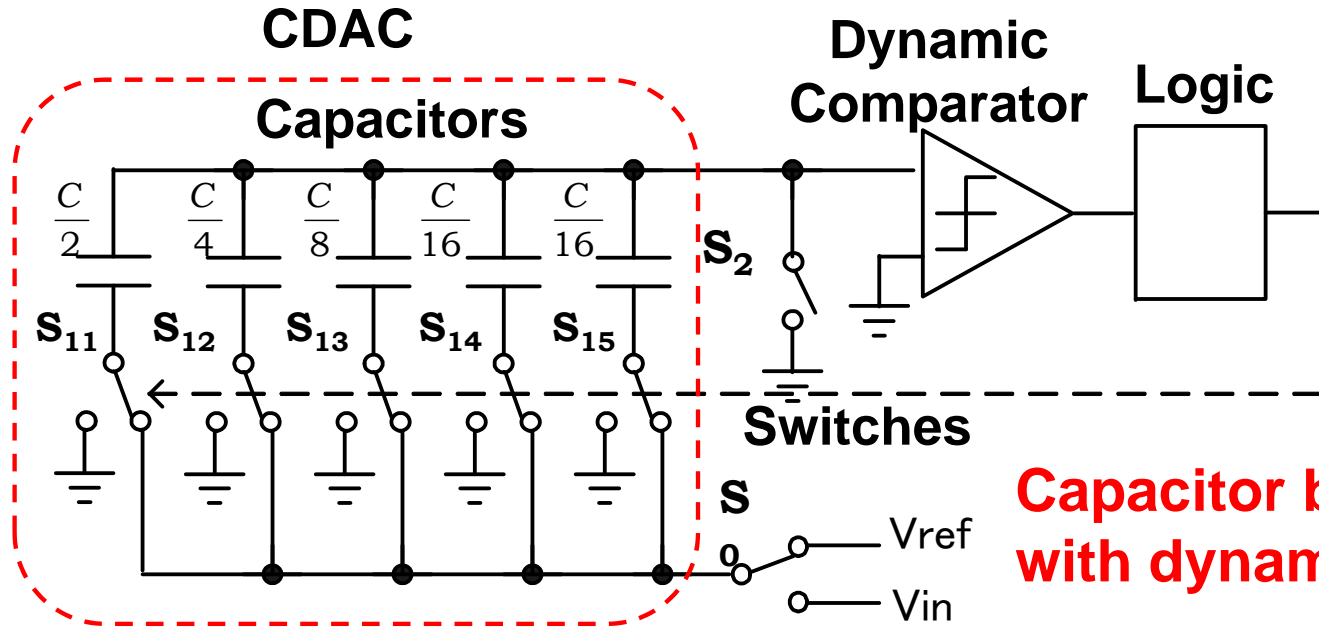
Dynamic circuits doesn't consume larger energy.

CMOS: Consumed energy is **independent** of the delay time.
**Scalable power consumption** for the operating frequency.

CML, OpAmp

CMOS

$$f_{togle} \propto \frac{I_s}{V_{DD}C_L}$$

$$P_d = V_{DD}I_s$$

$$f_{togle} \propto \frac{P_d}{C_L V_{DD}^2}$$

$$f_{togle} \propto \frac{1}{R_o C_L}$$

$$f_{togle} \propto \frac{1}{T_r} \propto \frac{1}{R_o C_L}$$

$$E_d = \frac{1}{2} C_L V_{DD}^2$$

$$P_d = f_{clk} E_d = \frac{1}{2} f_{clk} C_L V_{DD}^2$$

SAR ADC doesn't consume any static power and has no tradeoff between the speed and the energy consumption.

CDAC

Capacitors

$\dfrac{C}{2}$ $\dfrac{C}{4}$ $\dfrac{C}{8}$ $\dfrac{C}{16}$ $\dfrac{C}{16}$

S_{11} S_{12} S_{13} S_{14} S_{15}
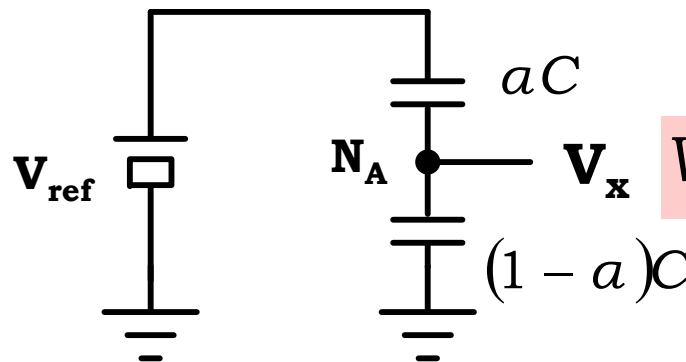
Dynamic Comparator

Logic

S_2

Switches

S

0

Vref

Vin

**No resistors
No amplifier
No static current !
Potentially full swing**

Capacitor based analog processing with dynamic comparator

Sample

V_{in} C N_A
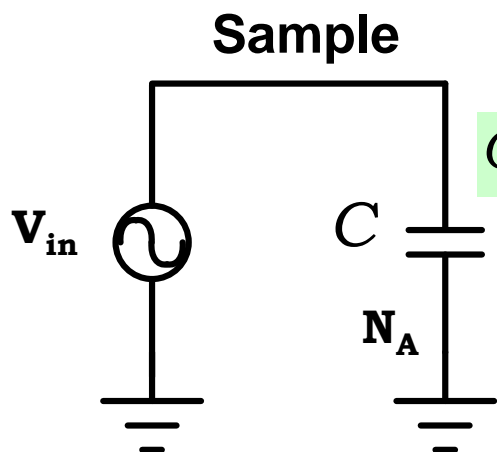
$Q = -CV_{in}$

Generating subtracted signal

aC

V_{ref} N_A V_x $(1-a)C$
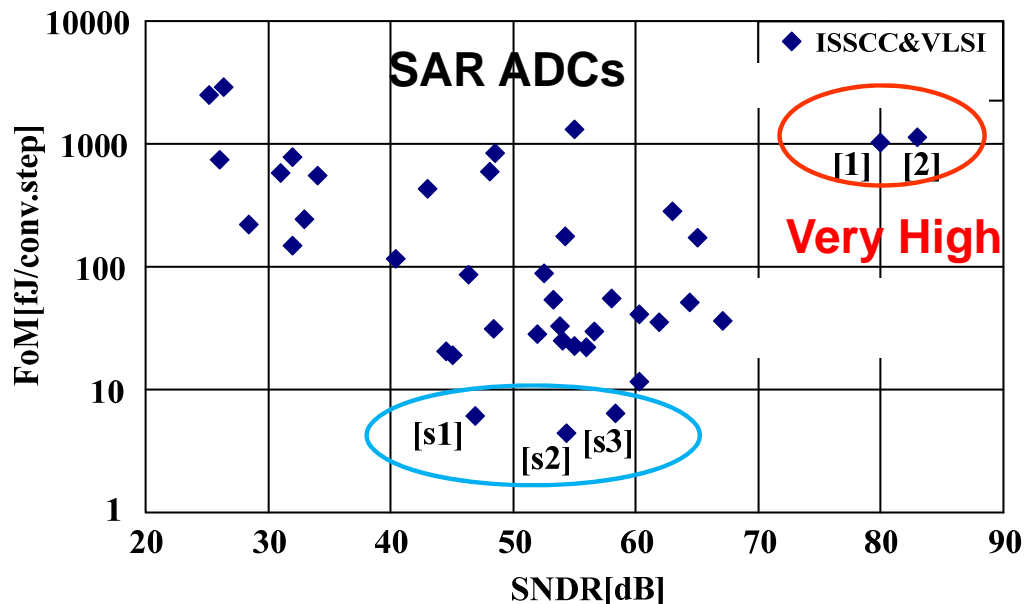
$E_d \approx \dfrac{1}{2}CV_{ref}^2$

$V_x = -\left(V_{sig} - a \cdot V_{ref}\right)$
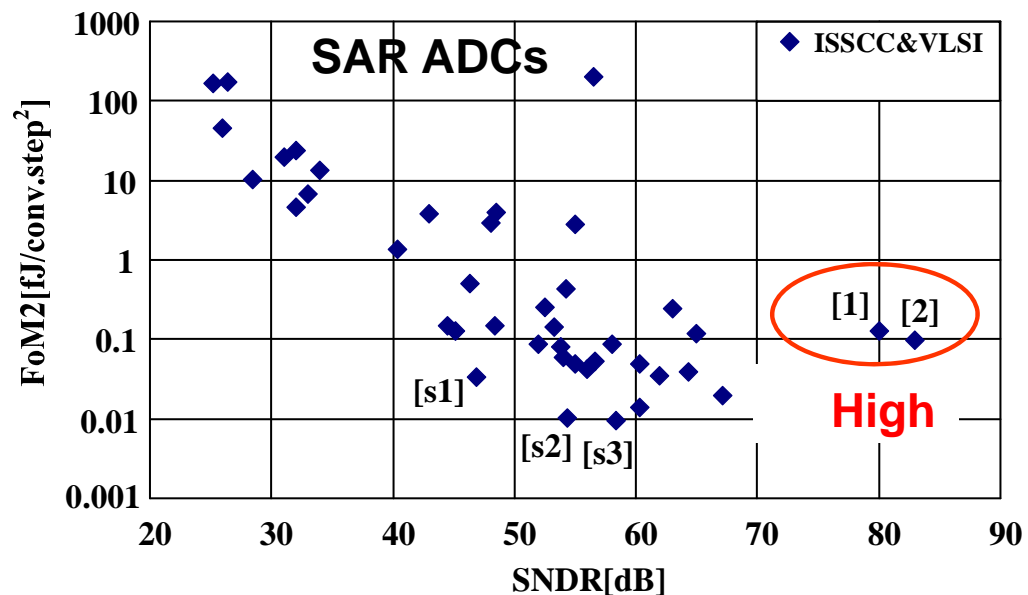
$0 < a < 1$

High SNDR over 70dB and low FoM of less than 50fJ looks not easy.

FoM LT. 10fJ is possible, however its SNDR is < 60dB

Low FoM, if SNDR is > 70dB is not easy.

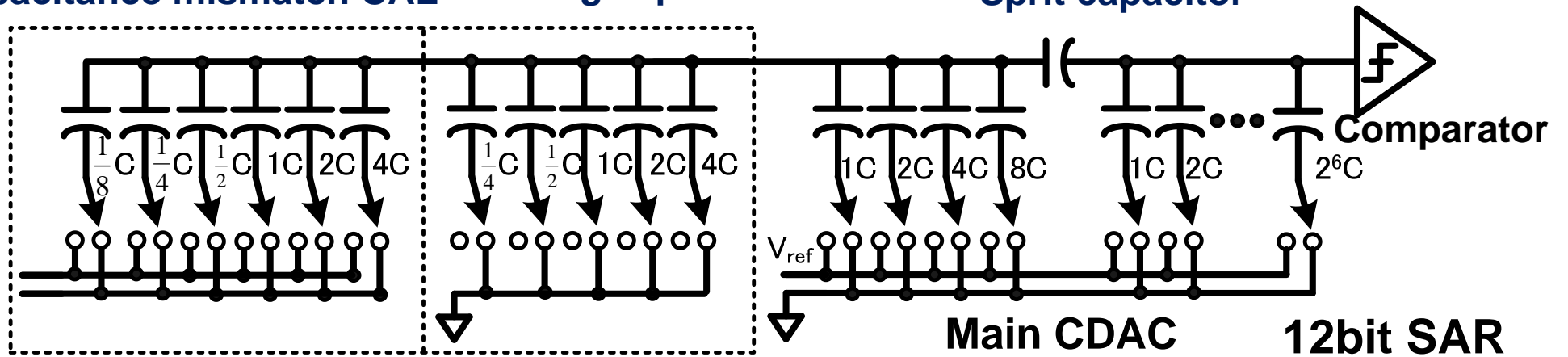**FoM2 is supported by theory and show the energy trend more clearly.**

$$FoM = \frac{P}{2^{(SNDR-1.76)/6.02} \cdot Fs}$$

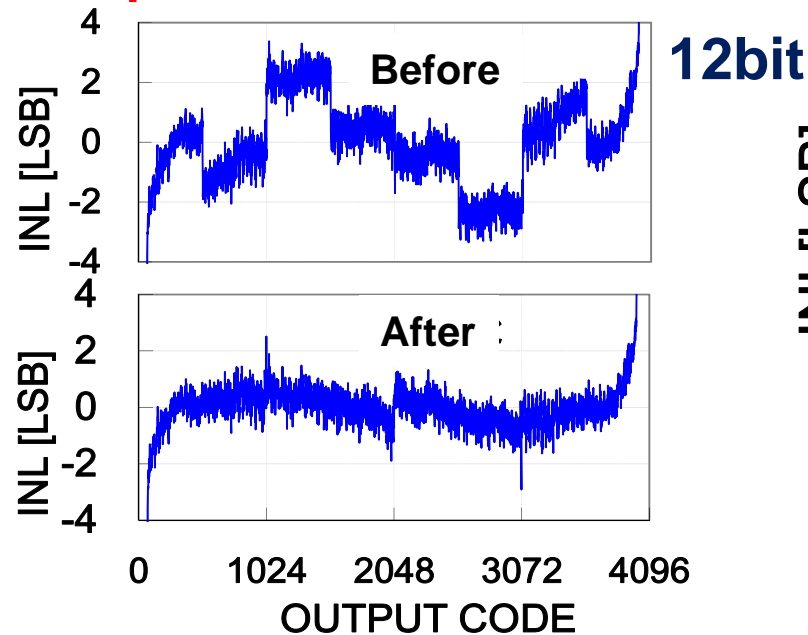$$FoM2 = \frac{P}{2^{2 \cdot (SNDR-1.76)/6.02} \cdot Fs}$$

Linearity of SAR ADC

Non-linearity caused by CDAC can be compensated digitally by using very small capacitor array. Therefore, a small capacitance can be used.
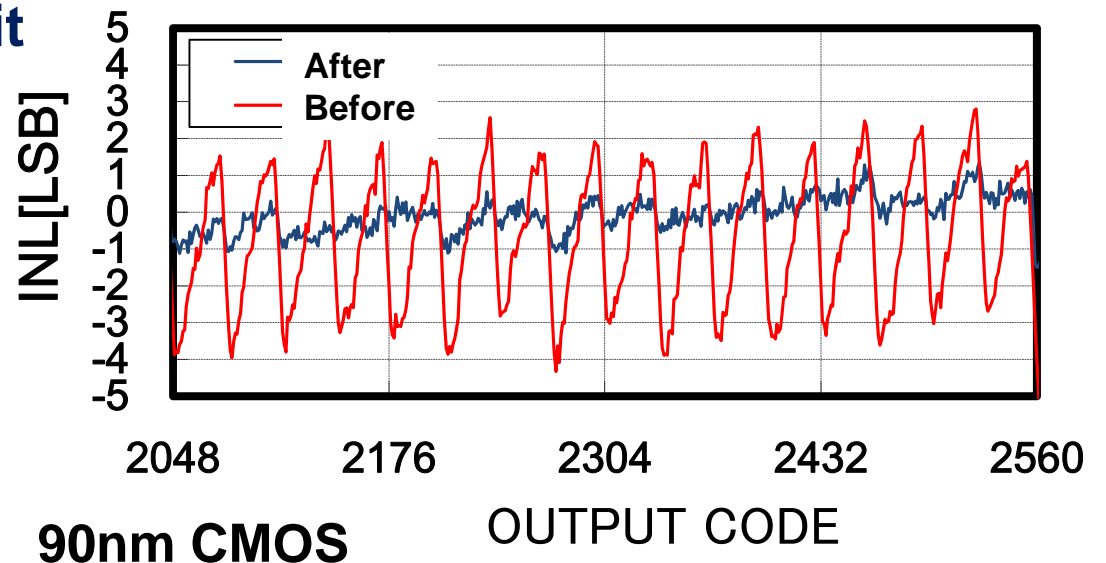
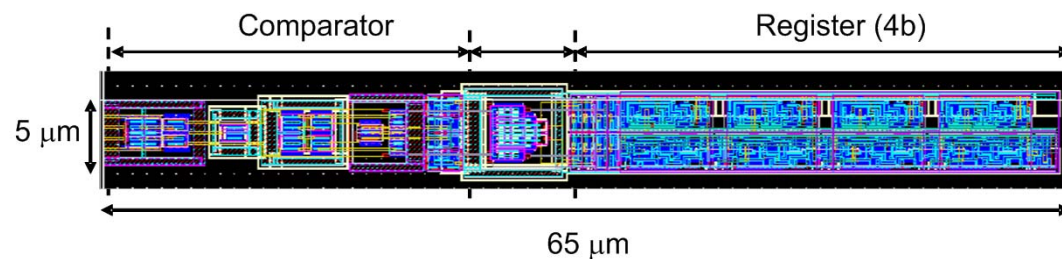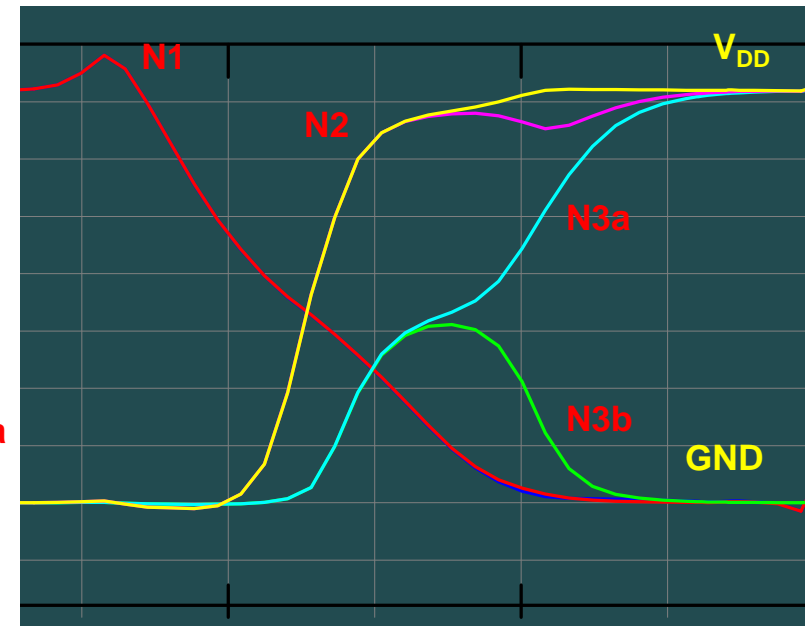**Capacitance mismatch CAL** **Floating capacitance CAL** **Sprit capacitor**

$\frac{1}{8}C$ $\frac{1}{4}C$ $\frac{1}{2}C$ $1C$ $2C$ $4C$ $\frac{1}{4}C$ $\frac{1}{2}C$ $1C$ $2C$ $4C$ $1C$ $2C$ $4C$ $8C$ $1C$ $2C$ 2^6C

Comparator

V_{ref} **Main CDAC**   **12bit SAR**

Capacitance mismatch CAL

12bit

Before

After

Floating capacitor CAL

After
Before

90nm CMOS

OUTPUT CODE

**A proposed dynamic comparator consumes no static current.
Operating speed is high of 4GHz and noise is very low.
The offset voltage can be compensated by changing the C_L or I_D.**

Dynamic amplifier Latch

Mismatch Comp.

CLK

N1b

N1a

C_L C_L

V_{in-}

For CAL

I_D I_D

V_{in+}

M_1 M_2

N2a N2b

N3b

N3a

N1

V_{DD}

N2

N3a

N3b

GND

Comparator Register (4b)

5 μm

65 μm
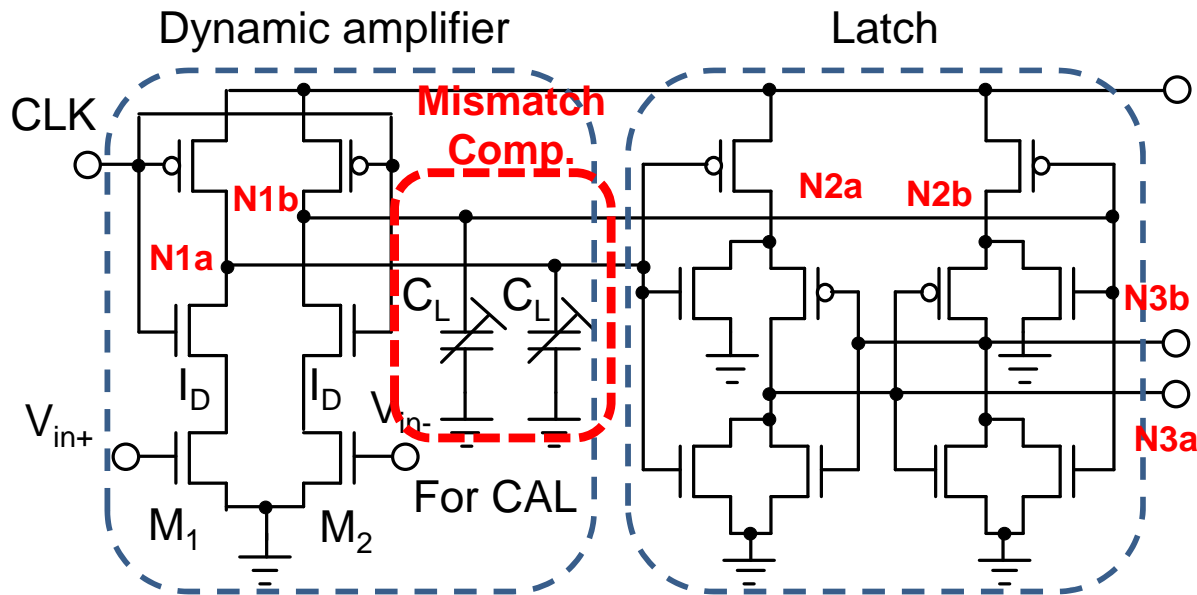
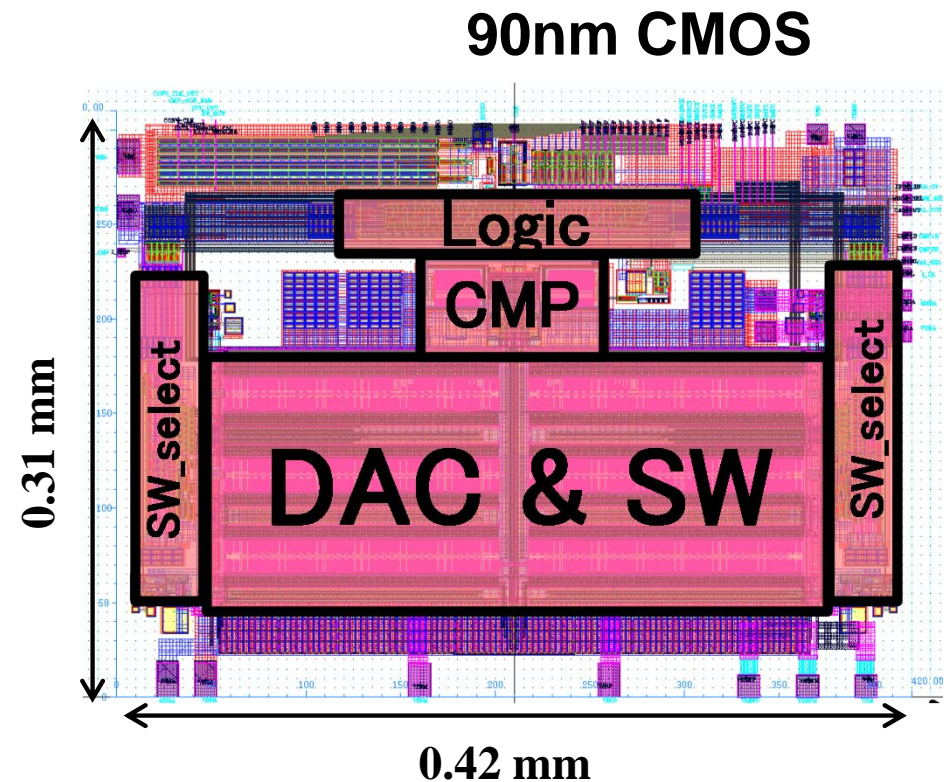**90nm CMOS**

**M. Miyahara and A. Matsuzawa, et al.,
A-SSCC, Nov. 2008.**

**Y. Asada, and A. Matsuzawa, et al.,
A-SSCC, Nov. 2009.**

We have developed 12bit SAR ADC using 90nm CMOS technology.
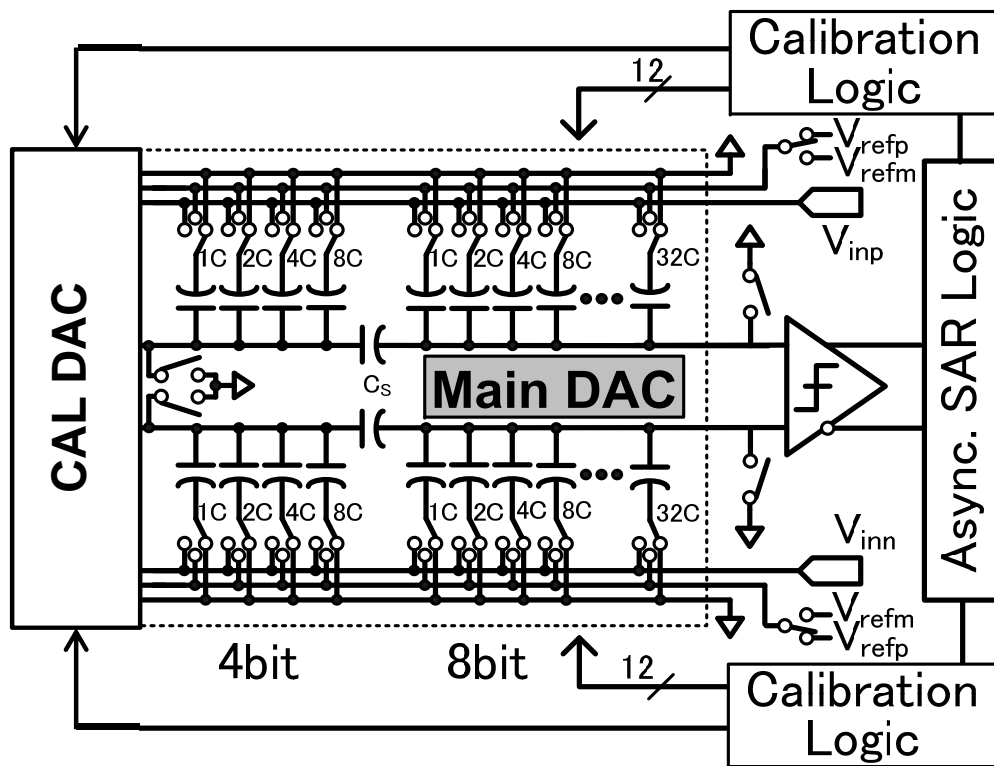
Block diagram of the SAR ADC

Layout of the SAR ADC

Self clocking technique
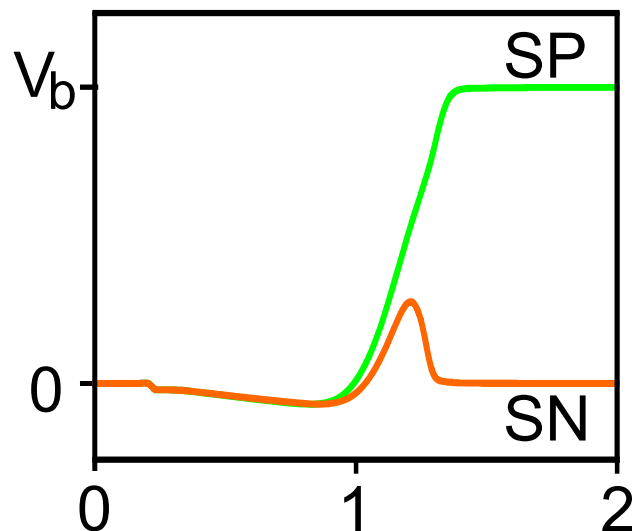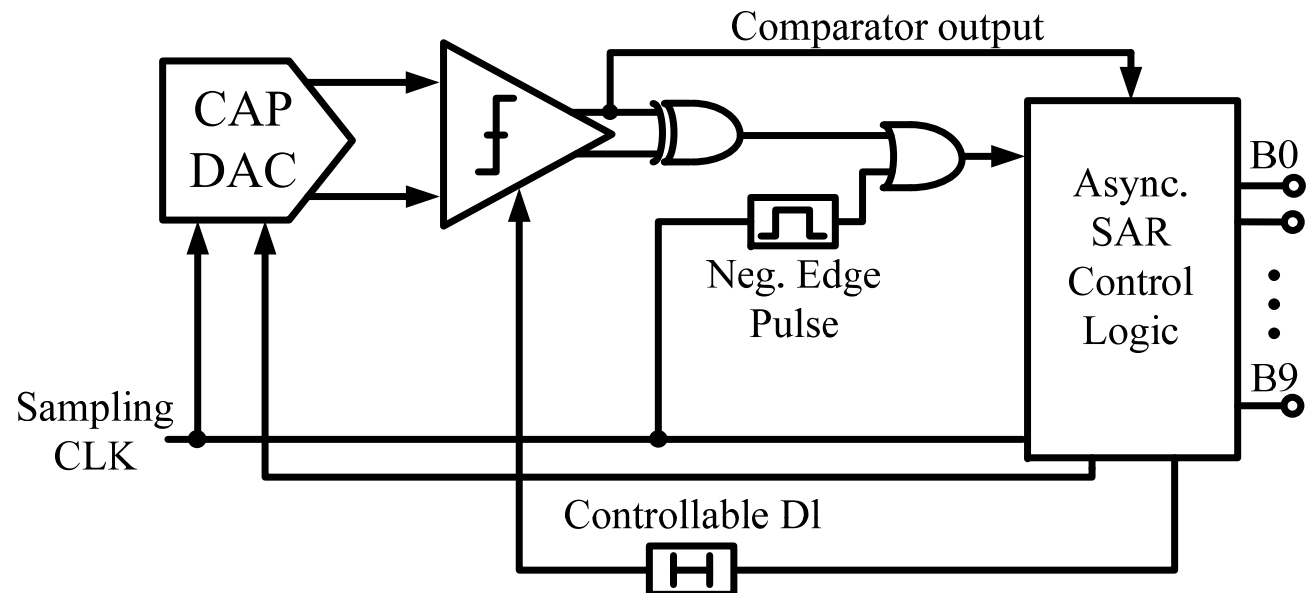
Self-clocking scheme is very useful

1) Reducing power consumption (Clock circuits, routing clock,)
2) Just an enable sampling pulse is required. No need of clock.

Comparison is ended if the output voltages are not same.

Output voltage of
dynamic comparator

Self-clocking scheme

V_b

SP

0

SN

0   1   2

Comparator output

CAP DAC

Neg. Edge Pulse

Async. SAR Control Logic

B0

B9

Sampling CLK

Controllable Dl
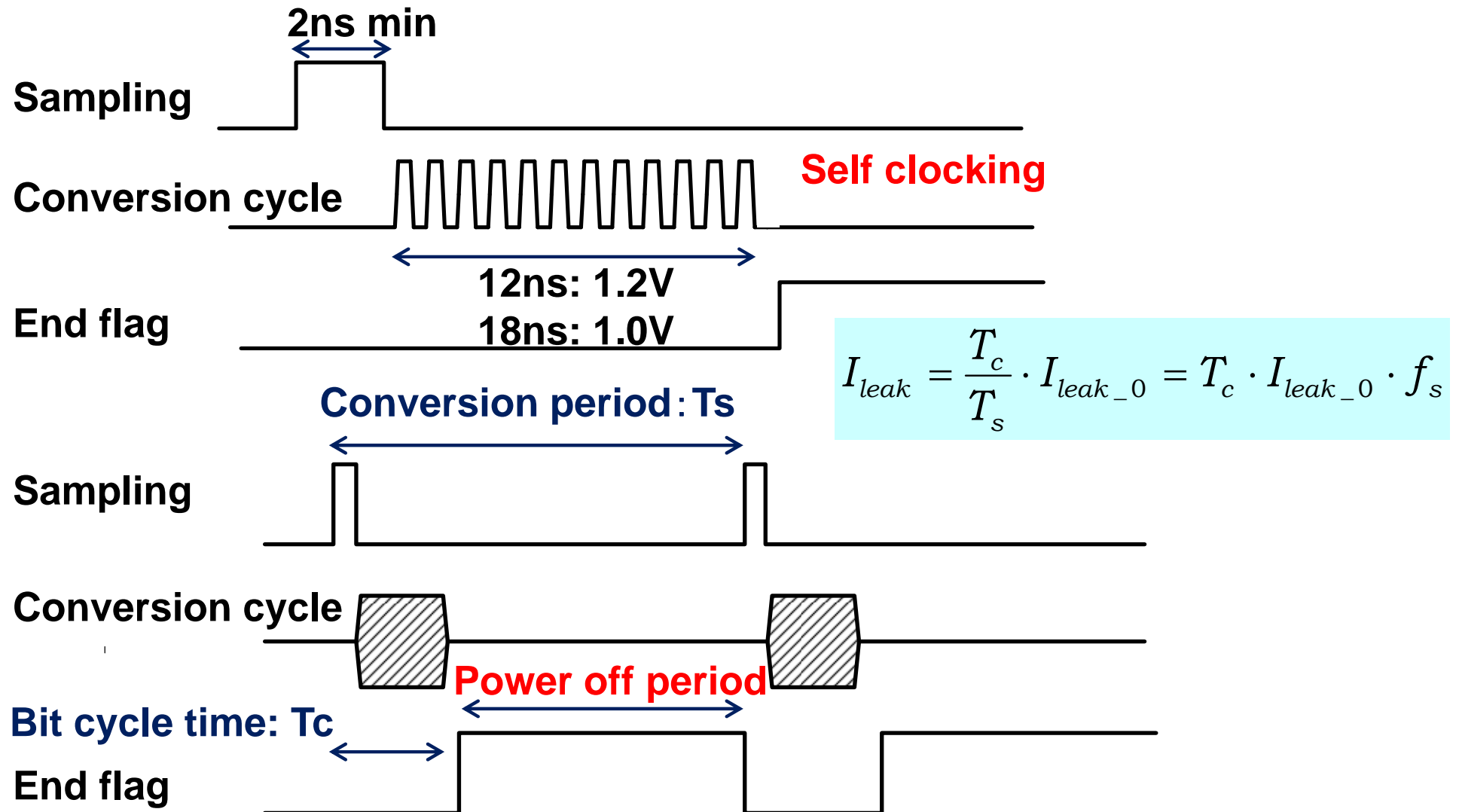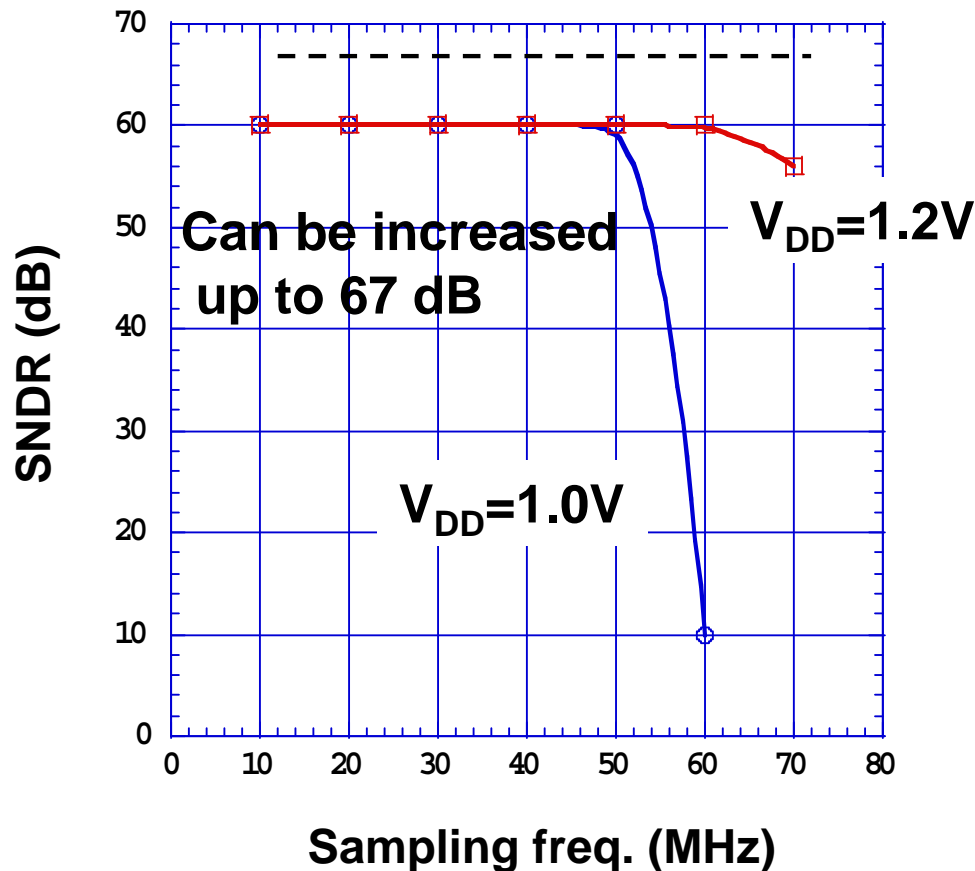
Timing and Leakage cutoff

ADC needs only sampling pulse and the conversion cycle is made by self clocking. The end flag is generated after the conversion, and it can be used as a leakage cutoff switch pulse.

2ns min

Sampling

Conversion cycle — **Self clocking**

12ns: 1.2V
18ns: 1.0V

End flag

$$I_{leak} = \frac{T_c}{T_s} \cdot I_{leak\_0} = T_c \cdot I_{leak\_0} \cdot f_s$$

Conversion period : Ts

Sampling

Conversion cycle

Power off period
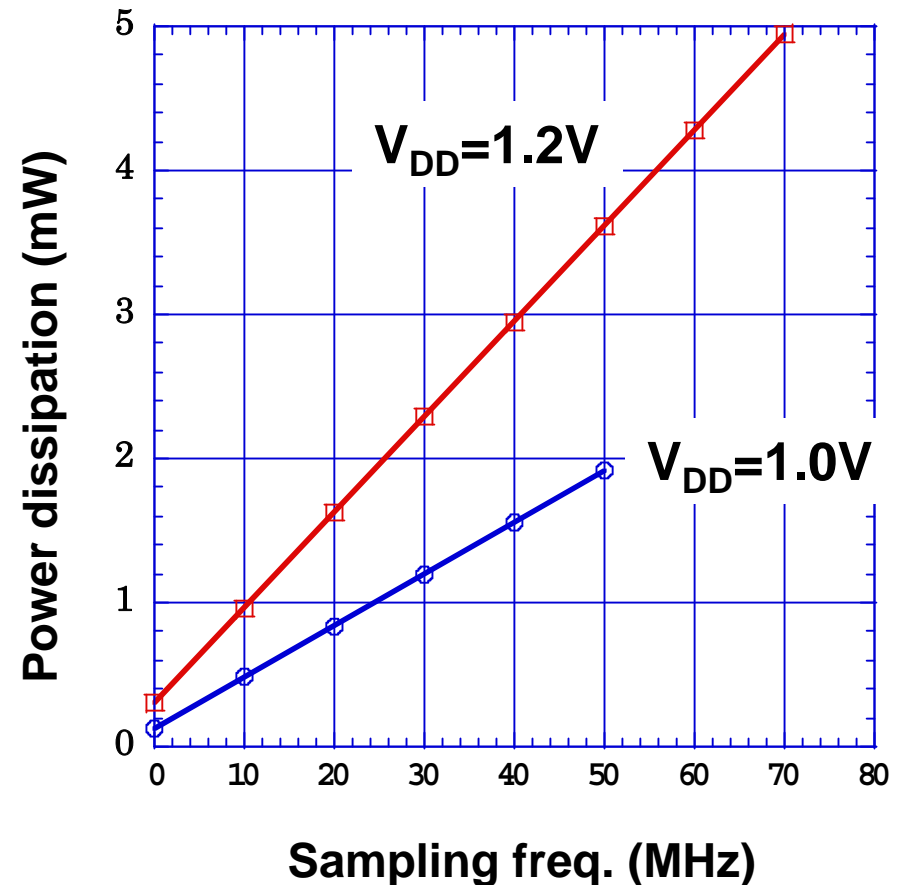
Bit cycle time: Tc

End flag

Measured performance of 12b SAR ADC

Very low energy and high speed operation can be obtained.
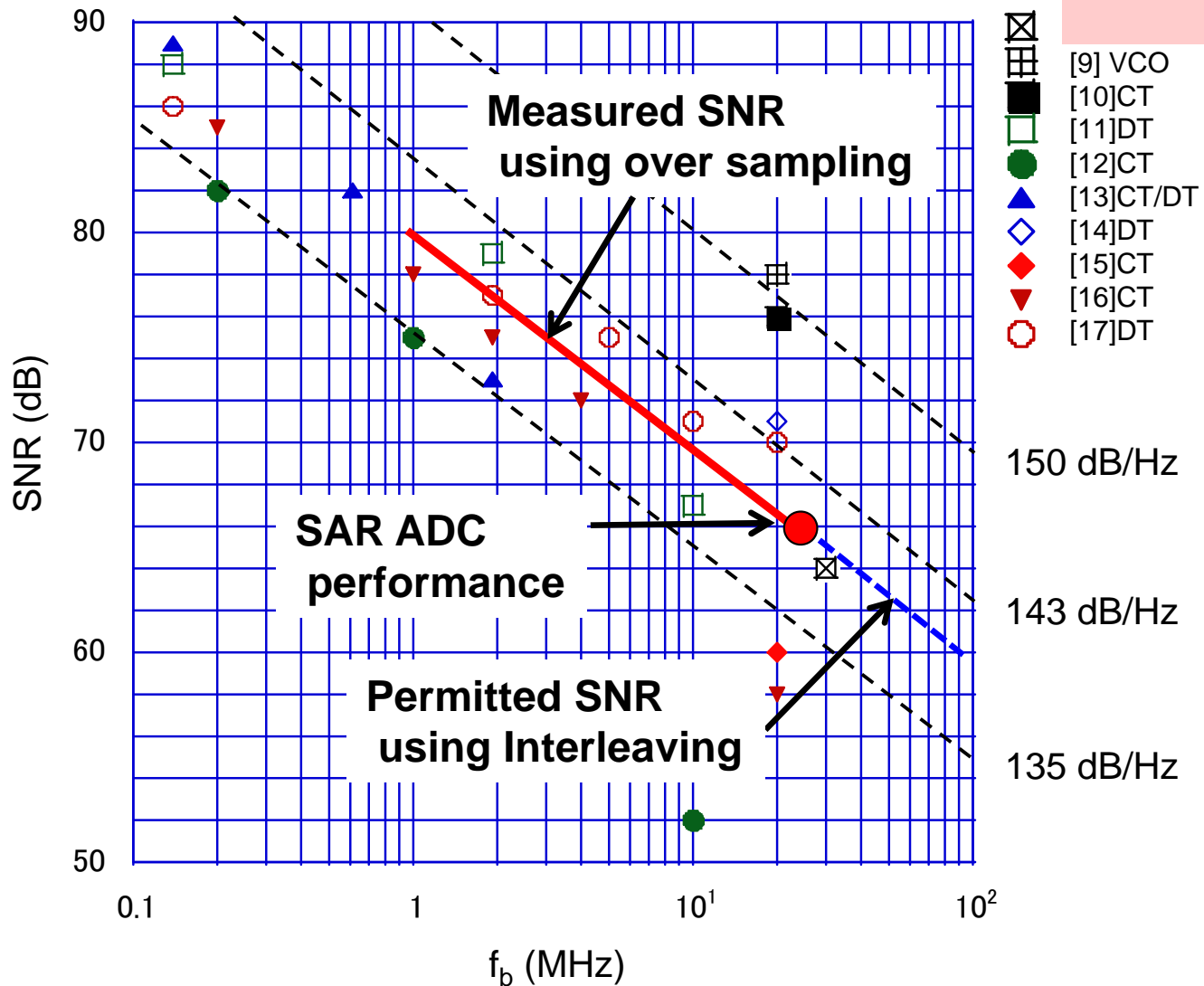**Power dissipation is quite scalable with sampling frequency.**

SNDR vs. f_s

Can be increased
up to 67 dB

V_{DD}=1.2V

V_{DD}=1.0V

SNDR (dB)

Sampling freq. (MHz)

P_d vs. f_s

V_{DD}=1.2V

V_{DD}=1.0V

Power dissipation (mW)

Sampling freq. (MHz)

SNR vs. signal bandwidth of ADCs

SNR can be increased by over sampling using digital filter.

$$SNR \approx SNR_{Nyq} + 10\log\left(\frac{f_{Nyq}}{f_b}\right)$$

Legend:
- ⊠ / ⊞ [9] VCO
- ■ [10]CT
- □ [11]DT
- ● [12]CT
- ▲ [13]CT/DT
- ◇ [14]DT
- ◆ [15]CT
- ▼ [16]CT
- ○ [17]DT

SNR_Nyq=66dB @25MHz

$SNR_{Nyq}=66dB @25MHz$

$f_{Nyq}=25MHz$

Measured SNR using over sampling

SAR ADC performance

Permitted SNR using Interleaving

150 dB/Hz

143 dB/Hz

135 dB/Hz

SNR (dB)

f_b (MHz)

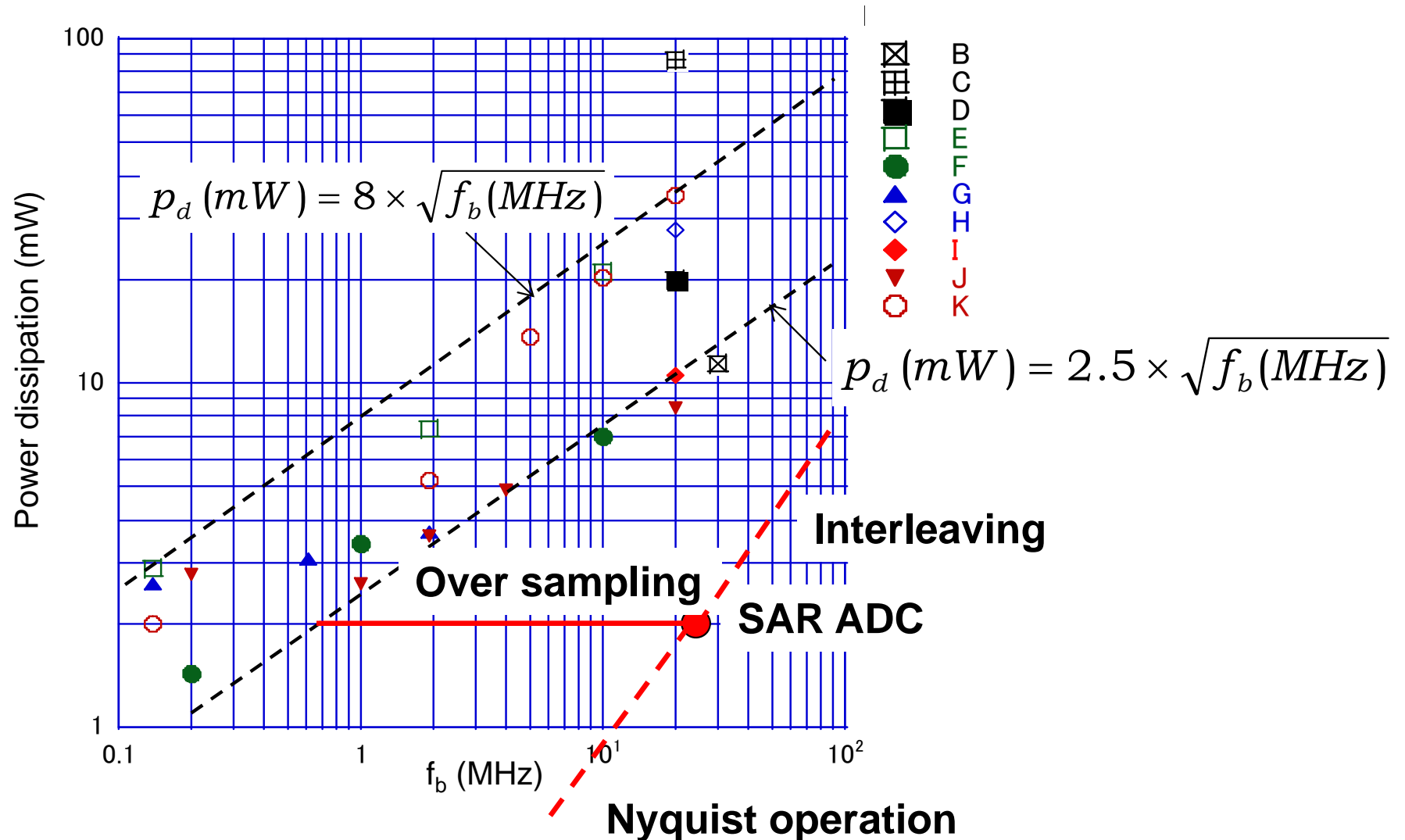**P_d of SAR ADC is lower than that of SD ADC.**
**Even if the over sampling method is used, it still lower.**
If the sampling frequency is lower, P_d becomes lower e.g. 100uW.

$$p_d(mW) = 8 \times \sqrt{f_b(MHz)}$$

$$p_d(mW) = 2.5 \times \sqrt{f_b(MHz)}$$

Interleaving

Over sampling
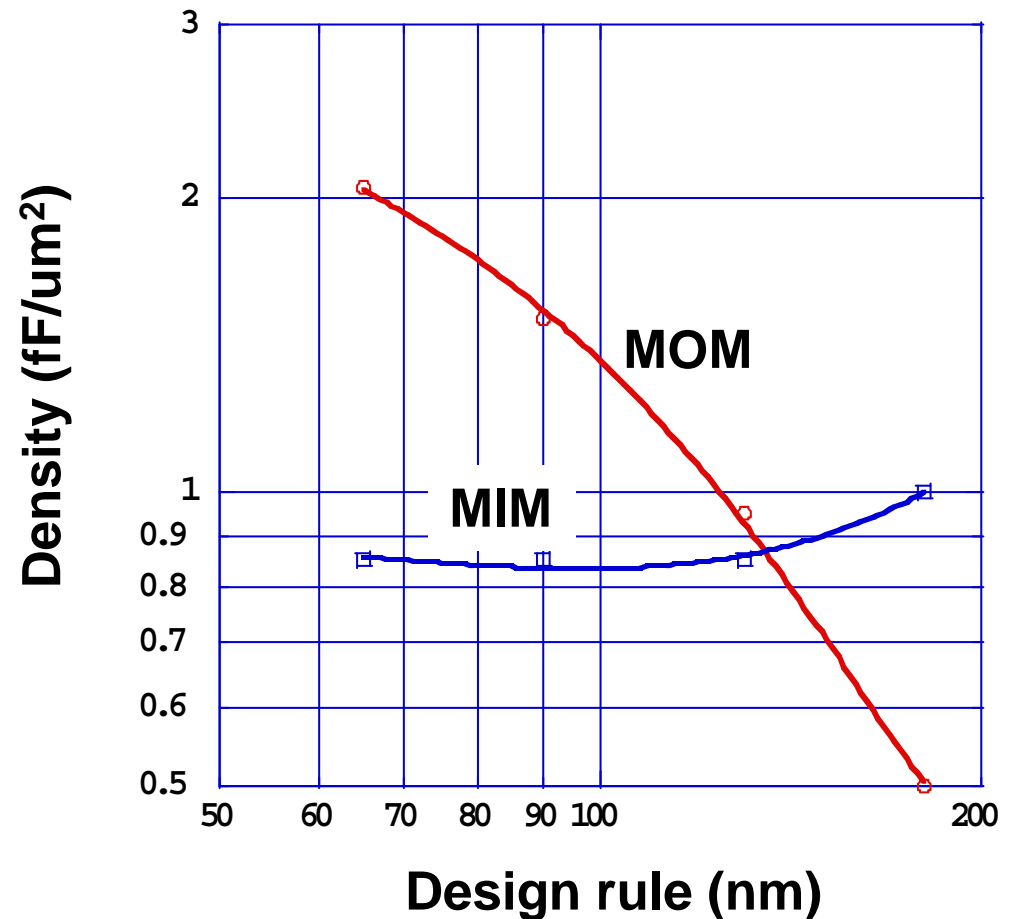
SAR ADC

Nyquist operation

Use of MOM capacitance

MIM capacitance has a good matching, MOM is not so,,,.
However matching issue can be solved by digital mismatch compensation.
Capacitor density is increased by technology scaling.
Very small capacitance (<0.1fF) is available and useful for the mismatch comp.

MOM capacitance

MOM

MIM

Density (fF/um^2)

Design rule (nm)
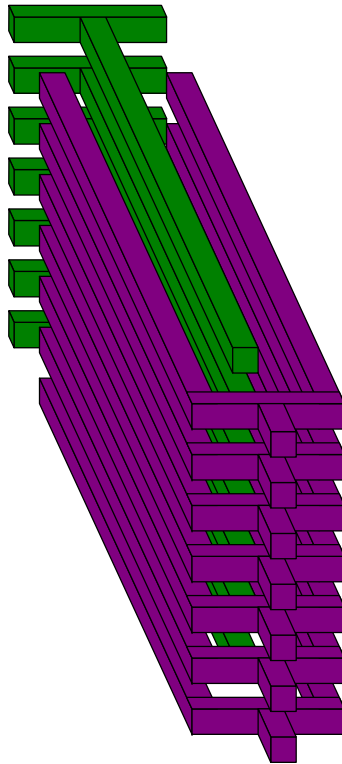
SAR ADC must be better than the SD ADC
; Small area, low power, easy to design, and low voltage of LT. 1.0V.

SAR ADC: Area：0.03mm^2 (65nm) f_b=25MHz P_d=2.0mW, SNDR=70dB
SDADC: Area：0.05mm^2 (40nm) f_b=10MHz P_d=2.6mW, SNDR=70dB

Conference	Technology	Area (mm^2)	Power (mW)	SNDR (dB)	DR (dB)	BW (MHz)	Fs (MHz)	FOM (fJ/conv.)	FOM2
Modulator-B	40nm	0.051	2.57	70.0	70.6	10	300	50	166.5
Modulator-A	65nm	0.060	1.36	68.8	69.3	3	186	101	162.0
VLSI2011[4]	40nm	0.085	2.80	78.0	83.0	1.92	246	112	171.4
ISSCC2006[5]	130nm	1.2	20.0	74.0	76.0	20	640	122	166.0
ISSCC2011[6]	90nm	0.15	8.0	63.5	70.0	25	500	125	164.9
ISSCC2009[7]	65nm	0.084	4.52	79.1	80.0	2	128	153	166.5
CICC2010[2]	65nm	0.16	3.6	69.8	70.2	4	140	178	160.7
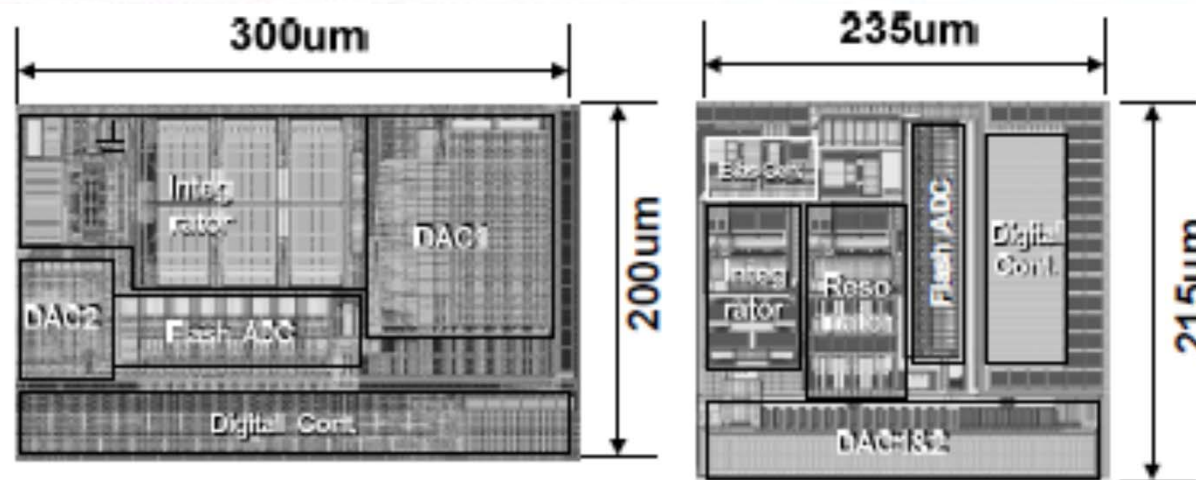
(a)Modulator-A

(b) Modulator-B

K. Matsukawa,
S. Dosho, VLSI 2012

Summary

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  - **Low power**
  - **Low voltage ..0.7V**
  - **Scalable P_d for the sampling frequency**
  - **Can increase SNR by oversampling using digital filter**
  - **Can increase signal bandwidth by interleaving**
  - **Small occupied area**

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