A 60-GHz CMOS Direct-Conversion Transmitter with Injection-Locking I/Q Calibration

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***Abstract*—This paper proposes a 60-GHz direct-conversion transmitter using an injection-locking I/Q calibration. The 65-nm CMOS transmitter consists of a 5-stage PA, differential VGAs, up-conversion Gilbert-cell mixers, 60GHz quadrature injection-locked oscillators, baseband amplifiers, and 20GHz PLL. The measured sideband rejection ratio is 56 dB by using the proposed calibration technique. The transmitter consumes 240 mW from a 1.2-V supply, and can transmit 7 Gb/s in 16QAM.**

Keywords*—CMOS, millimeter wave, 60GHz, transmitters, injection-locked oscillator, direct conversion, calibration.

I. Introduction

In order to achieve higher wireless data rate, the use of 60-GHz carrier is one of the promising technologies. The IEEE 802.11ad standard defines four 2.16-GHz-bandwidth channels around the 60-GHz frequency [1]. In QPSK, 3.5 Gb/s can be achieved, and 7 Gb/s in 16QAM can be achieved by using the 2.16-GHz frequency bandwidth in RF data rate. This is a very big motivation to use the 60-GHz carrier frequency. The 60-GHz wireless transceivers, implemented by CMOS chips, employing heterodyne architecture have been reported [2]–[4]. The direct-conversion transceivers have also been reported for saving area and power consumption [5]–[8]. However, the accurate quadrature LO generation is still challenging because it can be easily degraded by layout parasitic and PVT variation. The I/Q mismatch deteriorates the EVM performance, which is one of the most important remaining issues for mmW direct-conversion transceivers.

The I/Q gain and phase mismatches, caused by both RF and BB circuit blocks as shown in Fig. 1, have to be calibrated especially for the 16QAM modulation. The gain mismatch can be calibrated by amplifiers. However, the phase characteristic is also influenced due to the very high frequency of 60GHz and the wide bandwidth of 2.16GHz, so a fine calibration is not easy for analog amplifiers. Even though an I/Q phase calibration in the digital baseband is a common technique for lower-frequency transceivers, it is difficult to achieve a fine phase resolution for millimeter-wave transceivers due to the limited resolution of DAC, *e.g.*, 6-bit [7]. Thus, the hybrid I/Q calibration is proposed in this paper, which uses a quadrature injection-locked oscillator for a fine I/Q phase calibration.

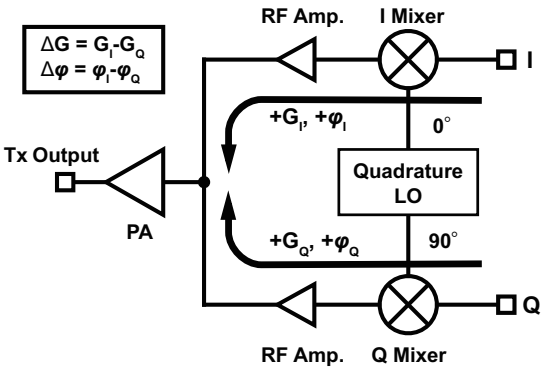


Fig. 1. I/Q mismatch error on transmitter

II. 60GHz CMOS Transmitter with Injection-Locking I/Q Calibration

A. Architecture

Fig. 2 shows the simplified block diagram of the proposed 60-GHz transmitter. The transmitter has a direct-conversion architecture. It consists of a 5-stage single-ended power amplifier (PA), parallel-line transformer balun [6], I/Q differential variable gain amplifiers (VGA), double-balanced Gilbert-cell up-conversion mixers, baseband (BB) gain-peaking amplifiers, and 60-GHz quadrature injection-locked oscillator (QILO) with 20-GHz PLL [7]. The differential VGAs are used for the I/Q gain calibration, and the QILO is used for the I/Q phase calibration. The VGA also has the phase shifting involved with the gain control, so the QILO compensates the entire I/Q phase mismatch caused by RF and BB amplifiers.

B. 60GHz LO using single-side injection QILO

Fig. 3(a) shows a simplified block diagram of 60-GHz quadrature local oscillator (LO). The LO consists of 60-GHz QILO, shown in Fig. 3(b), and 20-GHz PLL. The QILO works as a frequency tripler, and can generate I and Q LO signals. Since the 60-GHz phase noise of locked QILO is determined by that of 20-GHz PLL, the QILO can be designed to have a wide tuning range without paying much attention to lowering the phase noise in free-running state.

The QILO employs a single-side injection architecture as shown in Fig. 3(a), which is one of the most important

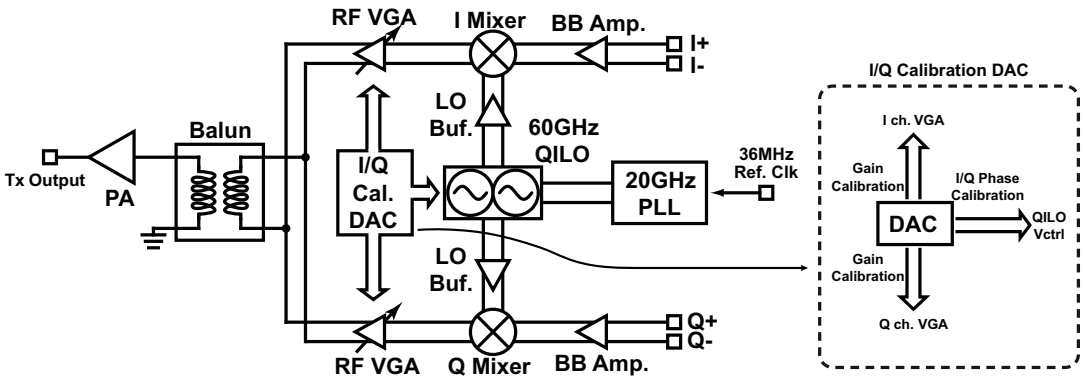
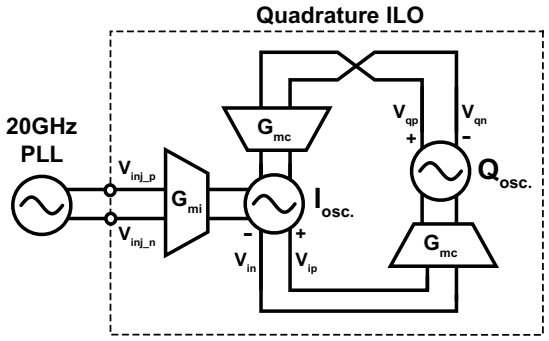
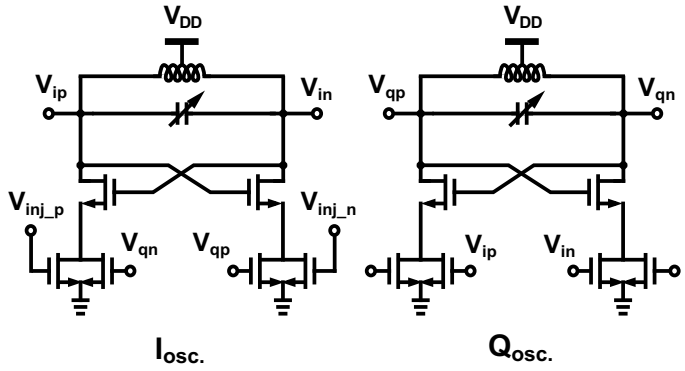


Fig. 2. Block diagram of the proposed 60-GHz transmitter with injection-locking I/Q calibration



(a) Block diagram of Quadrature LO



(b) Detail circuit schematic of QILO

Fig. 3. Quadrature LO with single-side injection QILO

features in the proposed transmitter. The quadrature-injection QILO in [8] uses a poly-phase filter for generating 20-GHz quadrature injection signal, and the I/Q phase mismatch is basically determined by that of poly-phase filter. On the other hand, the single-side injection enables controlling I/Q phase offset by adjusting the free-running frequency of QILO.

Fig. 4 shows an equivalent circuit of QILO in Fig. 3(b). I-oscillator has injection signals from Q-oscillator and 20-GHz PLL, and Q-oscillator also has an injection signal from I-oscillator.

In a steady-state, the stationary phase angle between tank current and cross-couple transistor current is expressed by the following equation [9].

$$\phi_{\rm ss} = \sin^{-1}\left[2Q\left(\frac{\omega_0 - \omega_{\rm inj}}{\omega_0}\right)\cdot\frac{I_{\rm osc}}{I_{\rm inj}}\right] \tag{1}$$

where Q is the quality factor of LC-tank, ω_0 is the tank resonance angular frequency, $\omega_{\rm inj}$ is the angular frequency of injected signal, $I_{\rm osc}$ is the current used for oscillation, and $I_{\rm inj}$ is the current flow by injected signal. From this equation, the phase relations between each current vectors in Fig. 4 are depicted as shown in Fig. 5, and are expressed by the following equations.

$$\begin{aligned}\phi_{\rm i} &= \phi_{\rm ip}(=\phi_{\rm in})\\ &= \sin^{-1}\left(2Q\frac{\omega_{0\rm i}-\omega_{\rm inj}}{\omega_{0\rm i}}\frac{I_{\rm osc\_ip}}{I_{\rm inj\_ip}+\alpha I_{\rm inj\_PLLp}}\right) \quad (2)\\ \phi_{\rm q} &= \phi_{\rm qp}(=\phi_{\rm qn})\\ &= \sin^{-1}\left(2Q\frac{\omega_{0\rm q}-\omega_{\rm inj}}{\omega_{0\rm q}}\frac{I_{\rm osc\_qp}}{I_{\rm inj\_qp}}\right) \quad (3)\\ \Delta\phi &= \phi_{\rm q}-\phi_{\rm i} \quad (4)\end{aligned}$$

where ω_{0i} and ω_{0p} are the resonance angular frequencies of I and Q oscillators, respectively. α is the injection efficiency, when a QILO locked at N^{th} subharmonic frequency of injection signal, it is approximately $1/N$. The currents $I_{\rm osc\_ip}$, $I_{\rm inj\_ip}$, $I_{\rm osc\_qp}$, $I_{\rm inj\_qp}$, and $I_{\rm inj\_PLLp}$ are as in Figs. 4 and 5.

Fig. 6 shows the calculated result of phase offset from an ideal quadrature phase by sweeping the free-running frequency of QILO, which uses 65nm CMOS parameters. Here, the locked frequency is 60.48-GHz and injection frequency is 20.16-GHz, which is $1/3$ of the locked one. As shown in Fig. 6, the tunable phase offset in I/Q LO signals can be generated by adjusting the free-running frequency, for compensating the I/Q phase mismatch. The free-running frequency can be adjusted by DC-domain fine-resolution DACs, so a very fine and wide-range I/Q phase calibration can be realized.

C. Transmitter blocks

Fig. 7(a) shows the schematic of the up-conversion mixer with BB gain-peaking amplifier. The amplifier function is to compensate the frequency response of up-conversion mixer gain. The simulated up-conversion gain is shown in Fig. 7(b).

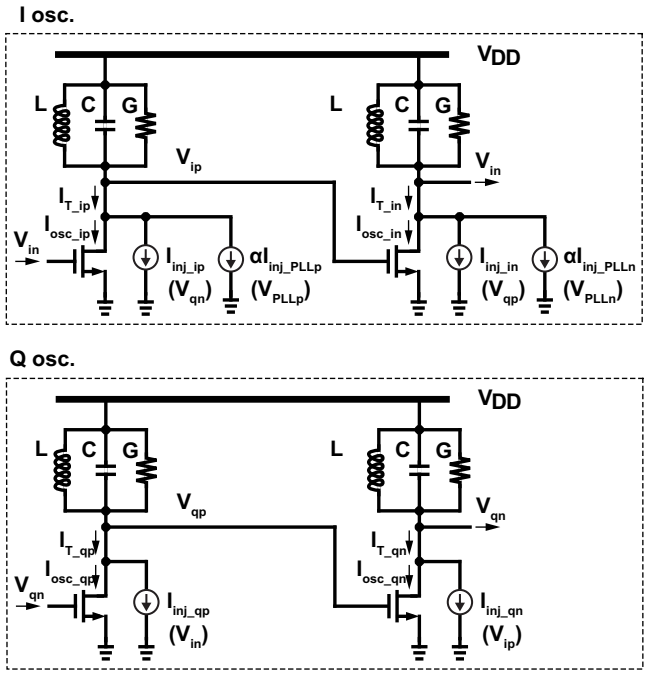


Fig. 4. Equivalent circuit of quadrature injection-locked oscillator

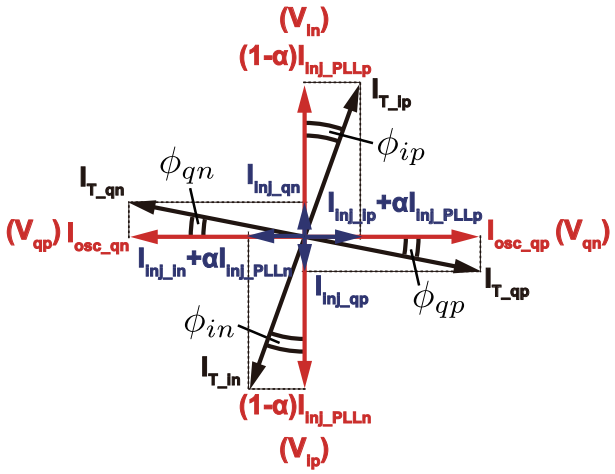


Fig. 5. Current vectors in locking state

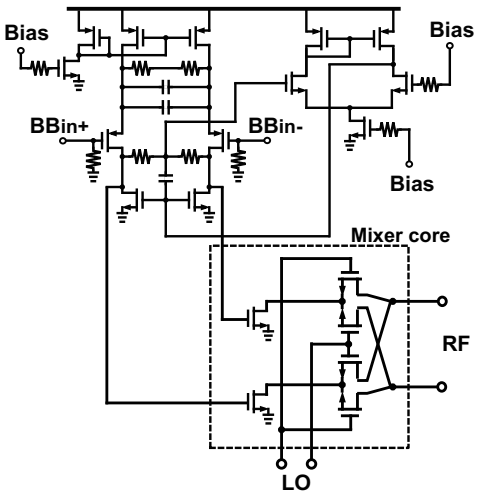
The gate bias of RF amplifiers is adjusted to compensate gain in order to calibrate the amplitude mismatch between I and Q paths. After the amplitude mismatch goes close to zero, the phase mismatch is calibrated on QILO by adjusting the free-running frequency of QILO, as discussed in the previous subsection.

III. Measurement Results

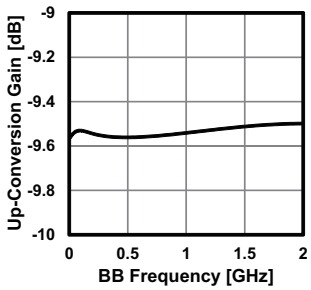
The transmitter is implemented in a standard 65 nm CMOS process. The die micrograph of the fabricated transmitter is shown in Fig. 8. The layout area is 8.74 mm^2 with an active area of 4 mm^2. The measured P_{sat} is 8.8 dBm. The phase noise of 20-GHz PLL is -106dBc/Hz at 1MHz offset. The power consumption is 240 mW (165 mW for the transmitter including 60-GHz QILO, and 75 mW for the PLL) with a 1.2-V supply voltage.

Fig. 9 shows the measured SRR of the transmitter output. The QILO control voltage (V_{ctrl}) is controlled by a 10-bit control DAC. The SRR was measured with 100MHz I/Q CW

Fig. 6. Calculation results of phase offset from quadrature



(a) Simplified schematic



(b) Up-conversion gain

Fig. 7. Gain-compensated up-conversion mixer

TABLE I. PERFORMANCE COMPARISON OF 60-GHZ CMOS TRANSMITTERS

	CMOS tech.	Topology	Conversion Gain	SRR	EVM	I/Q Calibration	P_{DC}
This work	65 nm	Direct-conversion	15 dB	**56 dB**	−23 dB	Yes	240 mW
Tokyo Tech. [7]	65 nm	Direct-conversion	18 dB	46 dB	−23 dB	No	319 mW
Toshiba [4]	65 nm	Heterodyne	15 dB	28 dB	—	N.A.	160 mW
IMEC [8]	40 nm	Direct-conversion	22 dB	—	−18 dB	N.A.	167 mW
CEA-LETI [3]	65 nm	Heterodyne	15 dB	—	−17 dB	N.A.	357(Tx) mW 732(ext. PA) mW
SiBeam [2]	65 nm	Heterodyne	—	—	−19 dB	N.A.	1820 mW
UCLA [11]	90 nm	Half-RF	—	20 dB	—	N.A.	78 mW

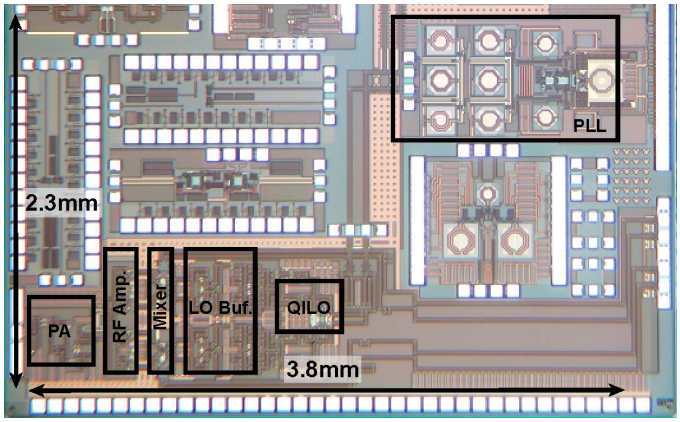


Fig. 8. Die micrograph

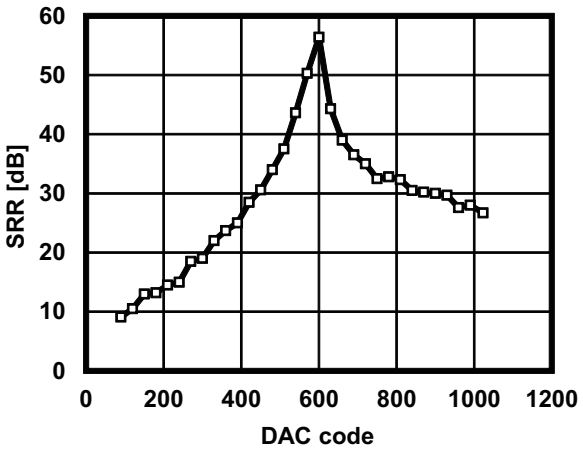


Fig. 9. Measured SRR versus DAC code of QILO $V_{\rm ctrl}$

input from an arbitrary waveform generator. As discussed in Section II, it is observed that the SRR performance is improved as the free-running frequency shifts by tuning the DAC code. The peak SRR is 56 dB in this case. This is equivalent to 0.18 degree phase error.

We measured the EVM performance by using a receiver chip reported in [7]. The transmitter PA output is connected to 14 dBi horn antenna, and the receiver input is connected to 6dBi in-package antenna. The modulated signal is inputted from an arbitrary waveform generator. The output baseband signal of receiver is measured by a digital oscilloscope. The measured Tx-to-Rx EVMs are −21.5 dB in QPSK and −23 dB in 16QAM.

Table 1 shows a performance comparison with the state-of-the-art 60GHz transmitters. The proposed transmitter achieves the highest SRR to enable high quality wireless communication in 60-GHz band.

IV. CONCLUSION

This paper has proposed a 60-GHz CMOS direct-conversion transmitter with injection-locking I/Q calibration. The implemented transmitter achieves the highest SRR performance by using a fine I/Q phase mismatch calibration.

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