A 13.2% Locking-Range Divide-by-6, 3.1mW, ILFD using Even-Harmonic-Enhanced Direct Injection Technique for Millimeter-Wave PLLs

Teerachot Siriburanon, Wei Deng, Ahmed Musa, Kenichi Okada, and Akira Matsuzawa
Department of Physical Electronics, Tokyo Institute of Technology
2-12-1-S3-27, Ookayama, Meguro-ku, Tokyo 152-8552, Japan. E-mail: tee@ssc.pe.titech.ac.jp

Abstract— This paper presents a wide-locking-range, low-power, Injection-Locked Frequency Divider (ILFD) using even-harmonic-enhanced direct injection technique which can operate with a high division ratio of 4 and 6. The proposed ILFD has been fabricated in a 65nm CMOS process with a core area of 0.002mm^2. The proposed ILFD achieves the widest measured locking range reported of 4.3 GHz (13.2%) for a divide-by-6 operation with a power consumption of only 3.1mW without any tuning mechanism. Moreover, it also achieves 5.7GHz (28.5%) for divide-by-4 operation while consuming only 3.1mW. Combining its multi-division and tuning capability, the dividing capability ranges from 14.0-38.0GHz while consuming 2.8 to 5.4mW.

I. INTRODUCTION

To meet the demand for increasing required data rate in emerging wireless applications, one of the most promising candidate is wireless communication using 60-GHz carrier frequency [1]-[3]. In the design of RF front-ends for mm-wave applications, one of the most important building blocks is the low-power 60-GHz local oscillator (LO). For a 60GHz frequency generation, a push-push VCO [2]-[3] or a sub-harmonic injection [4]-[5] are widely employed to avoid a power-hungry 60-GHz prescaler divider. Even though this approach can alleviate the power consumption by using a 30GHz prescaler divider, a higher-division-ratio is even more preferable to further reduce a number of high frequency dividing stages.

Conventionally, for high-speed frequency dividers, a Current Mode Logic (CML) divider is commonly used due to its wide locking range. However, several stages of cascaded CML dividers are needed before digital dividers can operate [2], [4]. More importantly, when operating at frequency higher than 20GHz, the power consumption of CML dividers increases tremendously. Therefore, an alternative approach using Injection-Locked Frequency Divider (ILFD) has become an appropriate solution for the first-stage divider in a low-power mm-wave frequency synthesizer since it can divide by higher than 2 and consume much lower power consumption at higher frequencies. Even though ring-based ILFDs have an advantage in terms of smaller areas comparing to LC-based ILFDs, a high-division operation in ring-based ILFDs is necessary to avoid more power dissipated for higher oscillation speed at mm-wave frequency. For example, a divide-by-3 ring-based ILFD and its following high speed dividers consume more than half of the power consumed by the entire PLL [3]. As shown in Fig.1, a single ILFD with a high-division operation such as divide-by-6 can down-convert the signal to lower frequency and safely drive the next-stage low-power digital dividers. This approach can significantly help reduce power consumption to enhance the battery life in mobile applications. Unfortunately, conventional ILFDs with a higher-division ratio usually have a narrow locking range which make it impractical over process-voltage-temperature (PVT) variations.

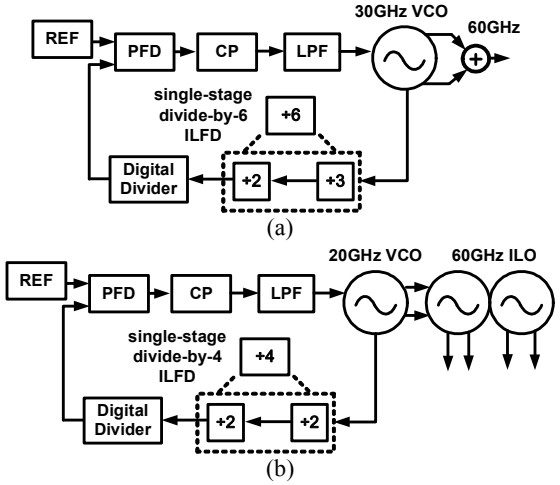


Fig.1. 60GHz frequency synthesizers in (a) [2]-[3] (b) [4]-[5]

In this paper, a low-power wide-locking-range divide-by-4, and 6 ILFD is proposed using an even-harmonic-enhanced direct injection technique instead of conventional direct mixing approach. The proposed ILFD has the widest locking range reported without any frequency tuning mechanisms for a divide-by-6 operation and can be suitable for 60-GHz frequency synthesizers proposed in [2]-[5]. This paper is organized as follows. In section II, the block models of the conventional and the proposed ILFDs are explained. The following section describes the proposed circuit topology in details. Section IV demonstrates experimental results of the proposed ILFD. Finally, a conclusion is summarized in section V.

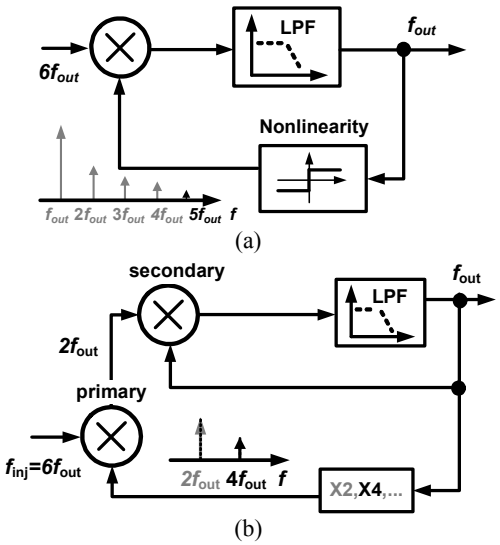


Fig.2. Conceptual block diagram models for (a) conventional ILFDs and (b) the proposed divide-by-6 ILFDs using even-harmonic-enhanced direct injection

II. Injection-Locked Frequency Divider

A. Model for Conventional ILFDs

A conceptual block diagram model for a conventional ring-based ILFD is depicted in Fig.2 (a) which has a fundamental output frequency of f_{out}. Since many high order harmonics are generated by the nonlinear transconductance of a transistor, this enables an ILFD to perform a high-division operation. For example, in a divide-by-6 operation, injection signal f_{inj}, which is approximately $6 \cdot f_{out}$, is mixed with $5 \cdot f_{out}$ harmonics. Only the mixed product that is close to fundamental frequency output is survived after the low-pass characteristics of the output nodes of ring oscillators. The ILFD will lock to the injected signal if the mixed product has enough power so that the oscillation frequency can be pulled and locked to that harmonic [6]. Since the fifth harmonic is much weaker, this method suffers from a narrow locking range. For different division ratios, similar explanation can be applied.

B. Proposed Even-Harmonic-Enhanced Direct Injection ILFD

The proposed block diagram model for an even-harmonic-enhanced direct injection ILFD is depicted in Fig.2 (b) which is composed of two mixing mechanisms in a single ILFD. A primary mixer is used to convert input frequency to the frequency near $2f_{out}$. In other words, it first performs a divide-by-N operation where N is an integer number. After that, a secondary mixer is utilized to further mix the frequency output of the primary mixer with fundamental frequency to a frequency near f_{out} for a divide-by-2 operation where other higher harmonics are filtered out by low-pass-filter characteristics of the output nodes of ring oscillators. Therefore, in the overall configuration, the proposed ILFD can operate as a divide-by-even-order ILFD. Since the secondary mixer utilizes strong fundamental signals for mixing in a divide-by-2 operation, it has a large typical locking range. The bottle neck for the overall locking rage of the proposed ILFD is at the primary mixer. In order to further enhance the locking range of the primary mixing stage, two differential signals at f_{out} are combined in the push-push configuration. As a result, even order harmonics can theoretically be enhanced by 3dB before mixing with the injection frequency. Consequently, the proposed even-harmonic-enhanced direct injection ILFD can perform a high-division operation with a wide locking range.

For example, for a divide-by-6 operation, f_{inj}, which is approximately $6 \cdot f_{out}$, is first mixed with $4 \cdot f_{out}$ harmonics at the primary mixer. The frequency output of the primary mixer is at around $2 \cdot f_{out}$ which is further mixed with a strong f_{out} to the location near its fundamental harmonic where other spurious frequencies are filtered out. If the mixed product is strong enough, the output frequency of ring ILFD will be locked to that harmonic signal. Similar explanation can be applied for the divide-by-4 operation.

III. Circuit Architecture

The proposed even-harmonic-enhanced direct injection ring-based ILFD is depicted in Fig. 3(a). It is composed of a 4-stage differential ring oscillator. The free-running frequency of the oscillator can be tuned by a current source that is connect to a current mirror. The delay cell is based on a differential pair topology with resistor loads as shown in Fig. 3(b). The size of resistor is carefully chosen to maintain enough loop gain and oscillation swing but in tradeoffs with the speed of the ring oscillator. This delay cell can acts as a secondary mixer which mixes the strong second harmonic with fundamental frequency at output nodes through the nonlinearity of transconductance of a transistor. A common node of this delay cell can be used as an even-harmonic-enhanced node which has strong even harmonics. Since at the common node of the first and the third delay cell, there are strong even harmonics

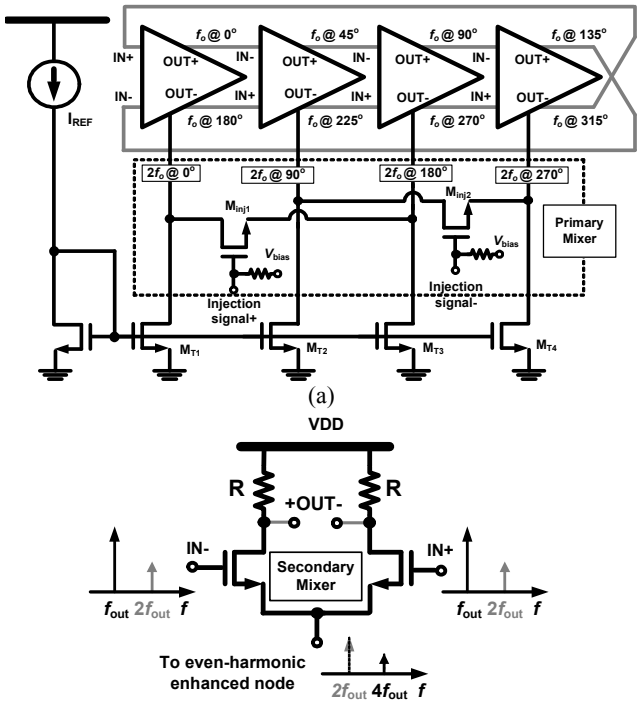


Fig.3. Detailed circuit schematic of the proposed (a) even-harmonic-enhanced ILFD and (b) its delay cell

with a relative phase difference of 180°. An NMOS switch is placed across these two nodes as a direct injection transistor to represent a primary mixer. To allow differential injection for an enhanced injection efficiency, another NMOS switch is placed between the common nodes of the second and the fourth delay cells for injections at appropriate phases. Unlike a conventional direct injection in LC-ILFD, the proposed even-harmonic-enhanced direct injection can perform high-division operation with wide locking range without bulky inductors.

In a conventional ILFD, for a divide-by-6 operation, an injection signal is input to the gate of the tail transistors (M_{T1}) which will mix with the fifth harmonic of f_{out} through a single balanced mixer that is form by a differential pair. Thus, locking range of high division ratio is limitedly narrow. On the other hand, this work, without any additional cascoded transistors [7] or additional inductors [8], can operate with a high division ratio with wide locking range while maintaining a low power consumption. For a divide-by-6 operation, differential injection signals is injected to the transistors (M_{inj1}, M_{inj2}) which mix with an enhanced fourth harmonics at the common nodes of delay cells. This enhanced fourth harmonic results in an improved locking range over the case in a conventional ILFD. Through transistor nonlinearity, the frequency output of the primary mixer is further mixed with fundamental frequency through a built-in secondary mixer. The mixed product will pull and lock the ring oscillation frequency to the injected frequency. For a divide-by-4 operation, the injection frequency is mixed with the strong second harmonic and further mixed with the fundamental frequency through transistor nonlinearity. Thus, free-running frequency of the ring oscillator can be pulled and locked to the injected frequency.

IV. Experimental Results

The proposed ILFD is designed and fabricated in a standard 65nm CMOS process. The microphotograph of the fabricated synthesizer is shown in Fig. 4. The core area of the proposed ILFD is only 47μm × 39μm. The ILFD spectrum is measured with an Agilent E4448A PSA spectrum analyzer. An injection signal is generated by PSG Analog Signal Generator E8257D which is connected to a 180° hybrid coupler to obtain differential injection signals. Fig.5 shows the comparison between the free-running and locked spectrum under divide-by-6 operation at output frequency of 5.67GHz.

The proposed ILFD can operate under 1.0-V supply with a power consumption of 2.2-3.3mW while running at 5.0-5.5GHz. The measured sensitivity curve for divide-by-6 and divide-by-4 operations using a 1.0-V supply is shown in Fig.6 (a) and (b), respectively. The divide-by-6 and divide-by-4 operations of the proposed ILFD show the widest locking range of 4.3GHz (13.2%) and 5.3GHz (25.4%) under 0-dBm input power while consuming only 3.1mW. For a 1.2-V

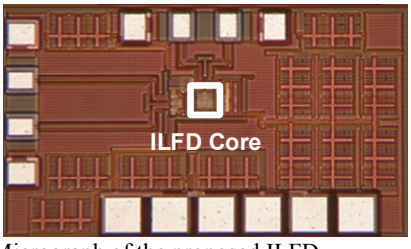


Fig.4. Chip Micrograph of the proposed ILFD

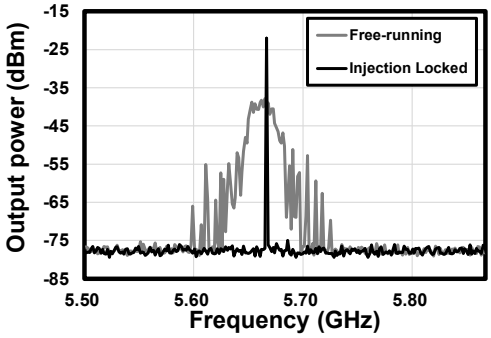
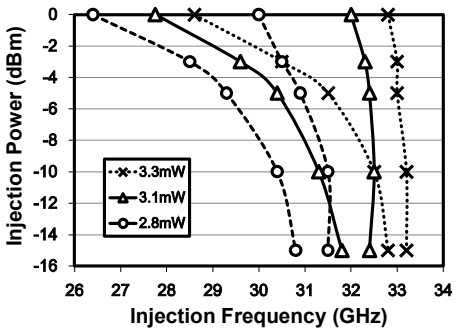
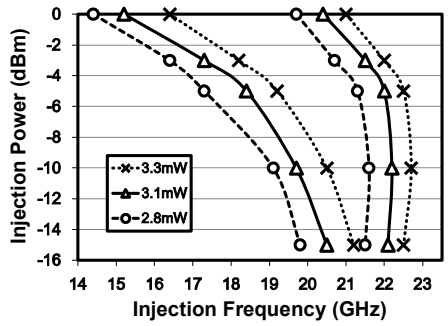


Fig.5. Measured locked spectrum of divide-by-6 operation to an injection frequency of 34GHz

supply, the proposed ILFD consumes a power of 3.0-5.4mW while running at 5.2-6.2GHz. Fig.7 shows the sensitivity curve of the proposed ILFD under 1.2-V supply. For a division-by-4 operation, the widest locking range is 6.6GHz (28.2%) while consuming 4.2mW which has a competitive performance when comparing to publications in [7]-[8]. The locking range for divide-by-4 operation is relatively larger than that of divide-by-6 since the injection frequency is mixed with the stronger second harmonic at the primary mixer. The widest locking range for the divide-by-6 operation is 4.3GHz (13.1%) while consuming 3.6mW. The divide-by-6 operation shows the widest locking range reported and its locking range is acceptably large enough to maintain its locking operation over PVT variations. More importantly, as shown in Fig.6 (a) and Fig. 7 (a), the proposed ILFD with a tuning mechanism can operate from 26.1-33.0 GHz and 27.0-38.0 GHz as a single divide-by-6 prescaler divider for 1.0-V and 1.2-V supply respectively which can cover the whole 7-GHz bandwidth of 60GHz PLLs proposed in [2]-[3] and directly down convert



(a)



(b)

Fig.6. Measured input sensitivity curve of (a) divide-by-6 (b) divide-by-4 of the proposed ILFD with a 1.0-V supply

TABLE I PERFORMANCE COMPARISON WITH THE-STATE-OF-THE-ART DIVIDE-BY-6 AND DIVIDE-BY-3 ILFDS

	Features	Division Ratio	Locking Range* (GHz)	Locking Range* (%)	Input power (dBm)	Power (mW)	FoM_1 (%/mW)	FoM_2 (%/(mW)^2)	Area (mm^2)
[13]	Direct mixing	3	21.7-24.9	13.7	0	8.3	1.7	5.1	0.140
[14]	Direct mixing	3	53.9-57.8	7.0	0	4.6	1.5	4.5	0.800
[9]	Direct mixing	6	141.0-144.3	2.7	0	14.0	0.2	1.2	1.160
[10]	Direct mixing	6	10.2-11.3	11.0	2	6.8	1.6	6.1	0.007
[11]	Direct mixing	6	14.6-15.4	5.0	10	12.5	0.4	0.24	0.300
[12]	Current reused ILFD	6	121.0-124.8	3.5	-5	4.5	0.8	14.2	0.140
This	Even-harmonic-enhanced	6	27.7-32.0	**13.2**	0	3.1	4.0	**24.0**	0.002

*without any tuning mechanisms, FoM_1 = (% Lock Range)/(mW Power), FoM_2 = (FoM_1)×(Division Ratio)/(mW Input Power)

output signal to low frequency where digital dividers can operate. This results to a significant power reduction of the entire 60GHz PLL. Similarly, the divide-by-4 operation can be used for a 60GHz frequency synthesizer based on 20GHz sub-harmonic injection proposed in [4]-[5].

Table I compares the proposed even-harmonic-enhanced direct injection ILFD with the state-of-the-art divide-by-6 and divide-by-3 ILFDs. To the best knowledge of the authors', the proposed ILFD can perform a divide-by-6 mode with the widest locking range reported of 13.2% when comparing to other divide-by-6 ILFDs [9]-[12] and as good as divide-by-3 ILFDs [13]-[14]. The proposed ILFDs shows the highest FoM_1 which compare % lock range over one mW power consumption. Moreover, when normalized FoM_1 by including division ratio and effect of injection power as FoM_2, the proposed ILFD shows a better performance over the ILFDs in [9]-[14].

V. CONCLUSION

The ILFD using an even-harmonic-enhanced direct injection is proposed for an enhanced locking range of divide-by-6 and divide-by-4 operations. Moreover, it provides the widest locking range reported for a divide-by-6 operation. This work can be suitable to be integrated in 60GHz PLLs proposed in [2]-[5] for a power reduction.

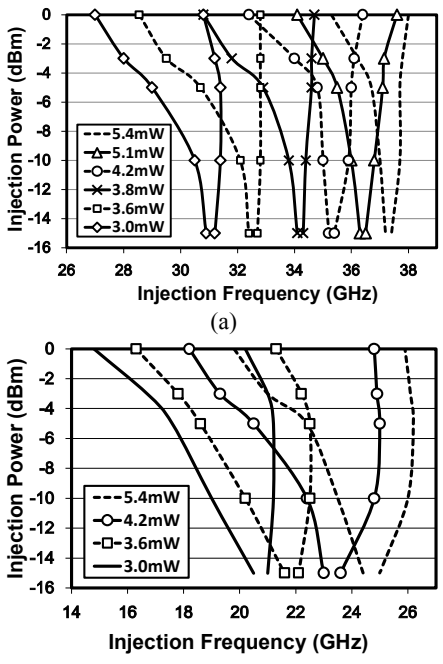


Fig.7. Measured input sensitivity curve of (a) divide-by-6 (b) divide-by-4 of the proposed ILFD with a 1.2-V supply

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