A 6-bit Subranging ADC using Single CDAC Interpolation

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Outline

- **Background**
- **Interpolation techniques**
- **6-bit, 500 MS/s Subranging ADC**
- **Simulation Results**
- **Conclusion**

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Background

- ADC for mobile applications
  - Low power and small area are required
- ADC in recent scaled process
  - Reduced intrinsic gain of transistor

  ⇒ Comparator based ADCs are growing

Characteristic of comp. based ADCs for 6-bit

	Speed	Core area	Power
Flash	Ultra high	Large	High
Subranging	High	Small	Low
SAR	Low	Medium	Ultra low

Purpose of Research

- **Interpolation technique**
  - **Generate new signal using two certain signals**
  - **Circuit components are reduced**
  - **Reference range is selected automatically**
- **Subranging ADC using interpolation** [1]
  - **Simplified design, high linearity**
  - **Lowest power consumption**
  - **Two CDAC are required ⇒ Need improvement**
- **Realize interpolation using one CDAC**
  - **For low power consumption and small core area**

[1] Y. Asada *et al.*, A-SSCC 2009

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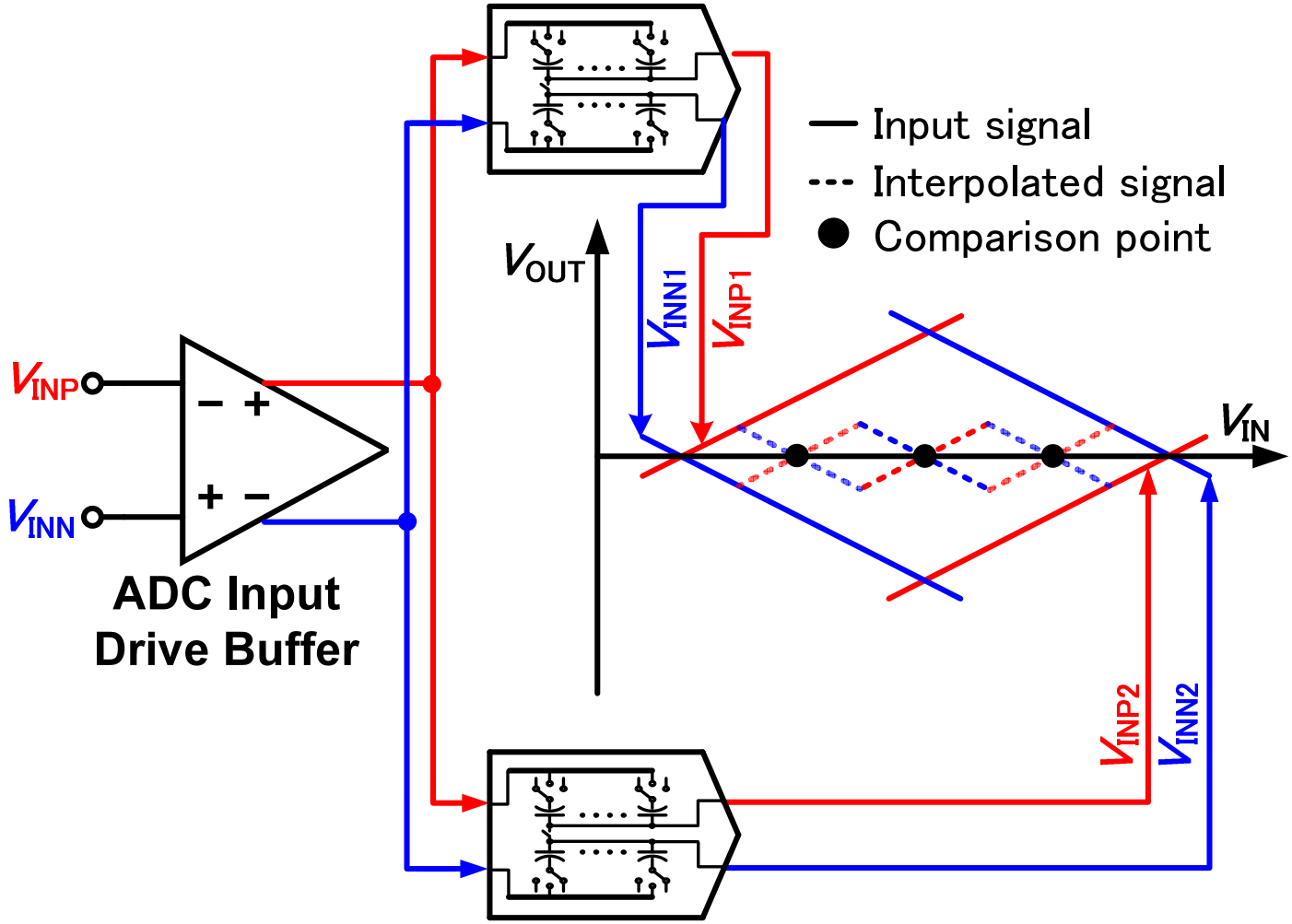
Previous Interpolation

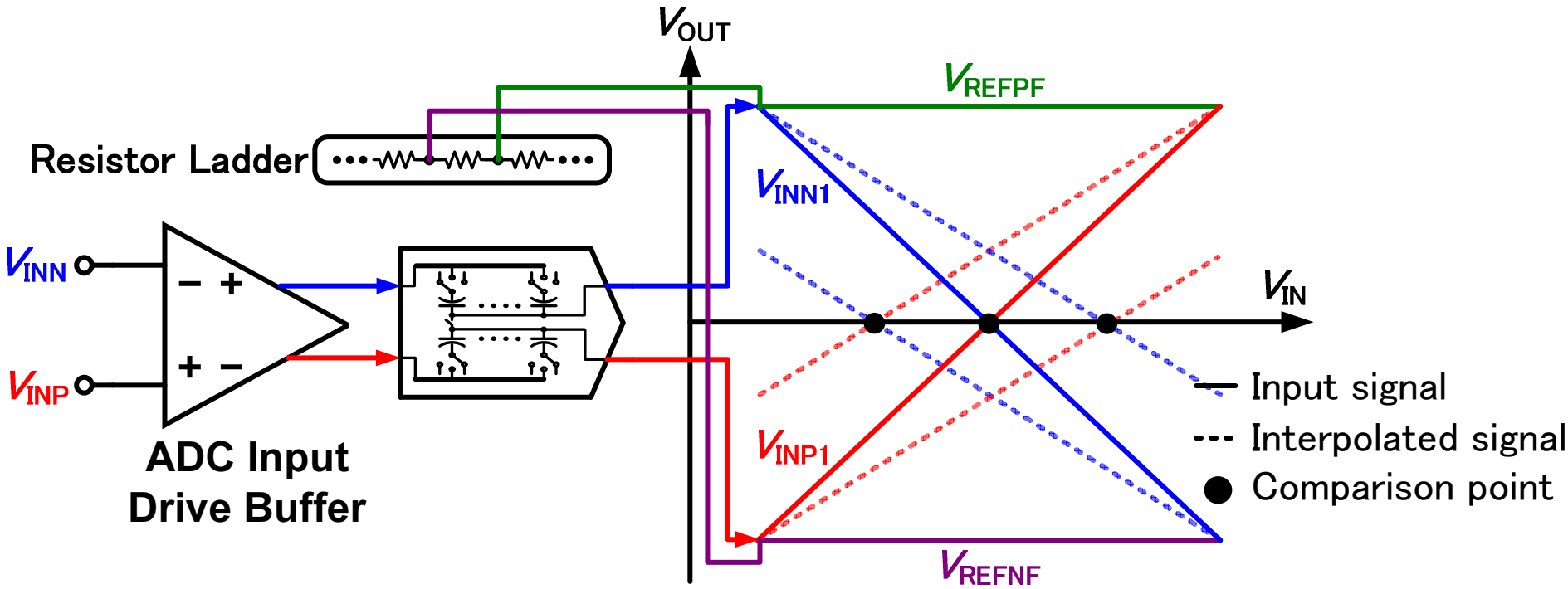
☺ DAC's gain is not problematic

☹ High power, large area, high performance buffer



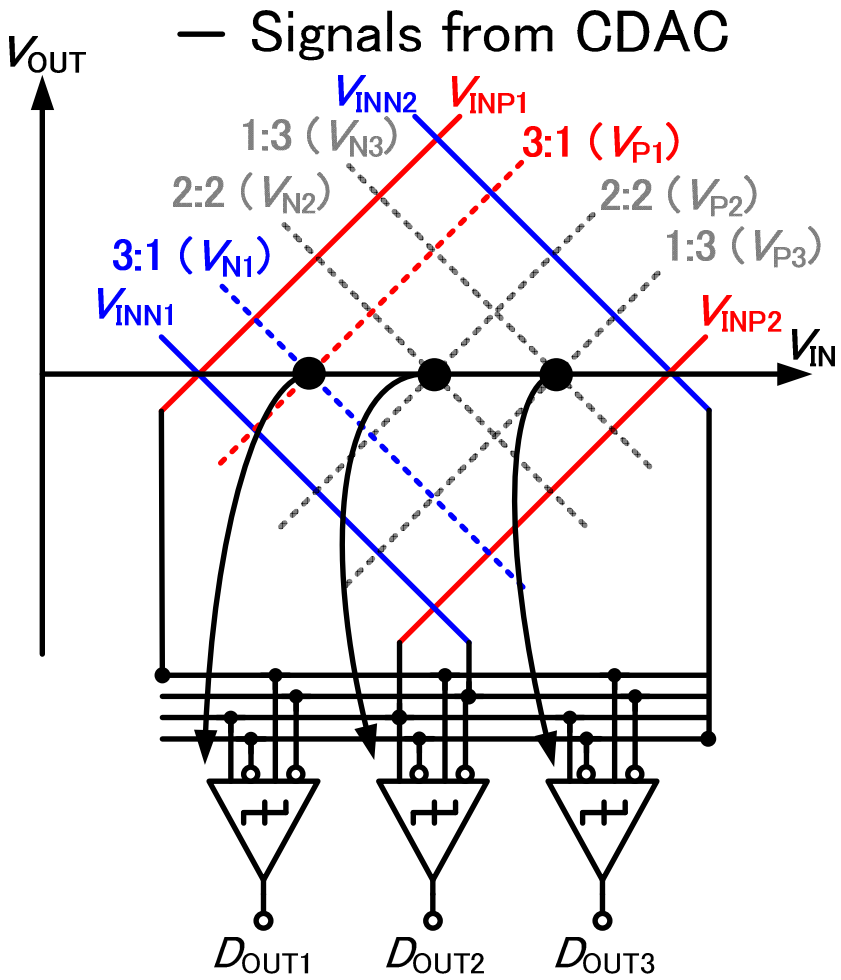
Proposed Interpolation

- Using one differential signal, two DC references
  - Only one CDAC is required
- Power consumption, core area, and sampling capacitance are reduced

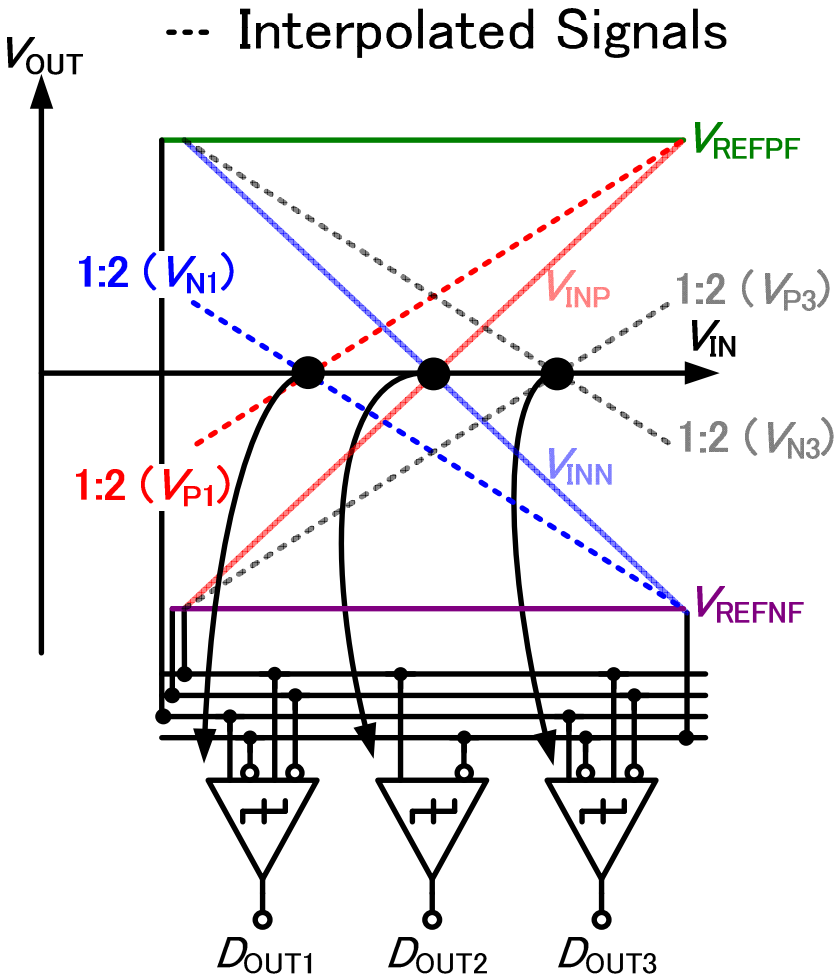


Comparisons of Interpolation

- **Same operation is achieved**



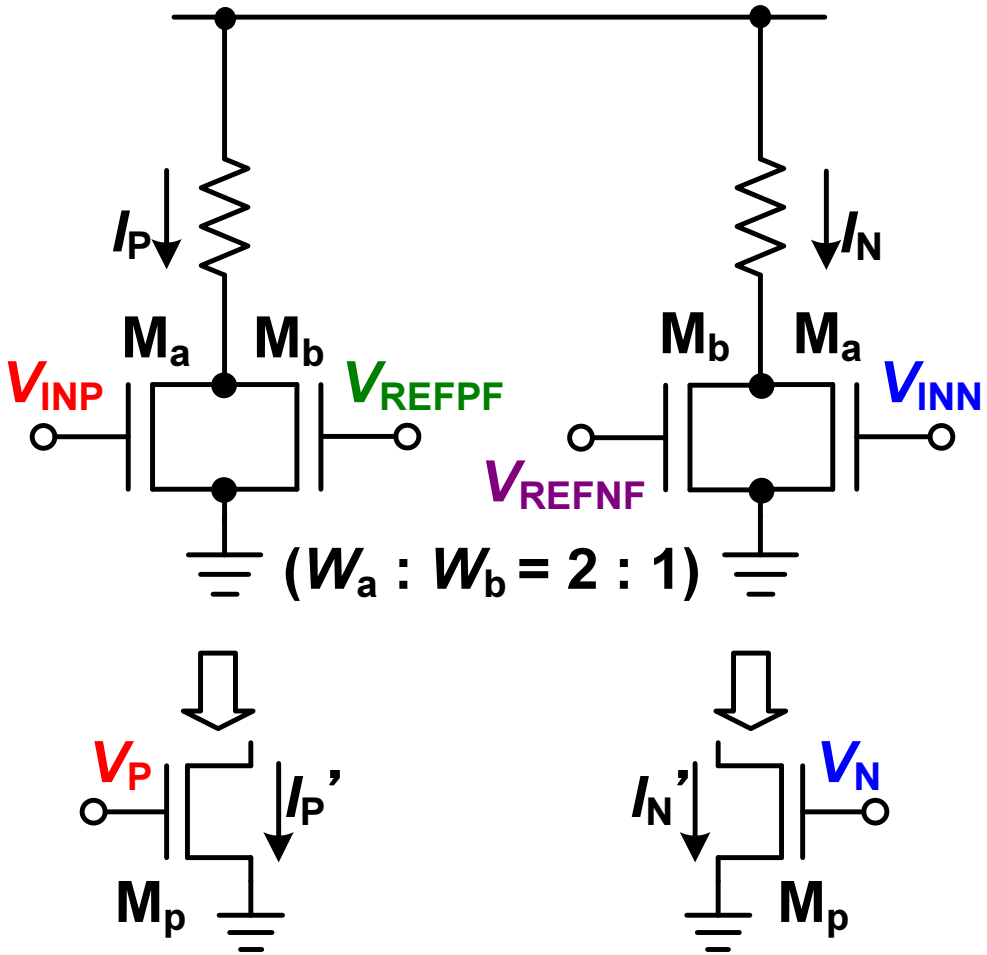
Previous interpolation

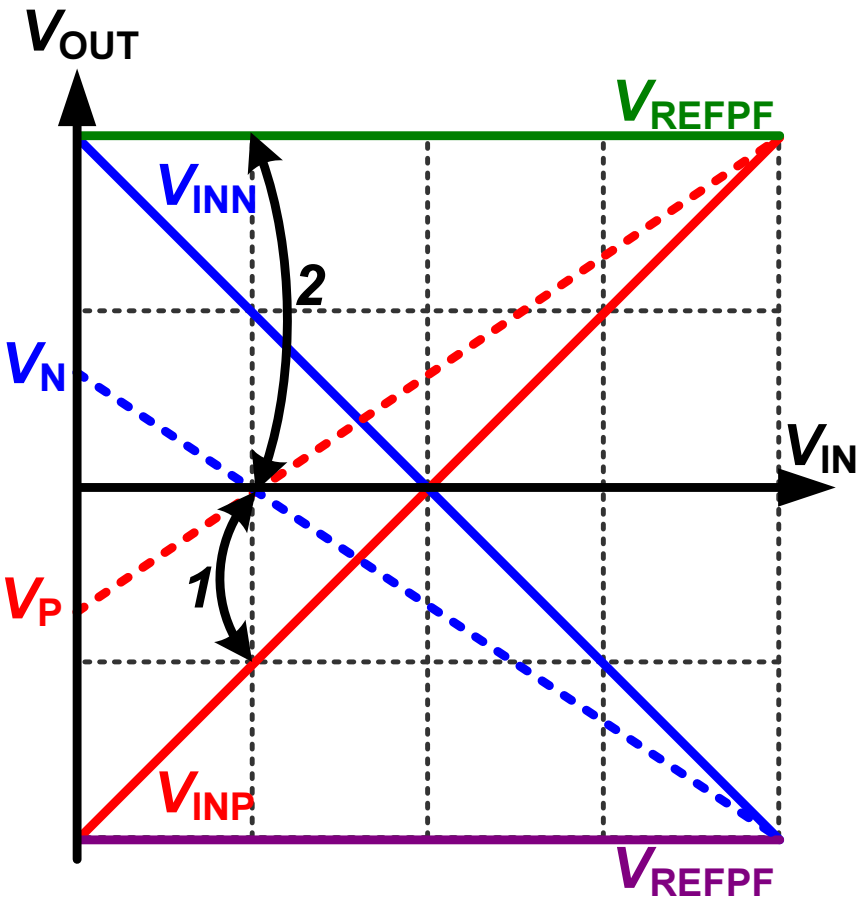


Proposed Interpolation

Gate-Weighted Interpolation

- Gate-weighted TR realize interpolation





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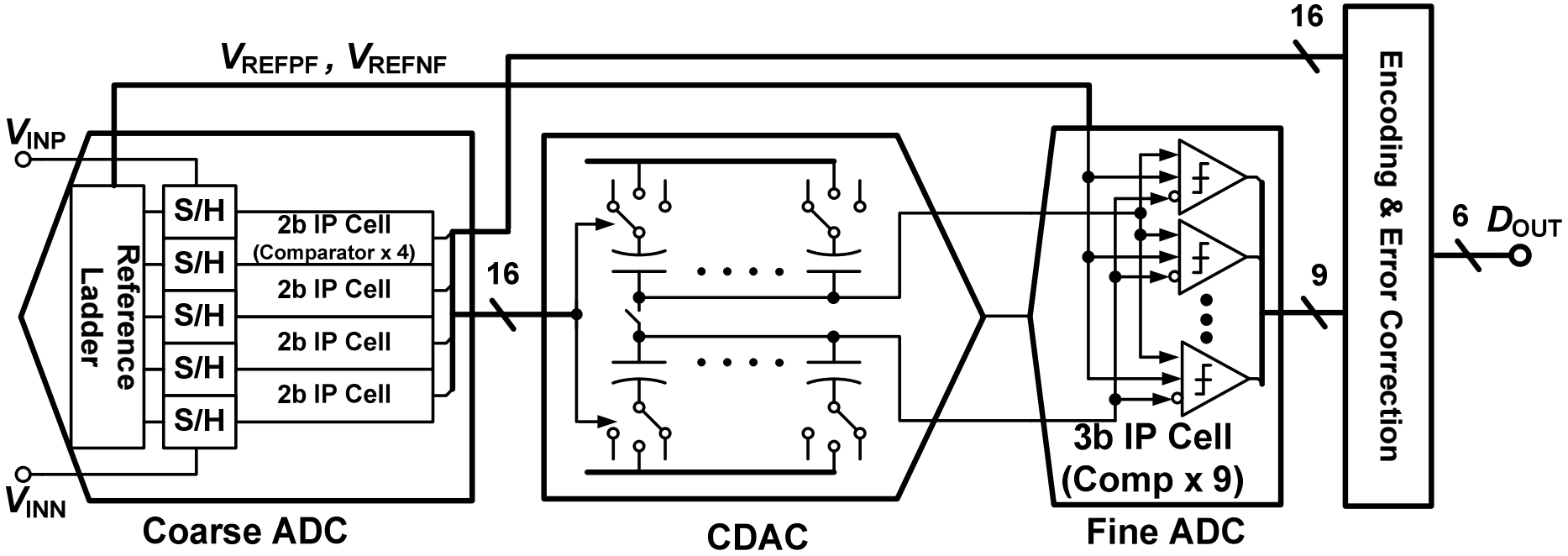
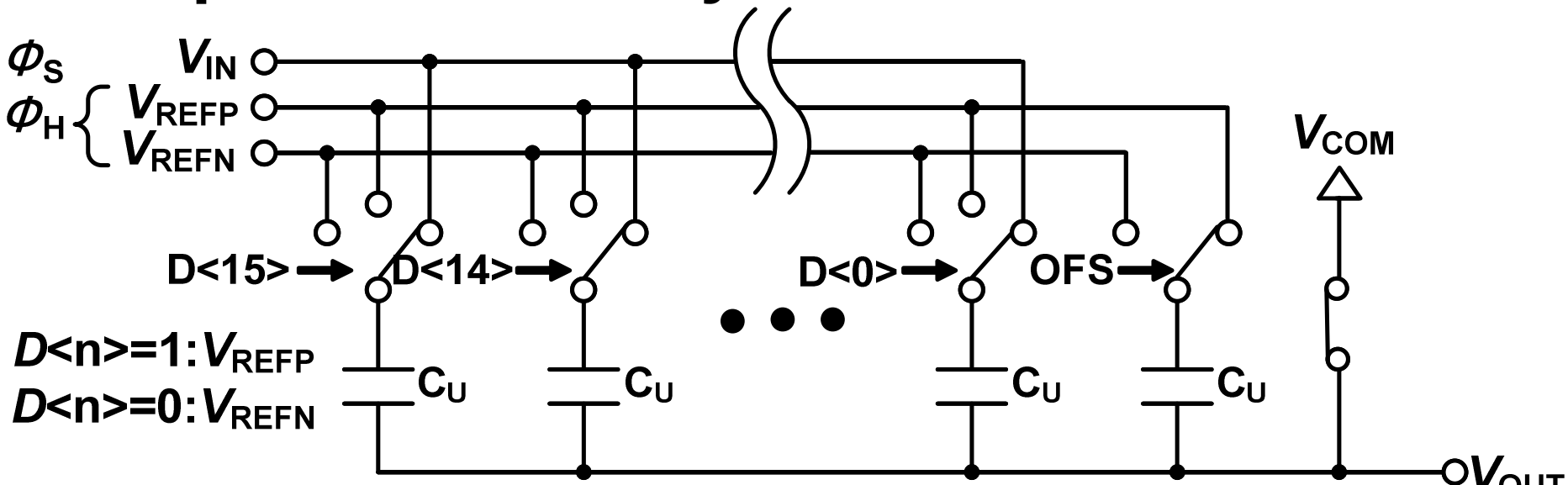
ADC Architecture

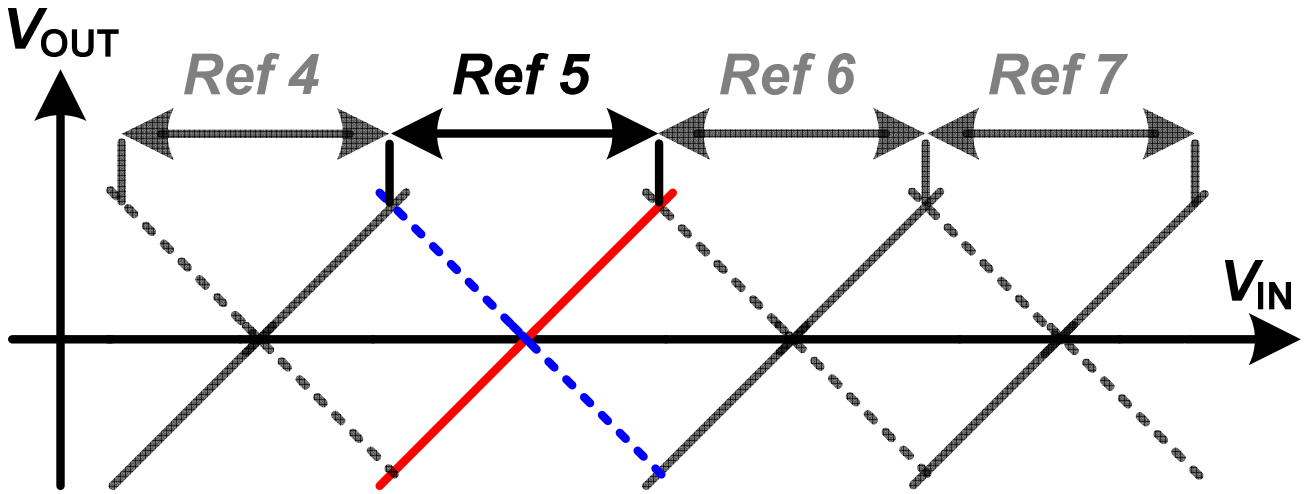
- 4-bit coarse, 3-bit fine stage
  - 1-bit redundancy for error correction
- Only one CDAC
  - DC references from ref. ladder in coarse stage



CDAC Operation

- Output is shifted by sub-ADC's result





V_{REFP} = 6

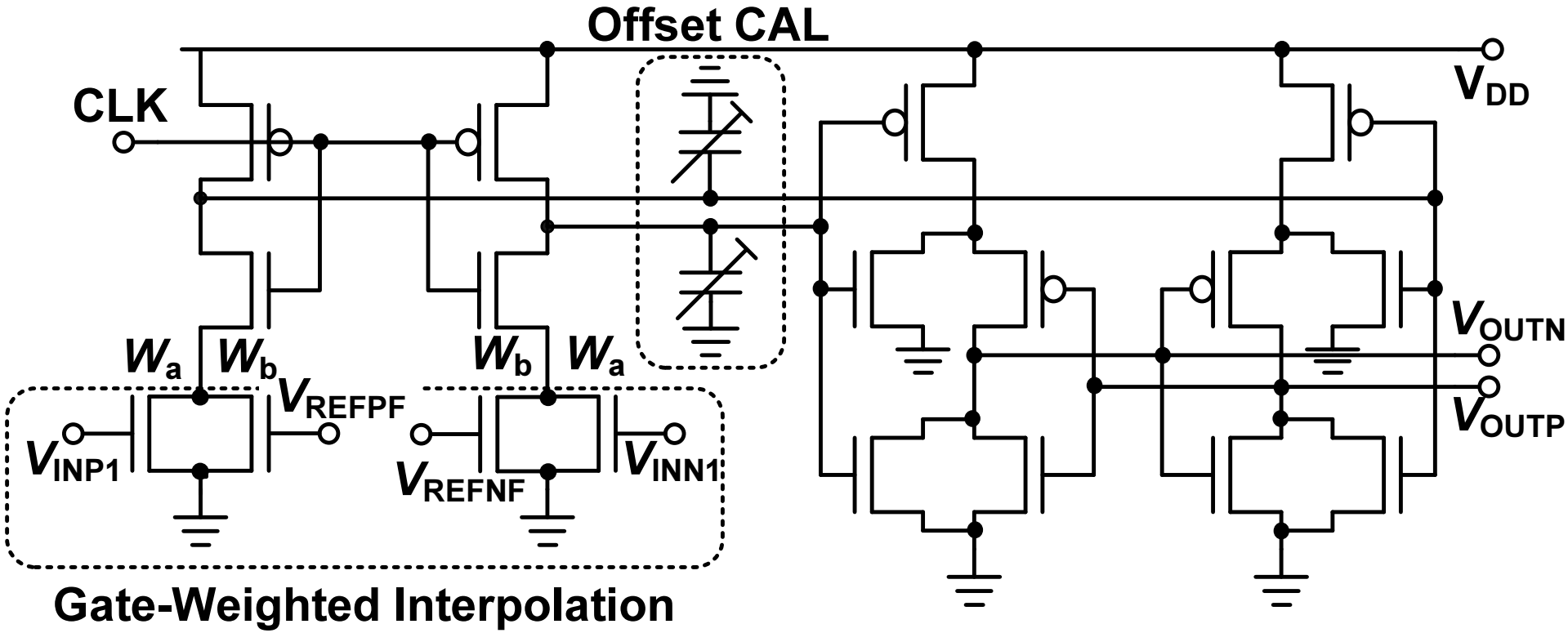
V_{REFN} = 10

Then,

Ref 5

Comparator

- **Based on double-tail latched comparator [2]**
  - **Offset is cancelled by varactors**

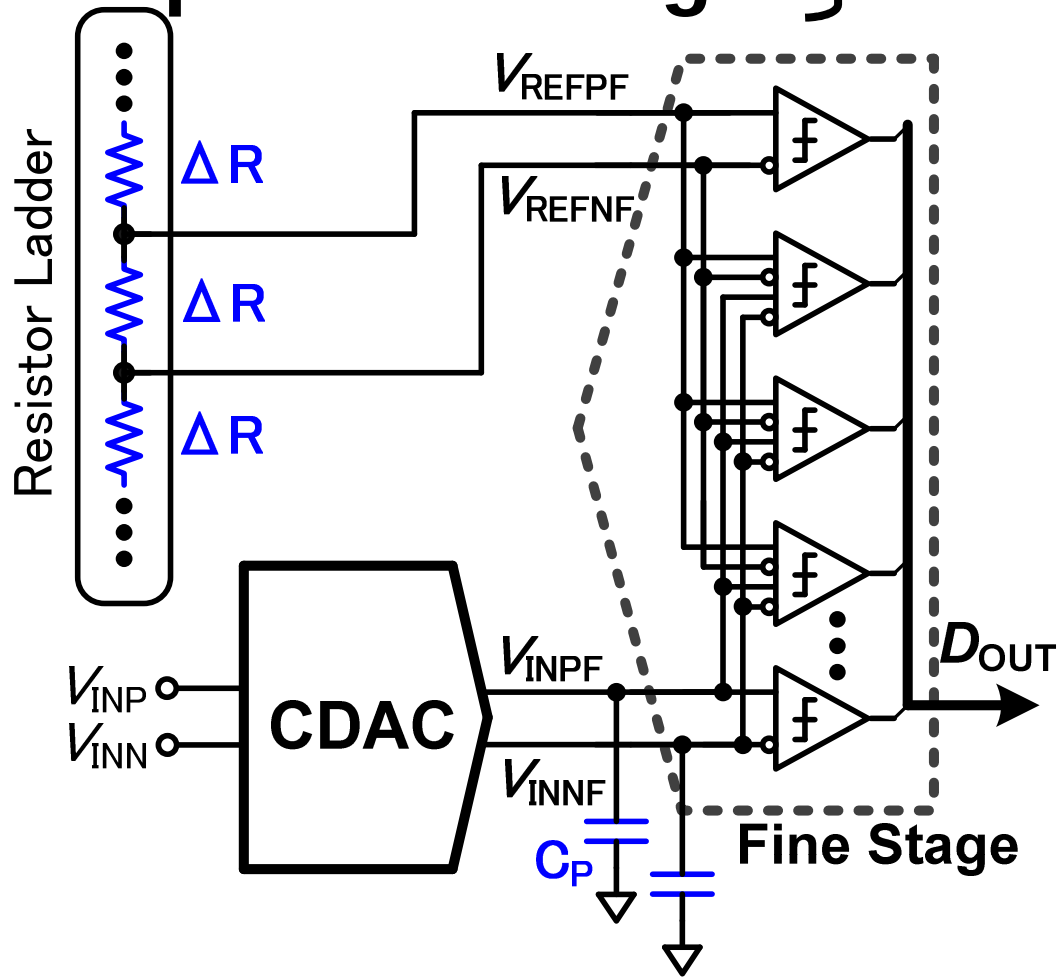


[2] M. Miyahara *et al.*, A-SSCC 2008

Issue of Proposed Interpolation

- Reference voltage variation
- Parasitic cap. in fine stage

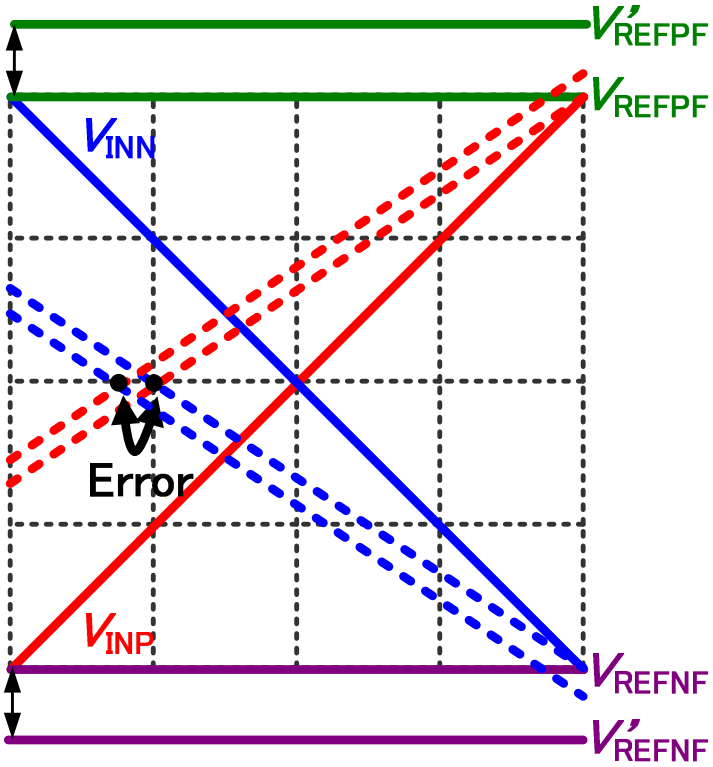
DNL Error

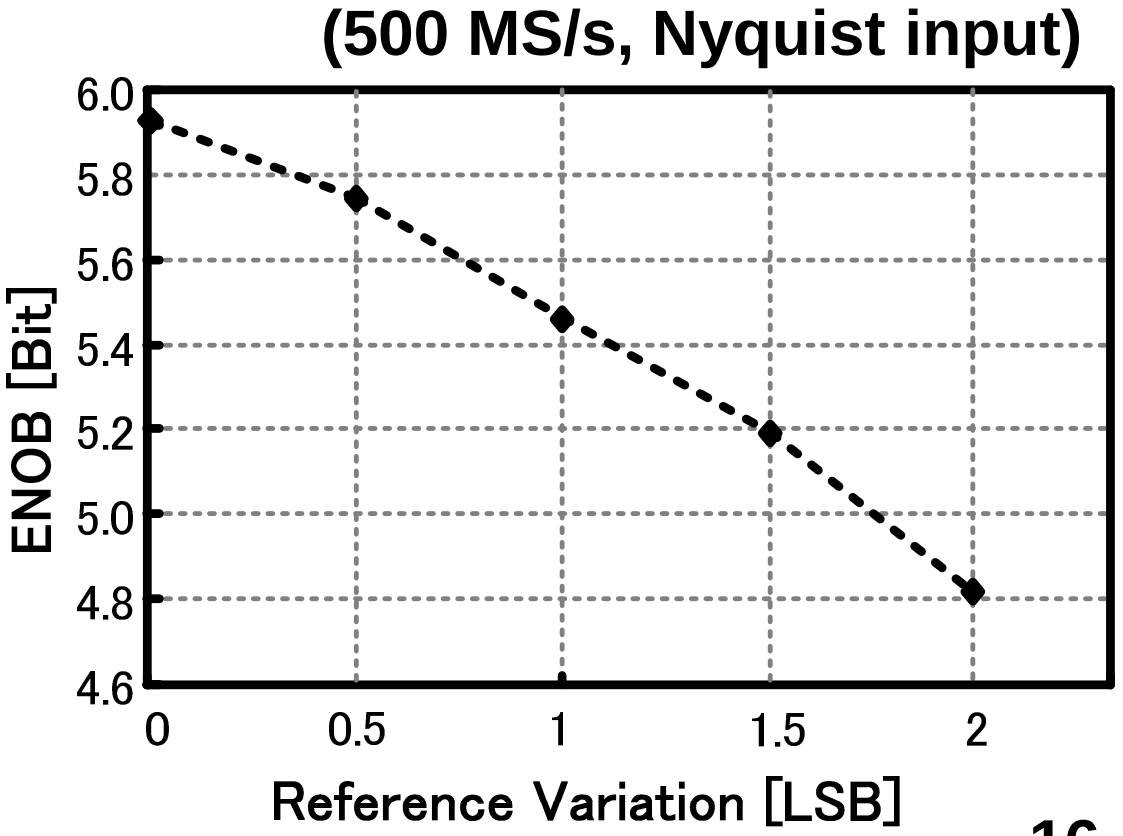


Effect of Reference Variation

- To achieve 0.2-bit ENOB degradation,

  ⇒ ΔRef. should be lower than 0.5-LSB





- Simulation conditions are described in DNL / INL results slide

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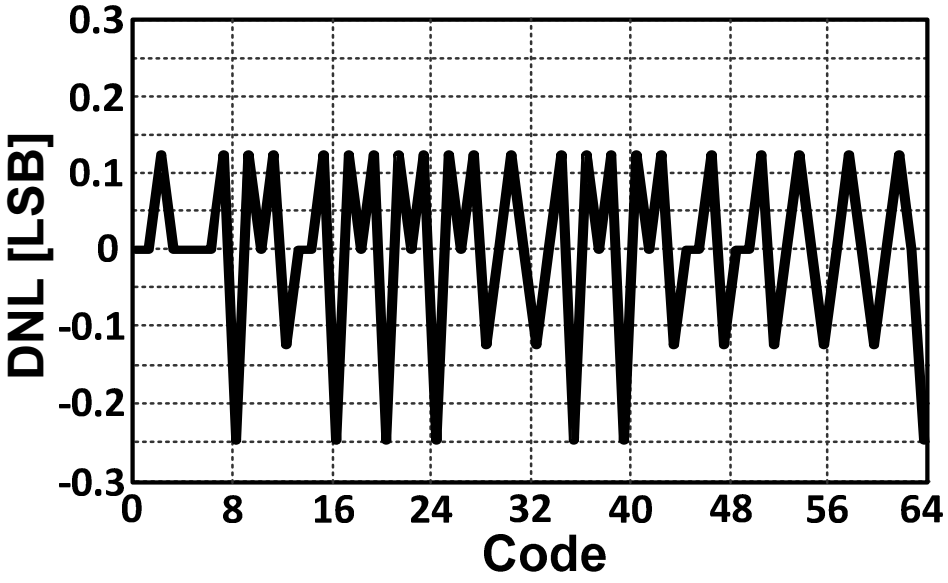
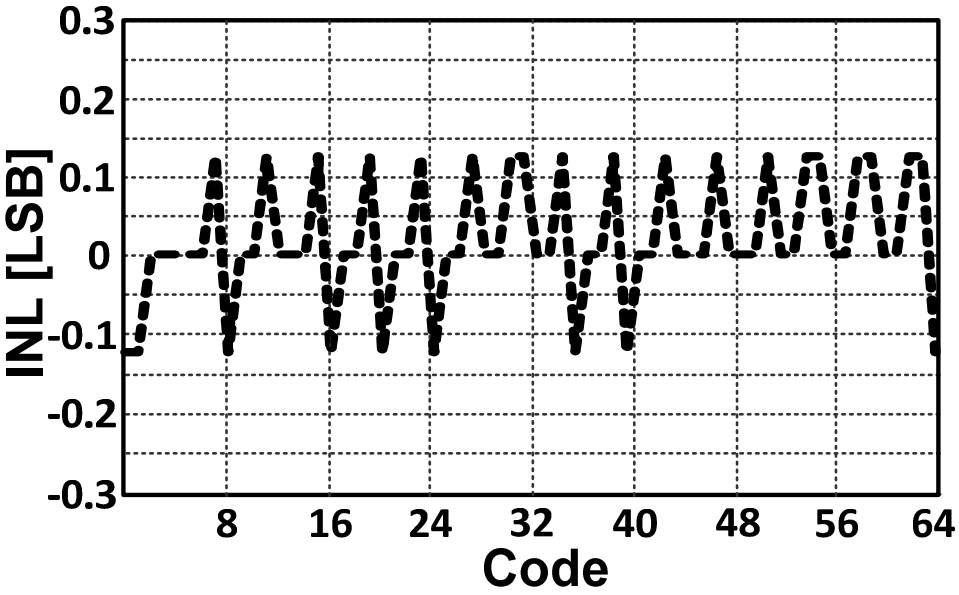
DNL / INL Simulation Results

- DNL: +0.15 / -0.25
- INL: +0.15 / -0.15

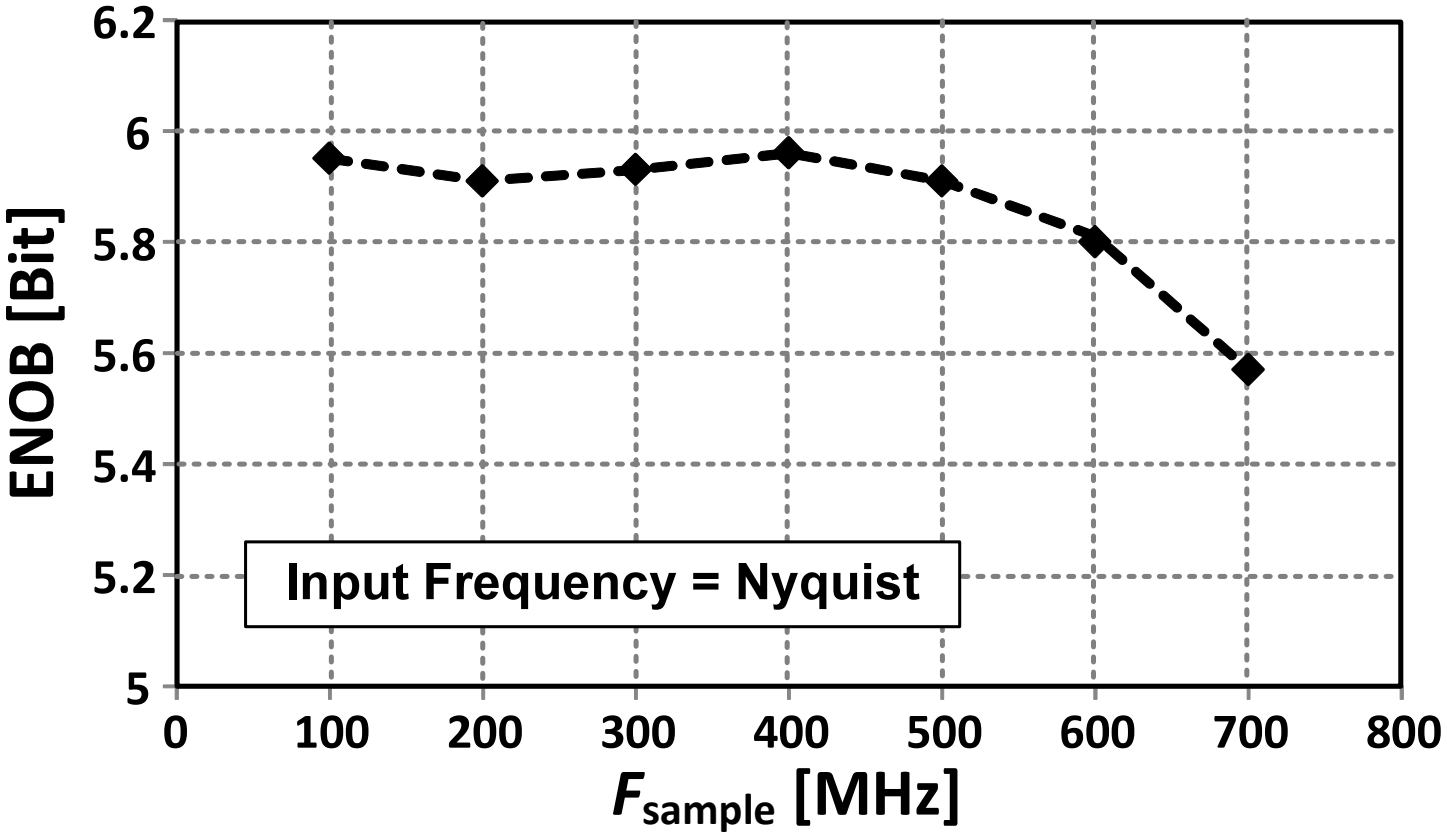




- All transistor model
- Sampling speed: 500 MHz / Data points: 512
- Room temperature
- Including transient noise, without component mismatch

ENOB vs. F_S Simulation Result

- ENOB keeps higher than **5.9-bit until 500 MS/s**



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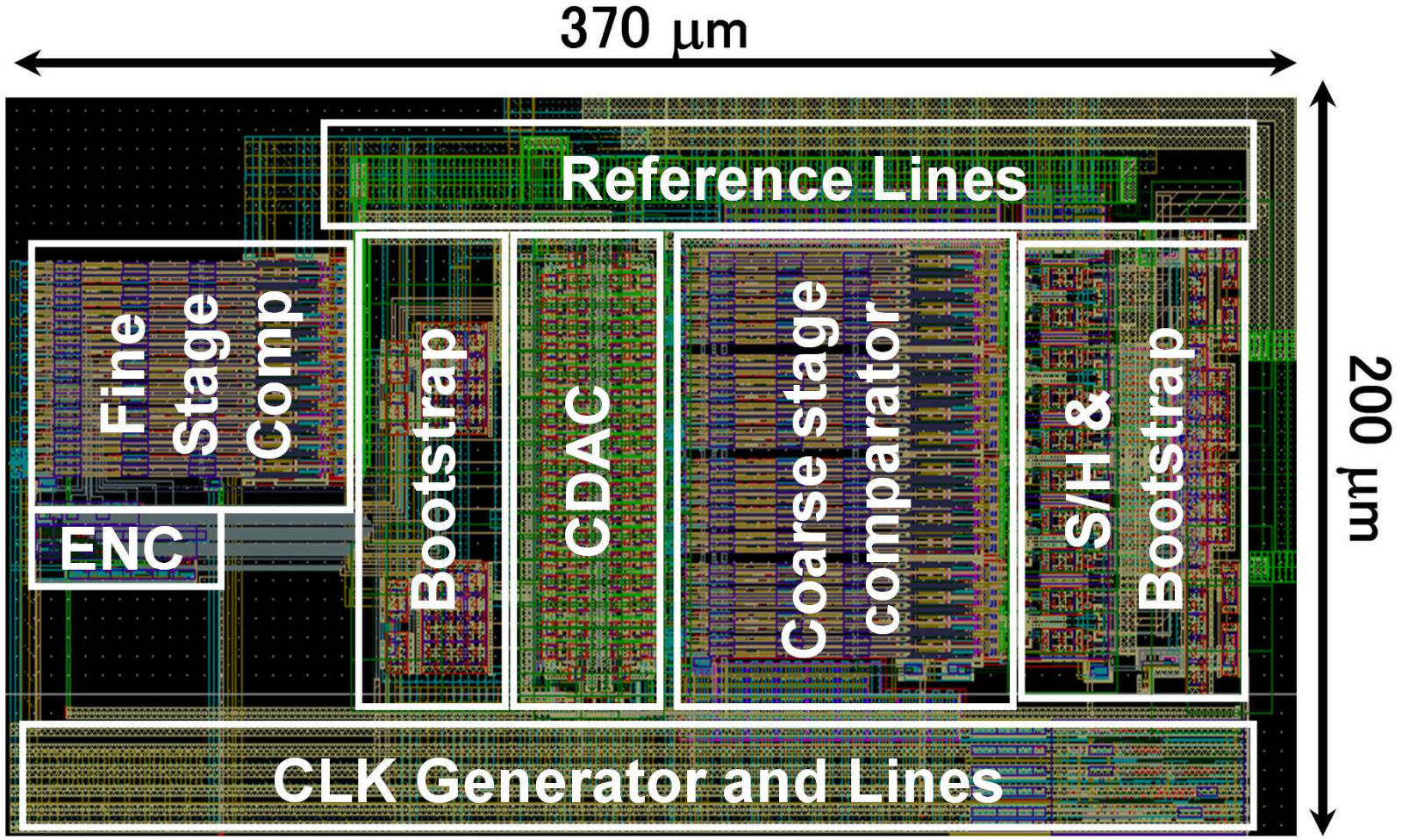
ADC Core Layout

- ADC is designed by 1P9M 90 nm process
- Core area is 0.074 mm^2



Performance Comparison Table

- **Recent published 6-bit ADCs**

Reference	Process [nm]	F_{sample} [GS/s]	P_d [mW]	SNDR [dB]	FoM [pJ/conv.]	Core Area [mm^2]
[1]	90	0.7	7	35	0.25	0.13
[3]	45	1.2	28.5	36	0.45	0.1
[4]	65	1	6.27	31.5	0.21	0.11
[5]	40	2.2	2.6	31.6	0.04	0.03
This Work (Sim.)	90	0.5	3.3	36	0.12	0.074

[3] P. Veldhorst, *et al*., ESSCIRC 2009. [4] J. Yang, *et al*., JSSC 2010.
[5] B. Verbruggen, *et al*., JSSC, 2010.

Comparison with Previous Version

- **Sampling Cap., power consumption (FoM), core area are improved**
  - **Speed is reduced due to no interleaving**

Reference	C_{sample} [pF]	F_{sample} [GS/s]	P_d [mW]	FoM [pJ/conv.]	Core Area [mm^2]
[1] (Previous Work)	2.7	0.7	7	0.25	0.13
This Work (Sim.)	1.7 (↓38%)	0.5 (↓29%)	3.3 (↓53%)	0.12 (↓52%)	0.074 (↓43%)

Previous work: Subranging using two CDAC interpolation

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Conclusion

- **Interpolation using one diff. signal and two ref. voltages has been proposed**
- **6-bit, 500 MS/s, 3.3 mW ADC has been designed**
  - **Sampling capacitance (↓38%)**
  - **Power consumption (↓53%)**
  - **Core area (↓43%) (compared with previous ADC)**
  - **Speed can be improved with interleaving**

Acknowledgement

This work was partially supported by NEDO, MIC, CREST in JST, STARC, Berkeley Design Automation for the use of the Analog Fast SPICE (AFS) Platform, and VDEC in collaboration with Cadence Design Systems, Inc. and Huawei.

Thank you for your interest!

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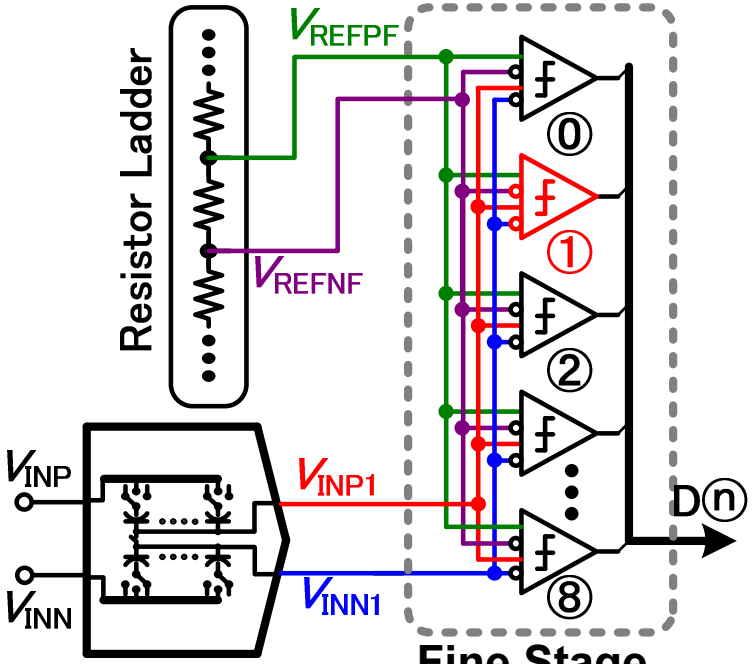
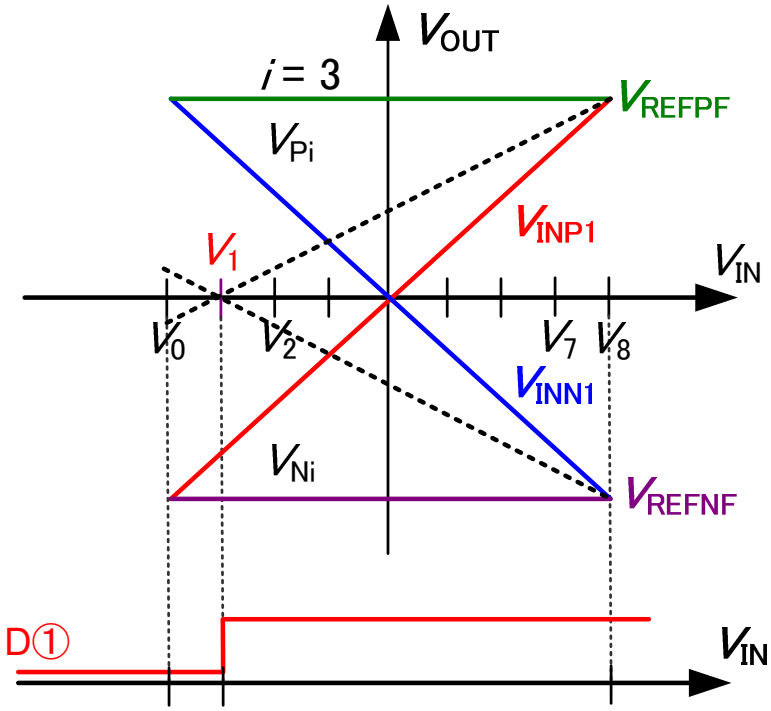
CDAC and Fine Stage Operation

- $V_{IN} < V_1$: $V_{Ni} > V_{pi}$ ⇒ Comp_out = Low
- $V_{IN} > V_1$: $V_{Ni} < V_{pi}$ ⇒ Comp_out = High



Fine Stage
(3-bit interpolation)

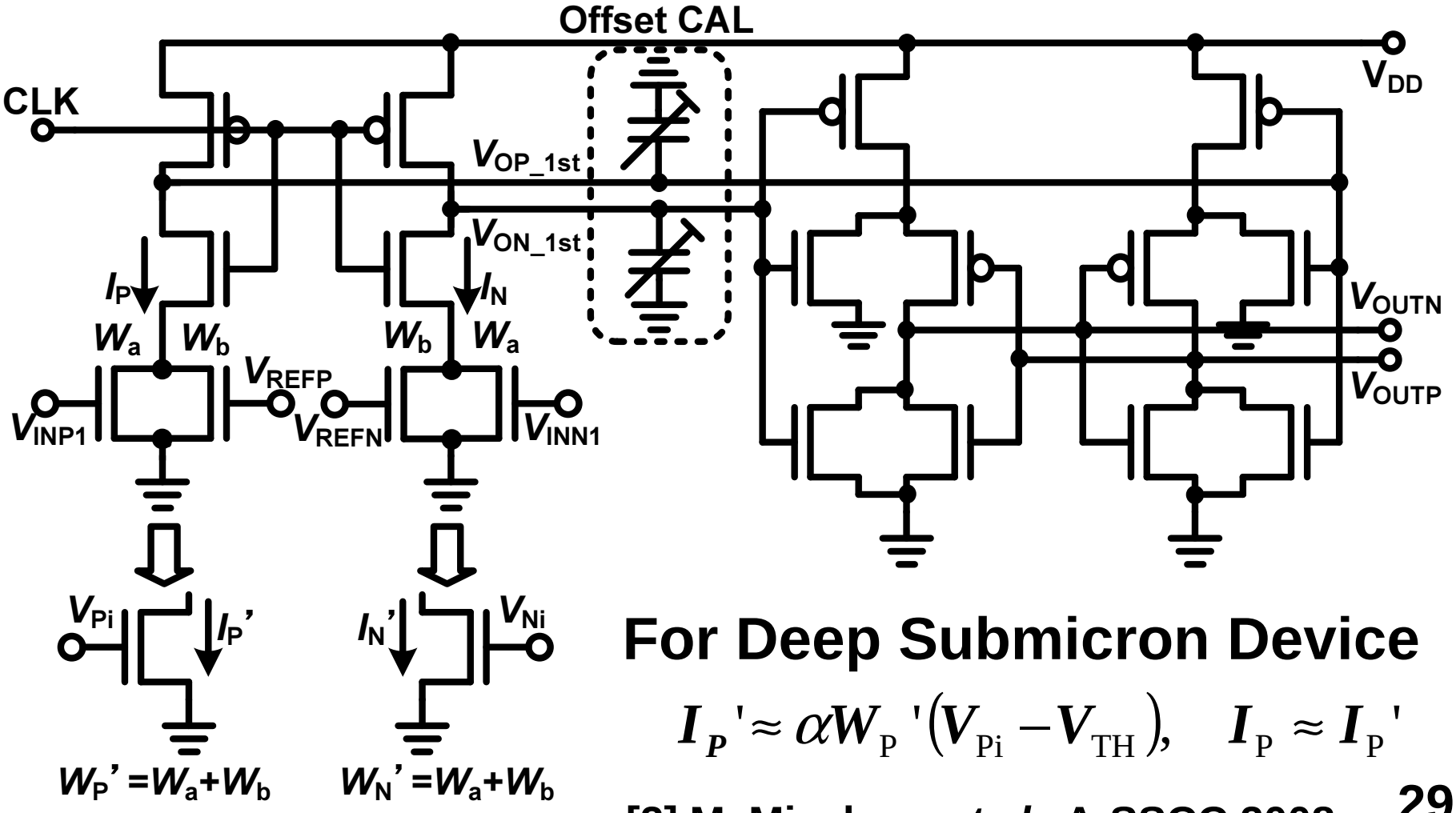


(i : 1~4)

$$V_{Pi} = \frac{iV_{REFPF,NF} + 4V_{INP1}}{(i+4)}, \quad V_{Ni} = \frac{iV_{REFNF,PF} + 4V_{INN1}}{(i+4)}$$

Gate-weighted Interpolation

- **Based on double-tail latch comparator [2]**



For Deep Submicron Device

$$I_P' \approx \alpha W_P' \left(V_{Pi} - V_{TH}\right), \quad I_P \approx I_P'$$

[2] M. Miyahara *et al.*, A-SSCC 2008