A 6-bit Subranging ADC with Single CDAC Interpolation

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***Abstract*—In this paper, a 6-bit subranging Analog to Digital Converter (ADC) using a new interpolation method is presented. The proposed interpolation method utilizes one differential input signal and two DC voltages. Therefore, the area of Digital to Analog Converter (DAC) is reduced half in comparison to the previous interpolation which utilizes two differential signals. The ADC is implemented in 90 nm process and achieves total power of 3.3 mW, ENOB of 5.8-bits, FoM of 0.12 pJ/conv. at 500 MS/s in simulation.**

Keywords—ADC, Subranging, interpolation

I. INTRODUCTION

Medium resolution, several hundred MS/s to several GS/s ADCs are widely used in wideband receivers. Meanwhile, low-power consumption is becoming the most important characteristic by growing demand for mobile devices, such as smartphone. A subranging ADC using interpolation [1-2] is one of the good candidates to satisfy the performance requirement. However, traditional interpolation utilizes two DACs for its analog to digital conversion operation. Those DACs reduce the ADC's attractiveness because of large power and area consumption. This paper presents a subranging ADC with interpolation using one differential signal and two DC reference voltages. By using the proposed interpolation, the DAC becomes half from the previous interpolation. Therefore, it benefits the ADC performance, such as power consumption and core area.

II. INTERPOLATION METHODS

A. Interpolation by two differential signals

The subranging ADC is divided into two parts, a coarse ADC and a fine ADC. The coarse ADC decides the MSB side and the fine ADC decides the LSB side. The DAC is located between two ADCs to output signals for the fine conversion. There are several methods to realize a DAC. Among those methods, a capacitive DAC (CDAC) with interpolation has many advantages. Fig. 1 shows CDAC architecture and its output signals. During sampling phase, CDACs charge input signal into unit capacitors. After that, during interpolating phase, CDACs outputs two differential signals for interpolation in the fine ADC. By using the CDAC, low power consumption is achieved because of no DC current path in the circuit. Also, good consistence in the fine conversion range is achieved by CDAC and interpolation. However, the input capacitance and the circuit size become large due to a large number of unit capacitors and two DACs are required for the interpolation.

B. Interpolation by one differential signal

Fig. 2 shows the operation of the two interpolation methods. Basically, an interpolation means dividing between two signals with a certain ratio. For example, in Fig. 2. (a), V_{P1} can be generated by dividing V_{INP1} and V_{INP2} with 3:1 ratio. Also, V_{N1} is generated by using V_{INN1} and V_{INN2} in the same way. If the comparator compares those two interpolated signals, the conversion of D_{OUT1} is performed without reference voltages. Two differential signals are required for realizing this operation. The proposed method is shown in Fig. 2. (b). Comparing to the previous method, the proposed method uses only one differential signal and two DC reference voltages. By using 1:3 ratio of V_{REFP} and V_{INP}, and 3:1 ratio of V_{INN} and V_{REFN}, the same operation of the previous method at D_{OUT1} can be performed. This can be realized based on the principle of the interpolation that the source signals for interpolation are not necessary to have the same slope. Even if one signal is changing and the other signal is DC, it can be interpolated without problem. The proposed interpolation can reduce the CDAC in half in comparison to the previous method. Therefore, core area and power consumption are reduced. Furthermore, the required performance of the ADC input driver is reduced because the CDAC also work as a sample and hold circuit.

III. ADC IMPLEMENTATION

Fig. 3 shows a 6-bit subranging ADC architecture using the proposed interpolation. The ADC consists of a 4-bit coarse ADC, a CDAC, a 3-bit coarse ADC, and digital logics. The one bit redundancy is incorporated for error correction. The ADC utilizes only one CDAC by the proposed interpolation. Two DC reference voltages for interpolation are generated by the resistor ladder in the coarse ADC. Comparators in the fine ADC work in the same way as explained in Fig. 2 (b).

IV. SIMULATION, LAYOUT AND PERFORMANCE TABLE

Fig. 4 shows DNL and INL at the 500 MHz sampling frequency. DNL is less than +0.15 / -0.25 and INL is less than +0.15/-0.15. Fig. 5 shows FFT results at 500 MS/s with Nyquist input frequency. The spurious level is lower than -55 dB. Fig. 6 shows layout of the 6-bit subranging ADC using the proposed interpolation. The core area is 0.074 mm^2. The core size can be reduced by the layout optimization. Table I shows a

performance comparison with recently published 6-bit ADCs. This subranging ADC shows a good performance in comparison to the others in the simulation. The sampling speed is slower than others; however, it can be improved by interleaving and circuit optimization. Table II shows the comparison to the ADC using previous interpolation method.

V. Conclusion

In this paper, the interpolation method using one CDAC and subranging ADC is presented. The proposed interpolation has advantages in circuit area, power consumption and ADC driver requirement. The presented ADC using the proposed interpolation method shows good performances, such as a FoM of 0.12 pJ/conv. in simulation.

Acknowledgment

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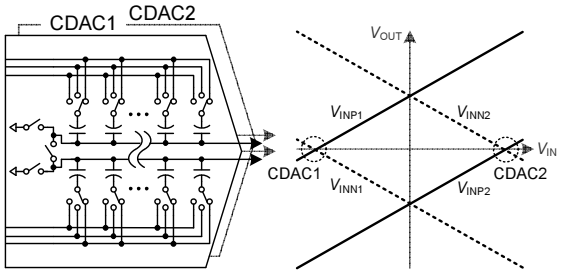

Fig. 1. CDAC architecture and output signals using two differential signals

TABLE I. Recently Published 6-bit ADCs

Reference	Process [nm]	f_{CLK} [Gs/s]	P_d [mW]	SNDR [dB]	FoM [pJ/conv.]	Active area [mm^2]
[2]	90	0.7	7	35	0.25	0.13
[3]	45	1.2	28.5	36	0.45	0.1
[4]	65	1	6.27	31.5	0.21	0.11
[5]	40	2.2	2.6	31.6	0.04	0.03
This Work (sim.)	90	0.5	3.3	36	0.12	0.074

TABLE II. Comparison with Subranging ADC using Two CDACs

Reference	C_{sample} [pF]	f_{CLK} [Gs/s]	P_d [mW]	FoM [pJ/conv.]	Area [mm^2]
[2]	2.7	0.7	7	0.25	0.13
This Work (sim.)	1.7 (↓ 38%)	0.5 (↓ 29%)	3.3 (↓ 53%)	0.12 (↓ 52%)	0.074 (↓ 43%)

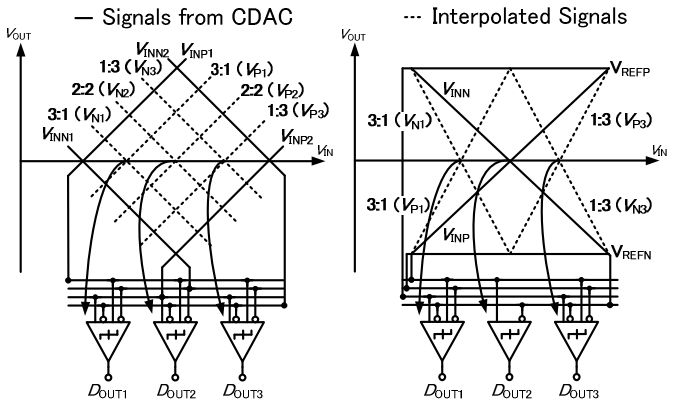

Fig. 2. Comparison of the interpolation methods

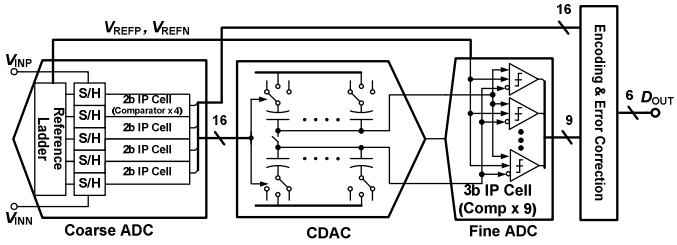

Fig. 3. 6-bit subranging ADC architecture using the proposed interpolation

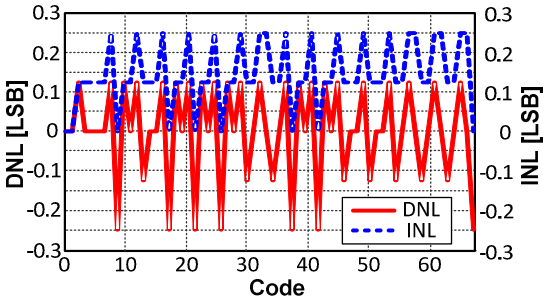

Fig. 4. DNL and INL simulation results at 500 MS/s

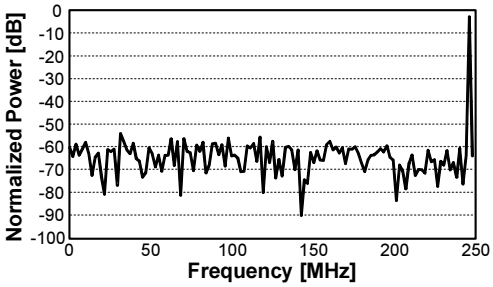

Fig. 5. FFT simulation results at 500 MS/s and Nyquist input

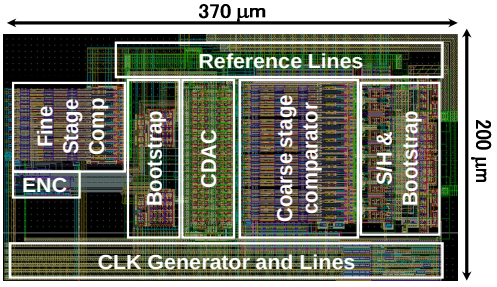

Fig. 6. ADC core layout