A 0.55 V 7-bit 160 MS/s Interpolated Pipeline ADC Using Dynamic Amplifiers

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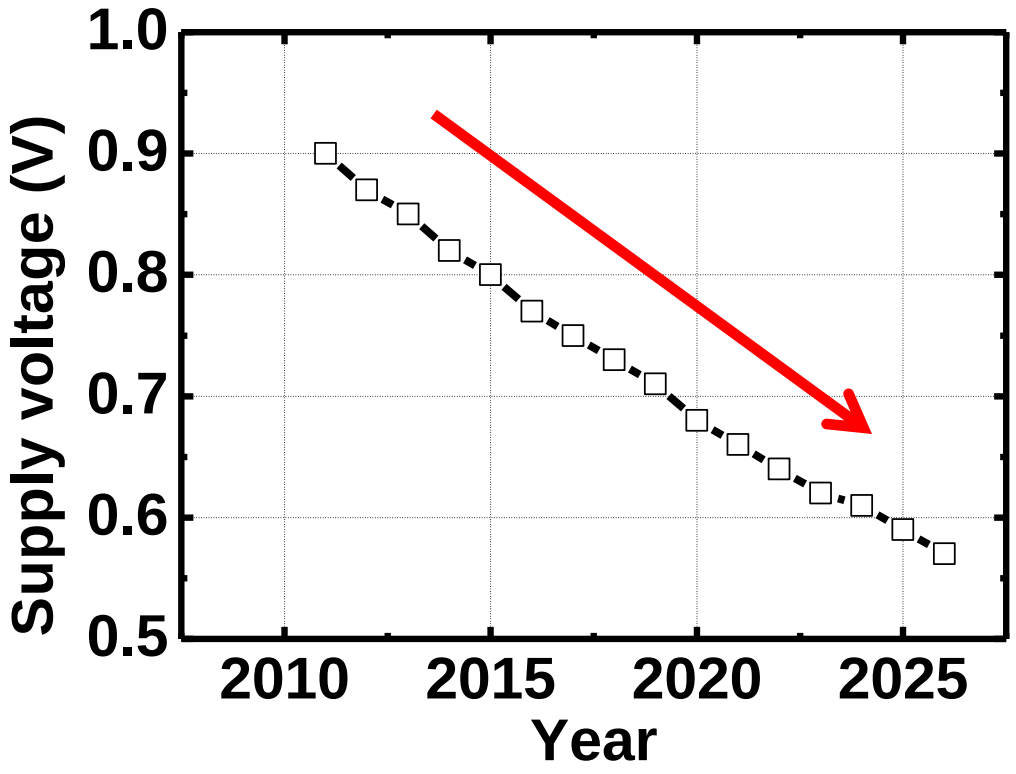
Outline

- **Motivation**
- **Prior Arts**
- **Circuit Design**
- **Measurement Results**
- **Conclusion**

Motivation

- **Ultra-low-voltage (ULV) operation**
  - **Immediate power saving potential**
  - **Explore new circuit techniques for future technology [1]**



Key Challenges

- **Reduced SNR**
- **Reduced headroom**
- **Reduced gain**
- **Increased mismatch**

[1] ITRS, 2011.

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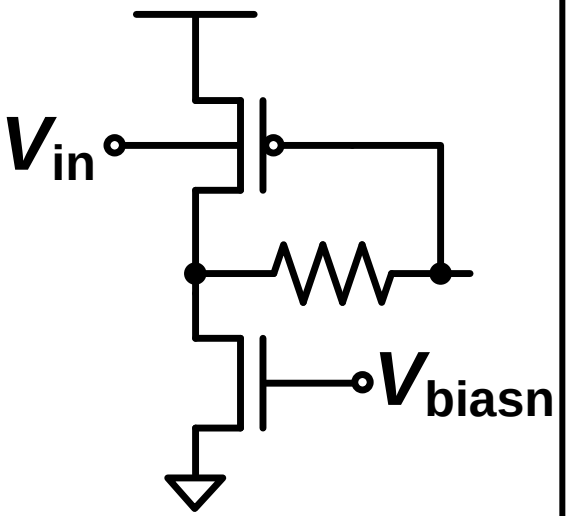
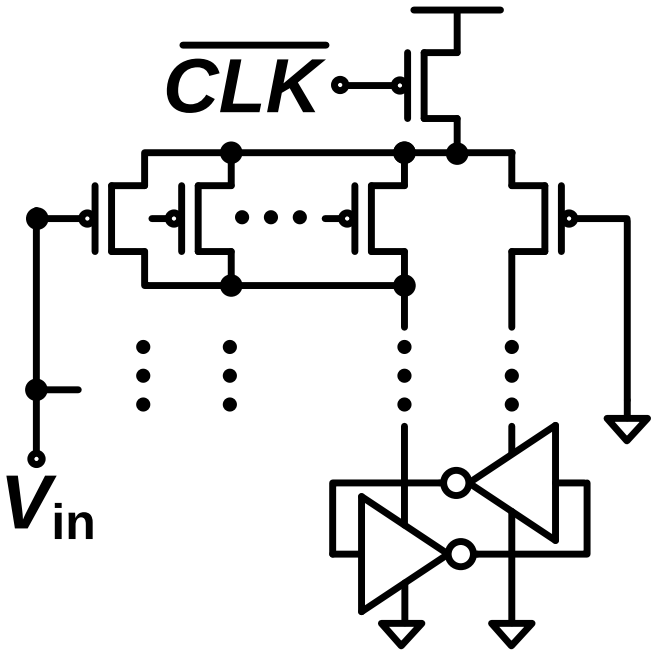
Prior Arts

- **Successfully demonstrated very good energy efficiency → but all suffer in speed**

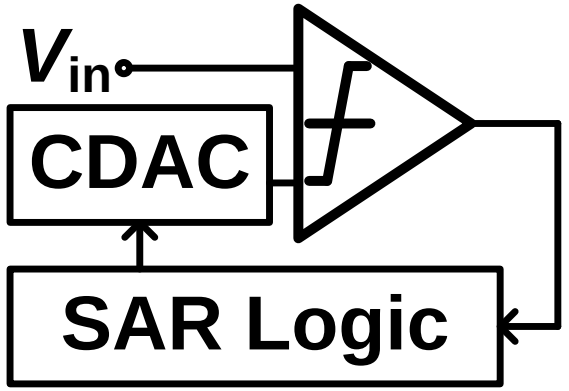
Body-Driven [2]



Sub-threshold [3]



SAR-based [4],[5]



[2] S. Chatterjee *et al*., JSSC 2005.
[3] D. C. Daly *et al*., JSSC 2009.
[4] A. Shikata *et al*., JSSC 2012.
[5] P. Harpe *et al*., ISSCC 2013.

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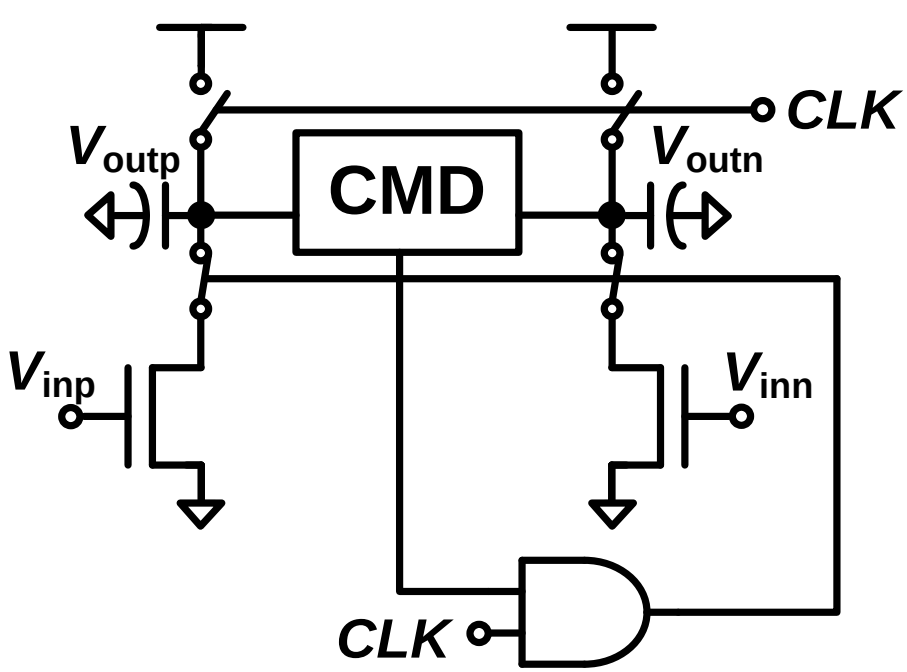
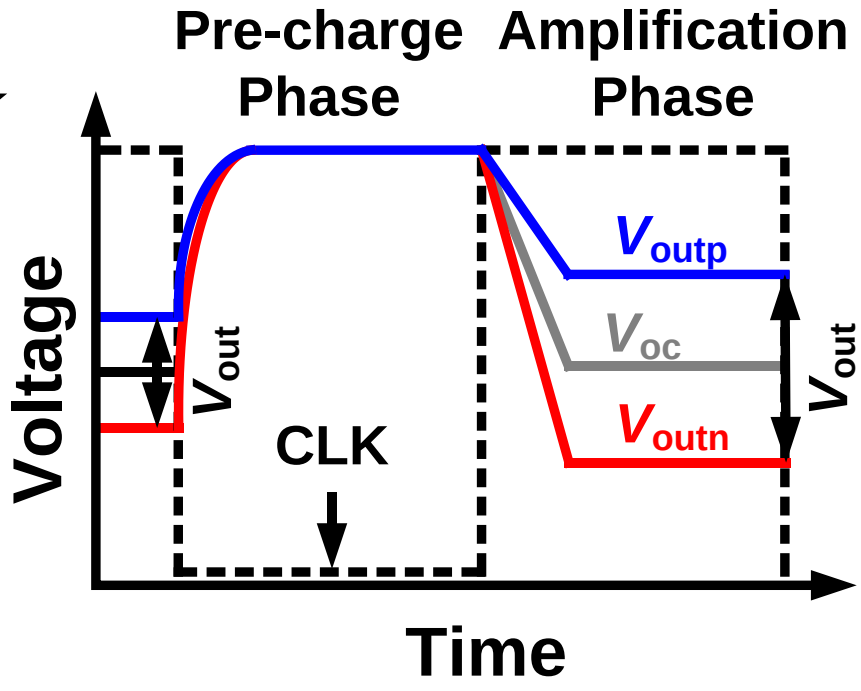
Circuit Techniques Overview

- ADC architecture
- Dynamic amplifier
- Interpolation technique
- Sub-ADC structure
- Self-clocking scheme

Dynamic Amplifier

- **Minimally stacked amplifier achieves high speed at low supply voltage [6]**





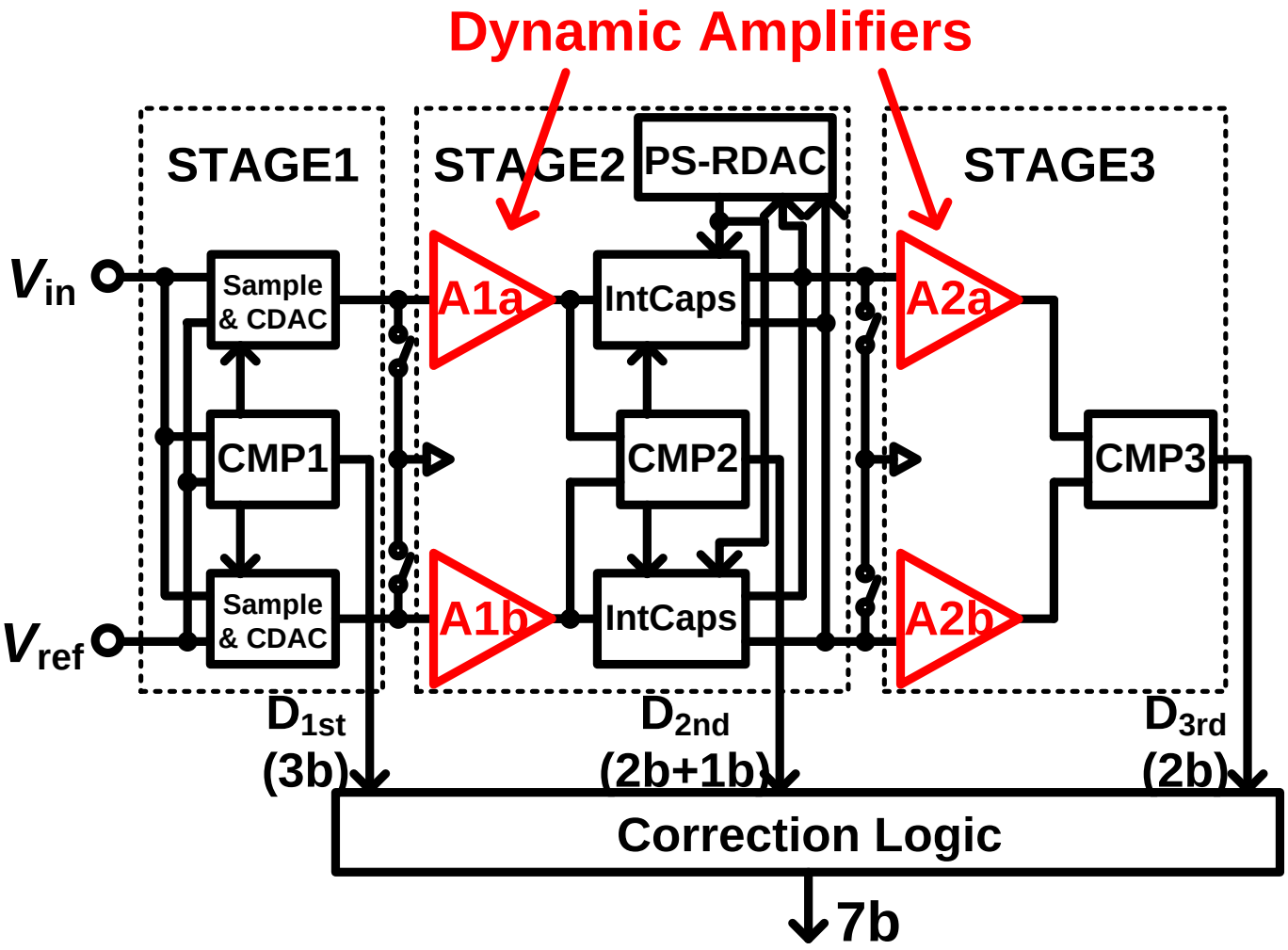
CMD: Common-mode voltage detector

$P_d = fCV_{DD}^2$

[6] J. Lin, *et al.*, ISCAS 2011.

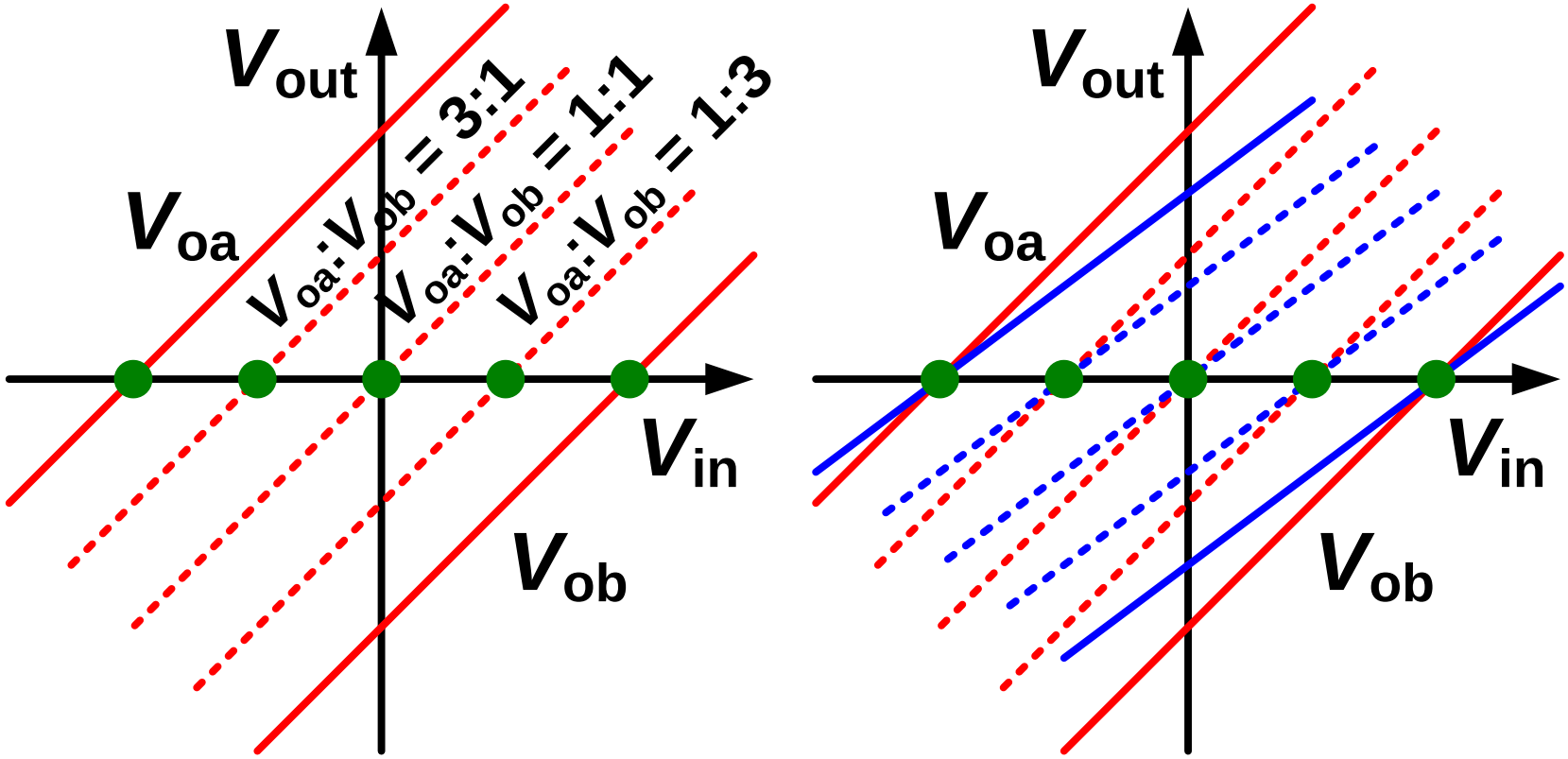
ADC Block Diagram

- **Ultra-low-voltage interpolated pipeline ADC**



Interpolation Technique

- **Interpolation shifts the gain requirement: absolute → relative gain accuracy [7], [8]**

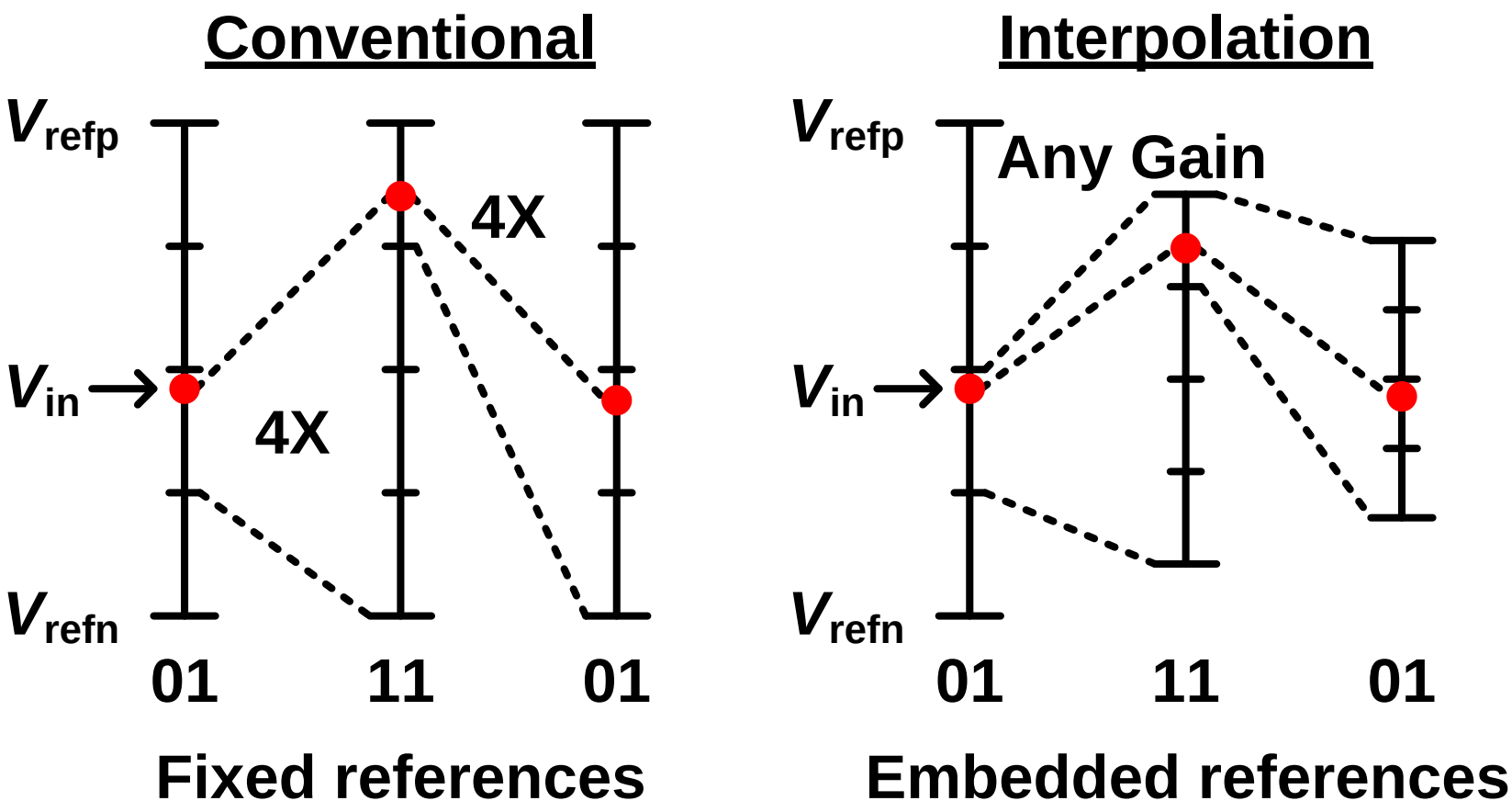


Different absolute gain, same decision levels!

[7] A. Matsuzawa, *et al.*, ISSCC 1990. [8] C. Mangelsdorf, *et al.*, ISSCC 1993.

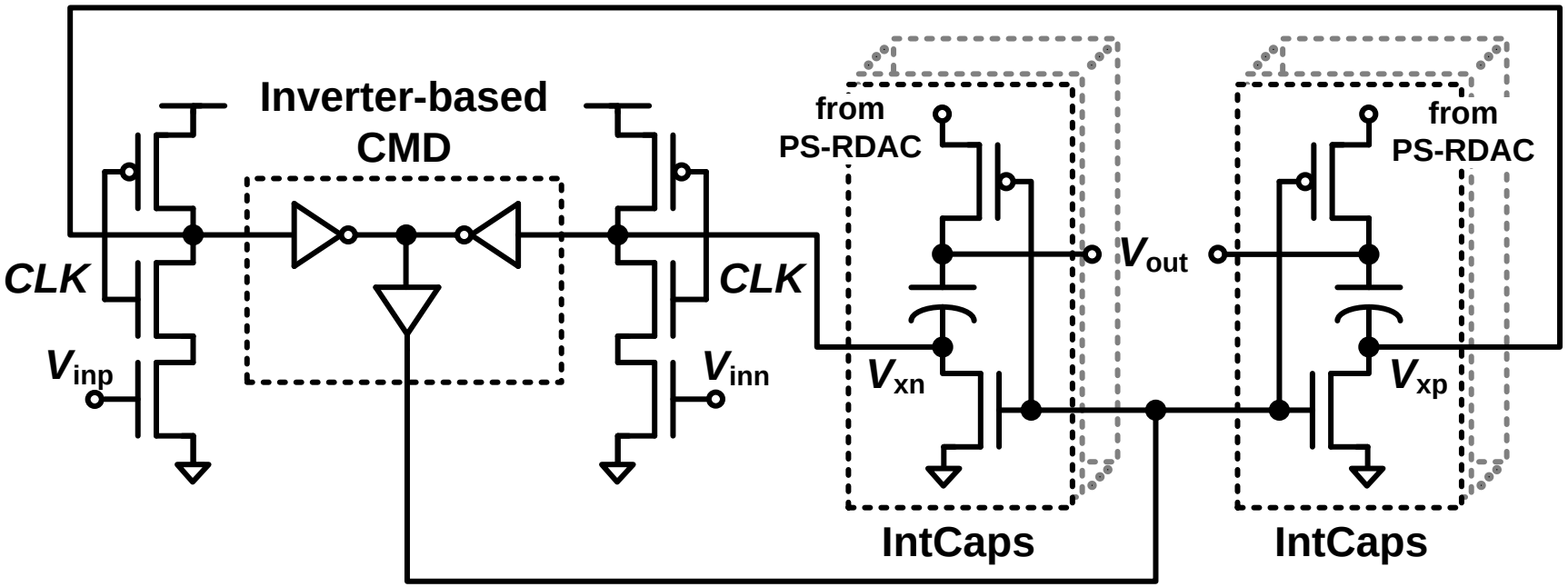
Interpolated Pipeline

- **Same path for both signal and references**



High-Speed Dynamic Amplifier

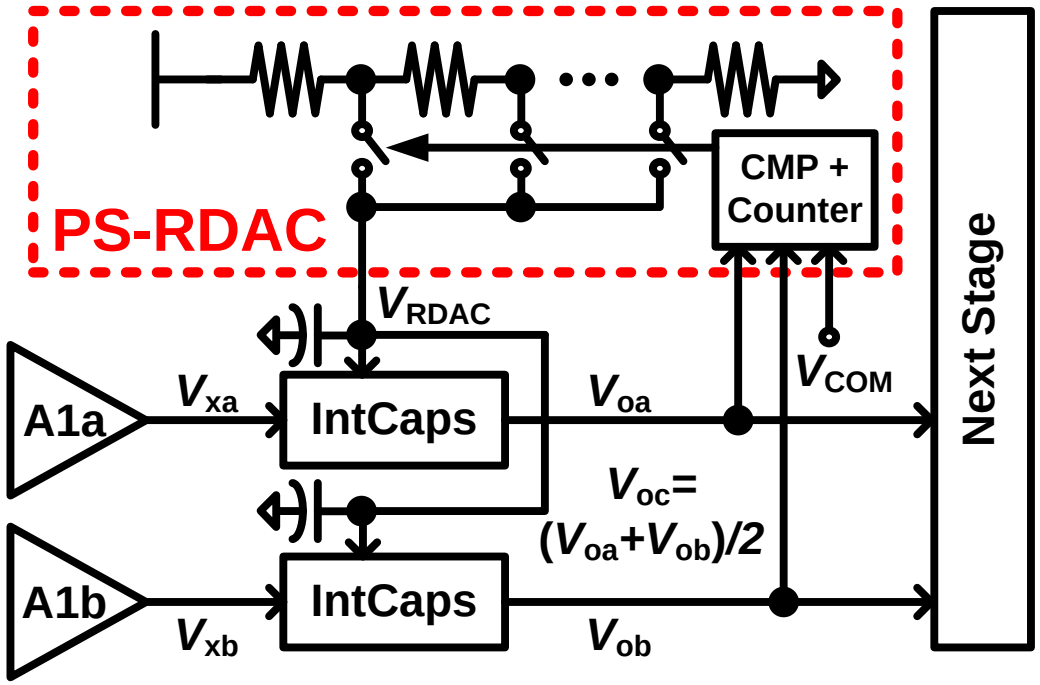
- **Dynamic amplifier with an inverter-based CMD for high-speed operation**

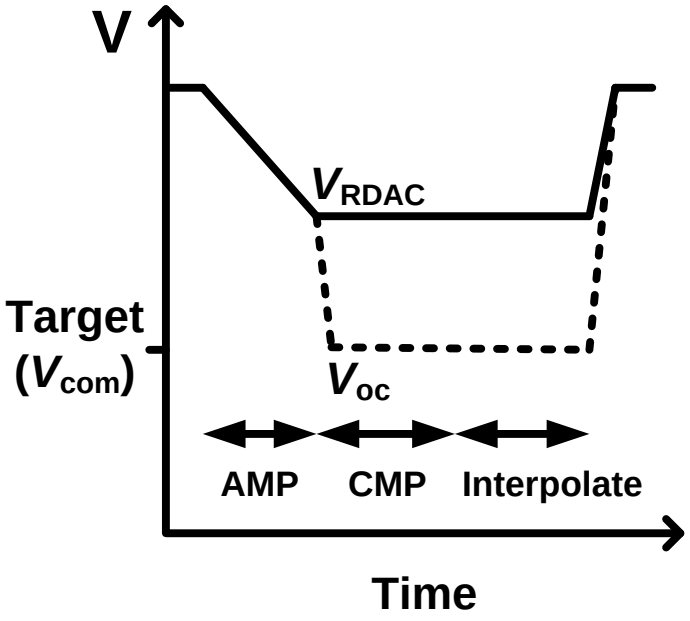


$$\text{Gain} = \alpha(V_{DD}-V_{oc})/V_{eff}\ ,\ 1<\alpha<2$$

Pseudo-Static RDAC

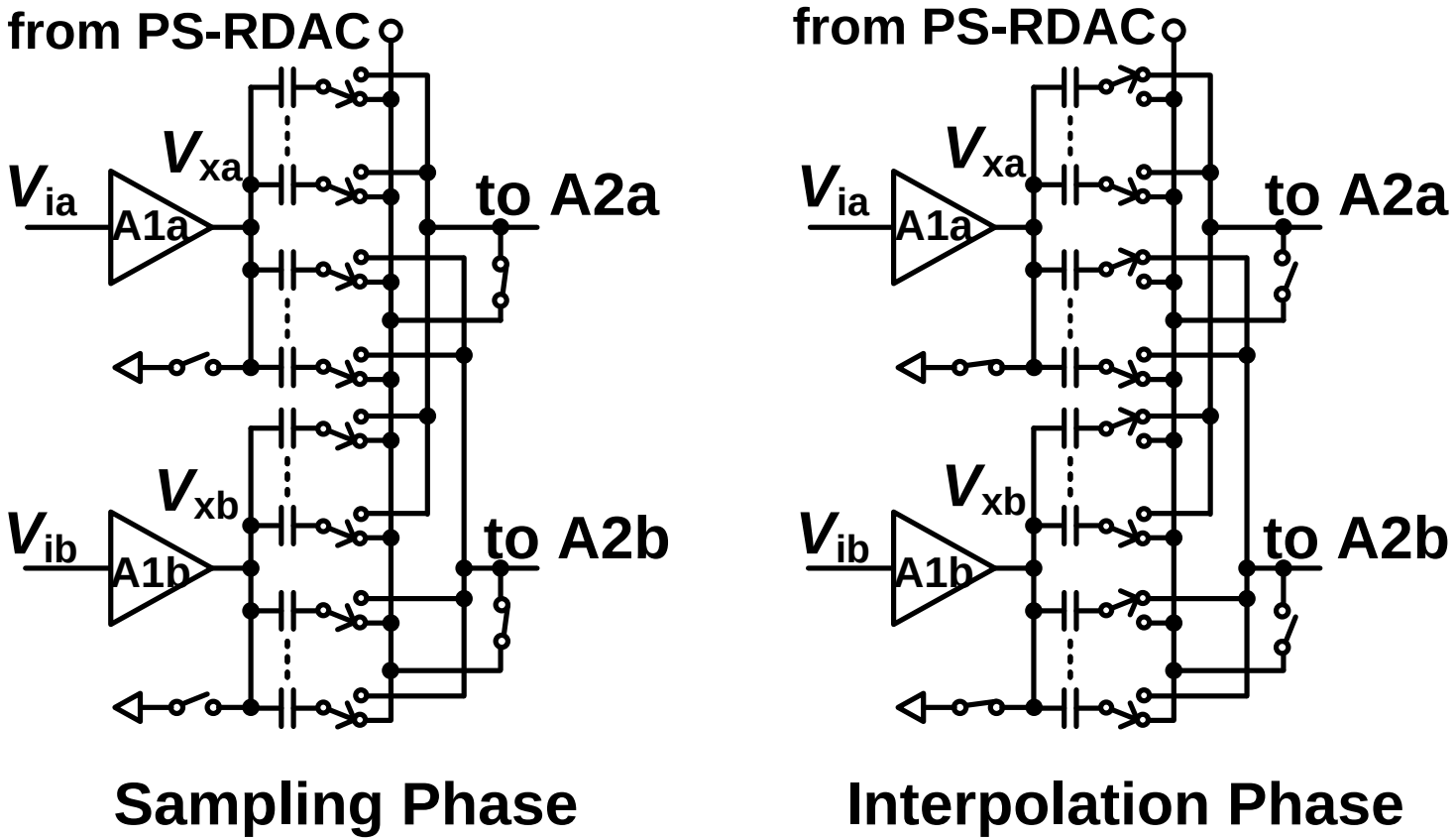
- **Pseudo-static RDAC is proposed to calibrate the common-mode voltage during startup**





Capacitive Interpolation [9]

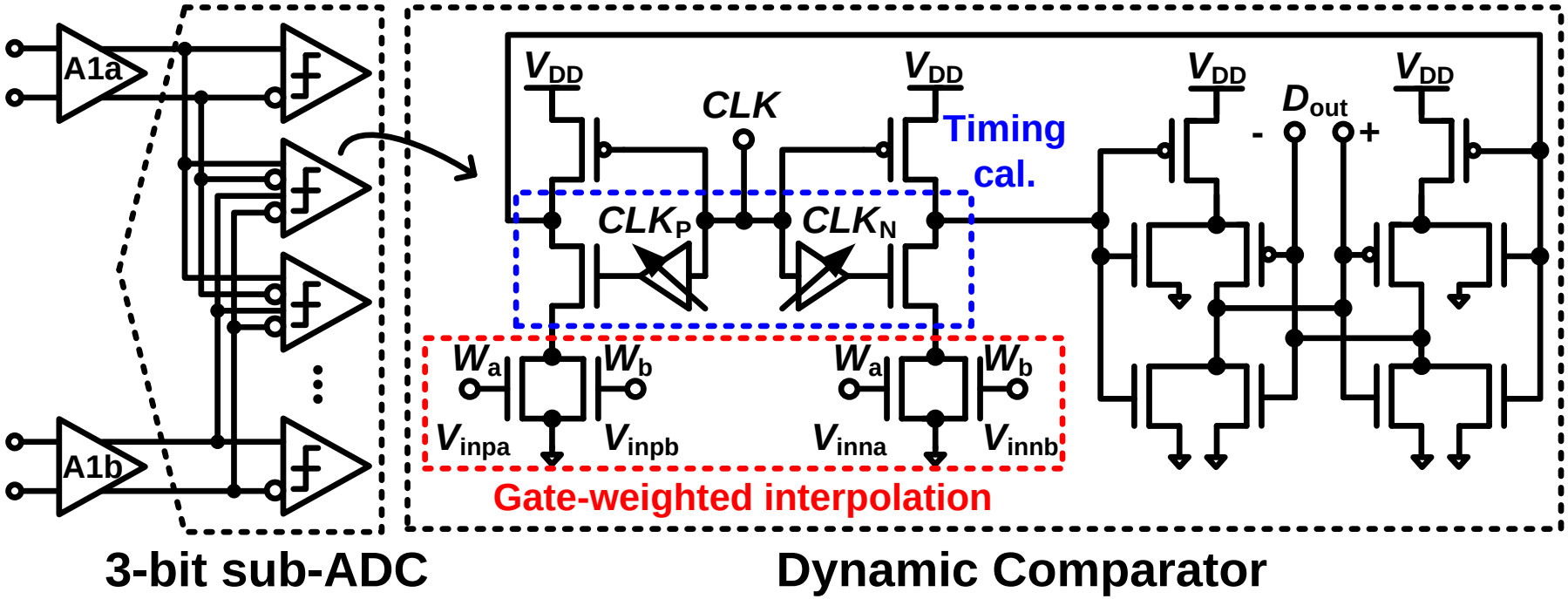
- **Absolute gain → relative gain accuracy**
- **Interpolation is controlled by the sub-ADC**



[9] M. Miyahara, *et al*., VLSI Circuits 2011.

Sub-ADC

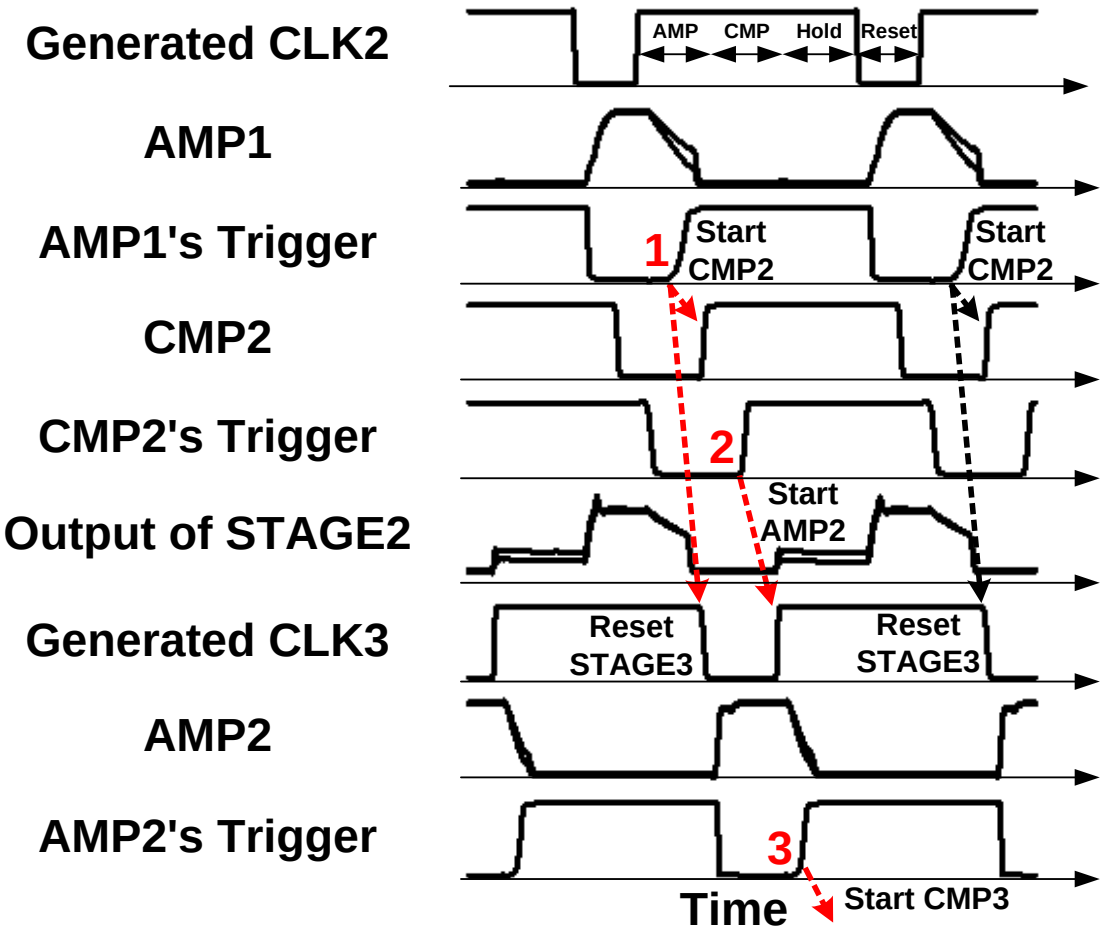
- **Gate-weighted interpolation comparators with a time-based offset calibration**



[10] Y. Asada, *et al*., A-SSCC 2009.
[11] M. Miyahara, *et al*. A-SSCC 2010.

Self-Clocking

- **Internal signals trigger the subsequent stages to maximize speed performance [12], [13]**



[12] J. Yang, *et al*., JSSC 2010. [13] R. Kapusta, *et al*., ISSCC 2013.

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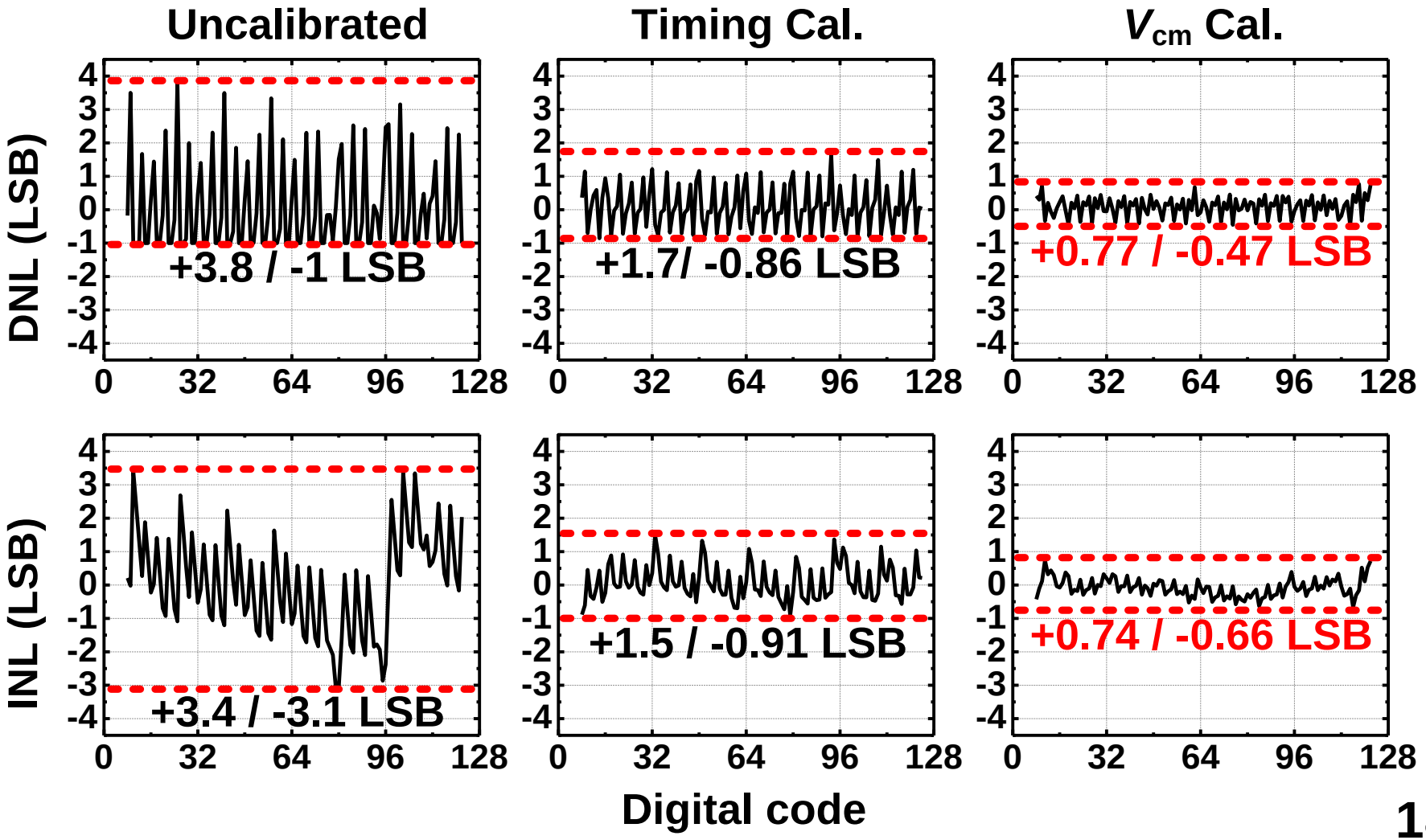
Measured DNL and INL

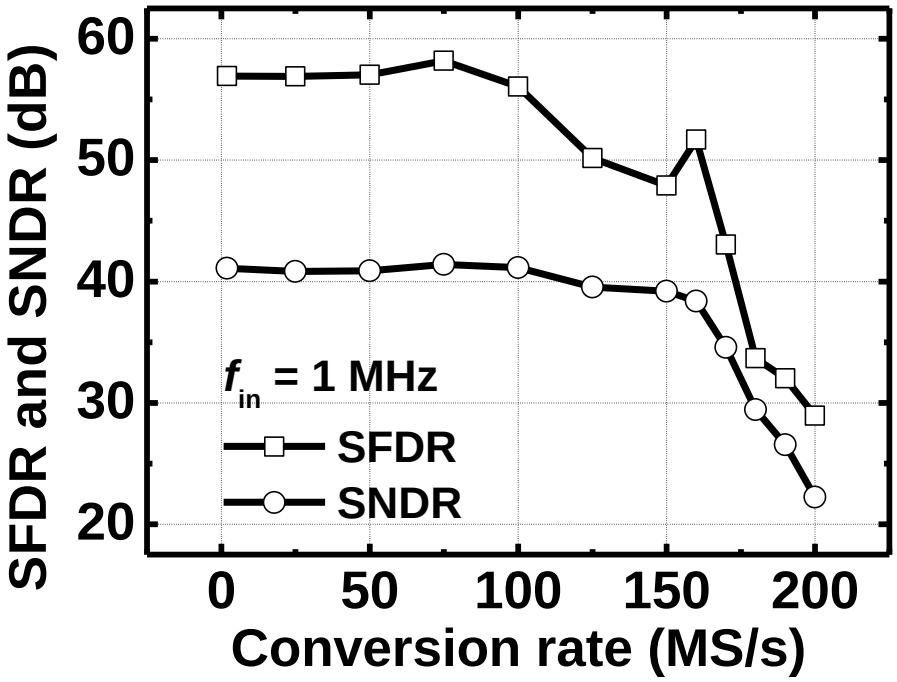
- **Startup calibration: timing cal. + common-mode cal.**



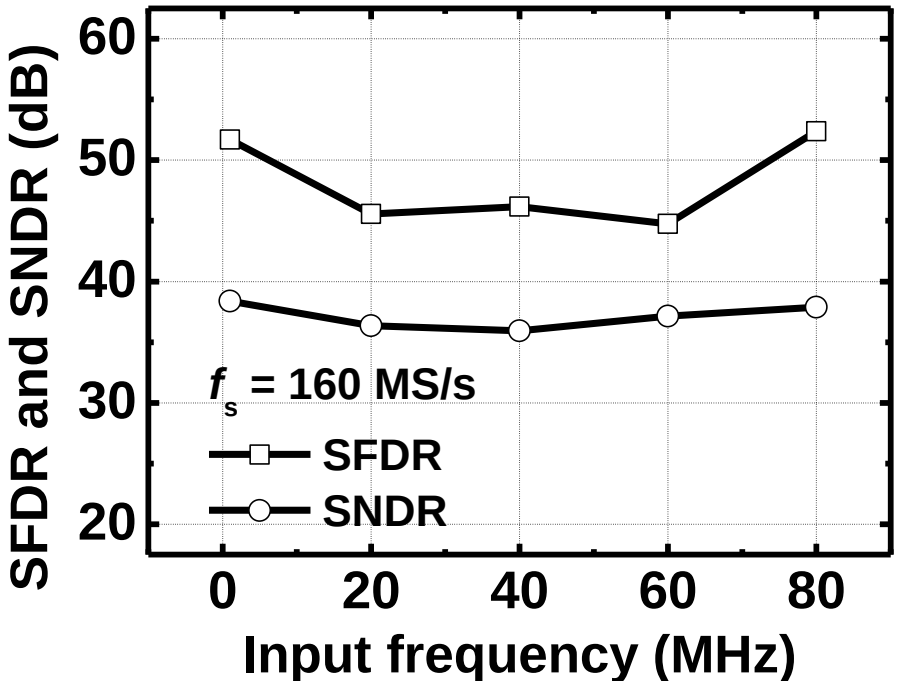
Measured SFDR and SNDR

- **>38 dB of SNDR is measured up to 160 MS/s with an ERBW >80 MHz**
- **Consumes 2.43 mW at 160 MS/s, FoM=240 fJ/c.-s.**

SFDR & SNDR vs. f_s

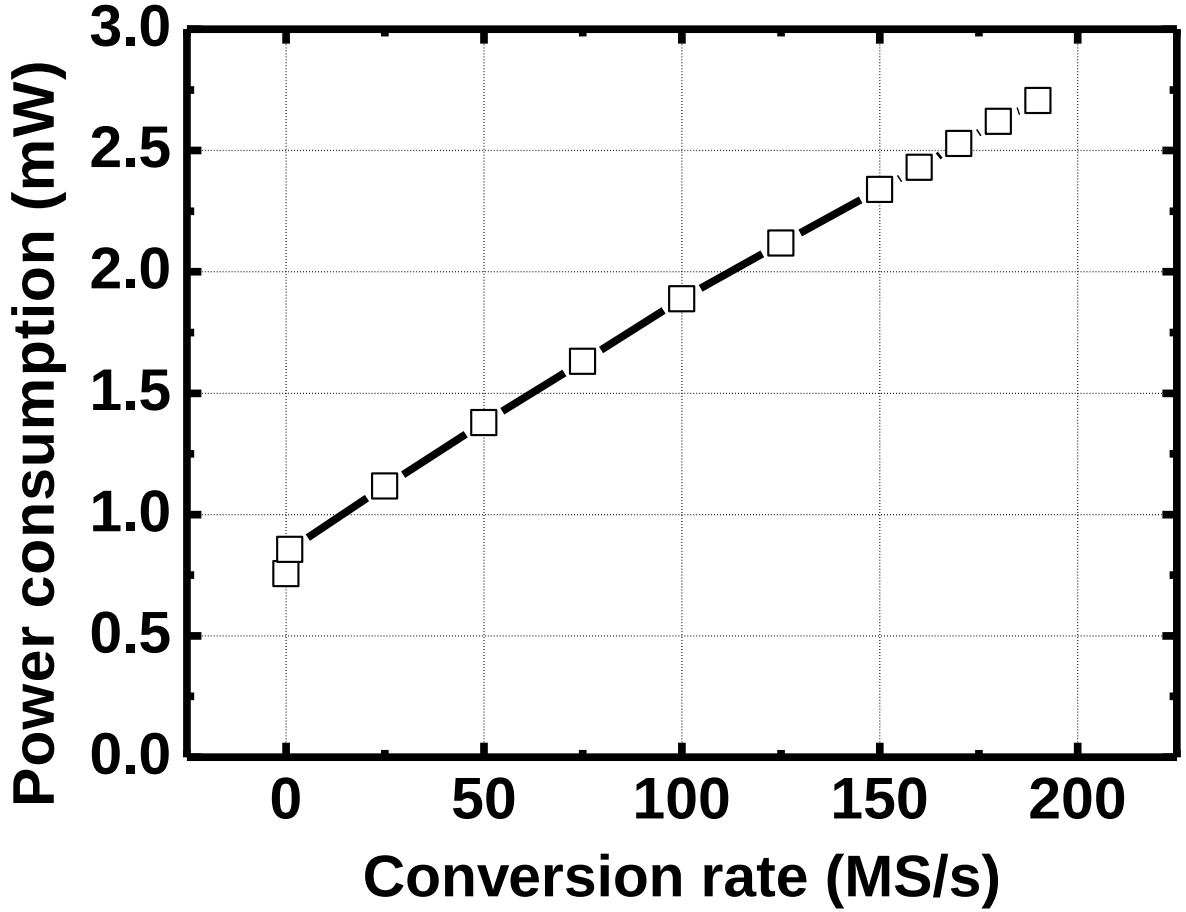


SFDR & SNDR vs. f_{in}



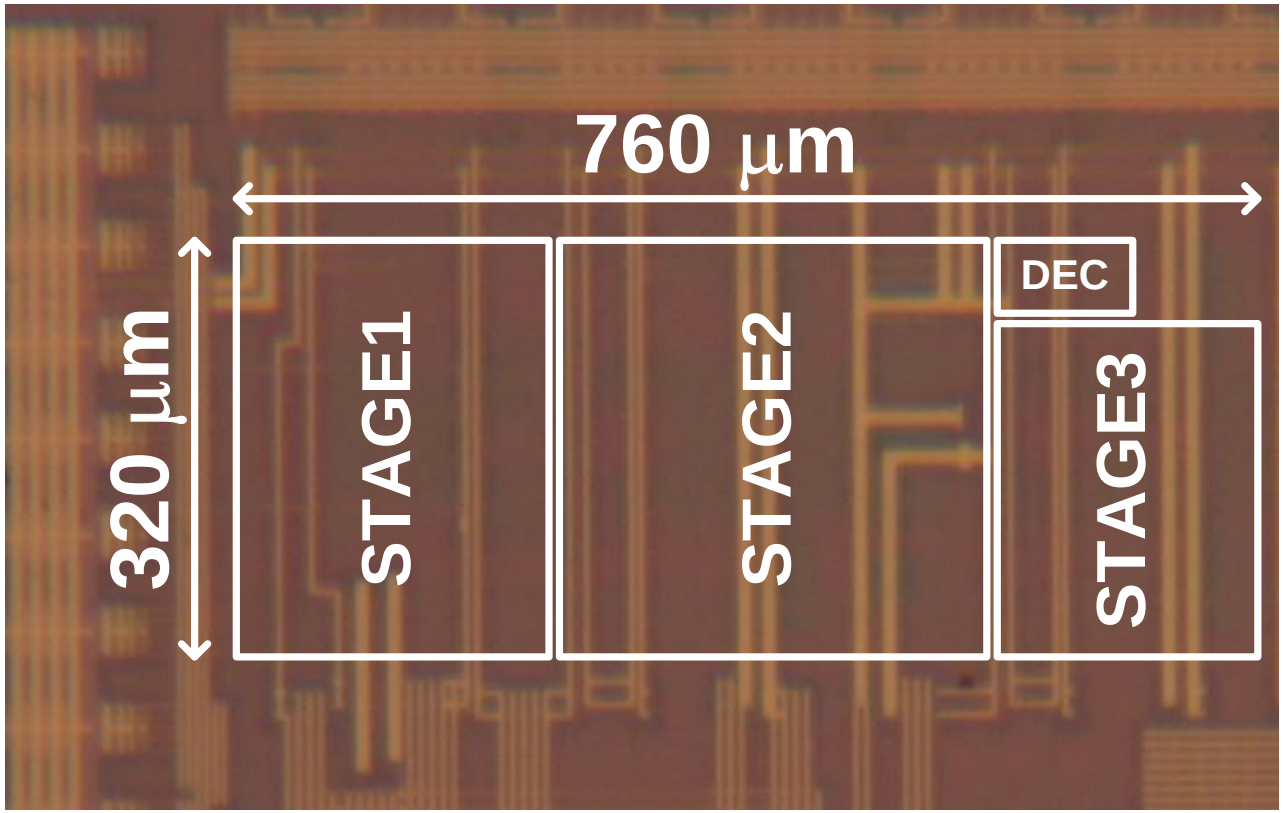
Clock-Scalable Power Performance

- **Dynamic amplifier enables clock-scalability in ADC's power performance**



Chip Photo

- **Prototype ADC is fabricated in 90 nm CMOS with the low threshold and deep N-well options**
- **Occupied area is 0.25 mm^2**



Performance Comparison

- **Fastest ULV ADC compared to other state-of-the-art ULV high-speed ADCs**

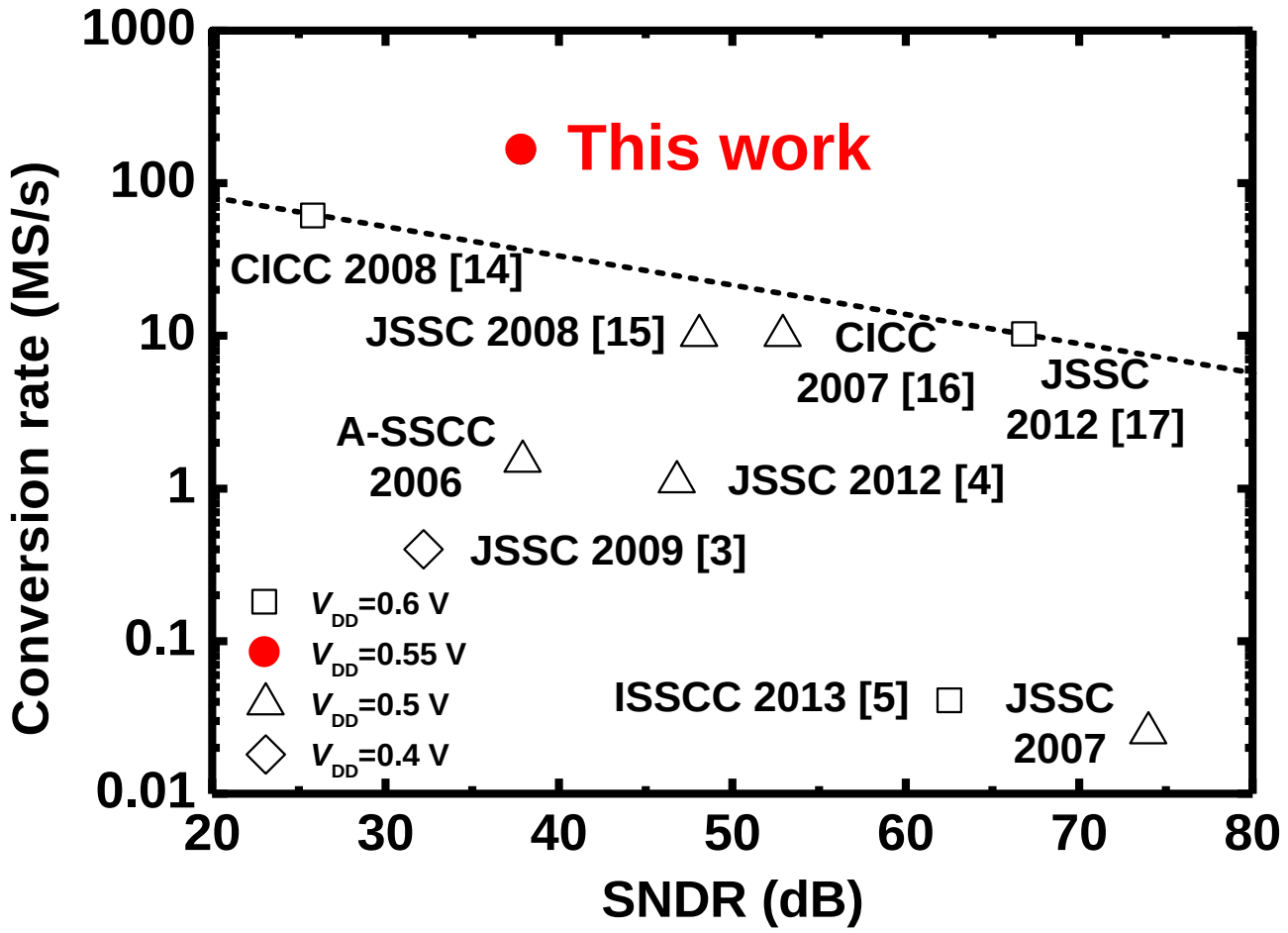
	[14]	[15]	[16]	[17]	This work
Architecture	Flash	Pipeline	Pipeline	Pipeline	Pipeline
Resolution (bit)	5	8	10	12	7
Supply voltage (V)	0.6	0.5	0.5	0.6	0.55/0.5*
f_s (MS/s)	60	10	10	10	160
Power (mW)	1.3	2.4	3.0	0.56	2.43
ENOB (bit)	4.01	7.7	8.5	10.8	6.0
FoM (fJ/c.-s.)	1060	1150	825	30.9	240
Technology (nm)	90	90	130	65	90
Active area (mm^2)	0.11	1.44	0.98	0.36	0.25

*Analog V_{DD} = 0.55 V, Digital V_{DD} = 0.5 V

[14] J. E. Proesel, *et al*., CICC 2008.
[15] J. Shen, *et al*., JSSC 2008.
[16] Y. J. Kim, *et al*., CICC 2007.
[17] S. Lee, *et al*., JSSC 2012.

Summary of ULV Pipeline ADC

- **Proposed ADC demonstrates the feasibility of ULV high-speed analog circuit design**



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Conclusion

- **0.55 V, 7-bit, 160 MS/s, 2.43 mW pipeline ADC is realized using dynamic amplifiers and interpolation**
- **Demonstrates the feasibility of ultra-low-voltage high-speed analog circuit design**
- **Proposed techniques are suitable for ULV and nominal-voltage high-speed circuits**

Acknowledgement

This work was partially supported by NEDO, Huawei, Berkeley Design Automation for the use of the Analog FastSPICE (AFS) Platform, and VDEC in collaboration with Cadence Design Systems, Inc.

Thank you for your interest!

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