

# A 0.55 V 7-bit 160 MS/s Interpolated Pipeline ADC Using Dynamic Amplifiers

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**Abstract**— This paper presents a 0.55 V, 7-bit, 160 MS/s pipeline ADC using dynamic amplifiers. In this ADC, dynamic amplifiers with a common-mode detection technique are used as residual amplifiers to increase its robustness against supply voltage lowering. These amplifiers also remove the unnecessary static power consumption achieving clock-scalability in power performance. The 7-bit prototype ADC fabricated in 90 nm CMOS demonstrates an ENOB of 6.0 bits at a conversion rate of 160 MS/s with an input close to the Nyquist frequency. At this conversion rate, it consumes 2.43 mW from a 0.55 V supply. The resulting FoM is 240 fJ/c.-s.

## I. INTRODUCTION

System-on-a-chip (SoC) designs have significantly reduced the cost and the form factor of modern electronics by combining the analog interface circuits with digital computing and signal processing circuits on the same die. As the digital circuits often occupy the majority of the area in a SoC, the technology selection and system design choices are mainly driven by the digital circuits' requirements.

As the feature sizes of advanced nanoscale CMOS technologies continue to reduce, the maximum supply voltage is expected to reduce to as low as 0.55 V in the next decade or so [1] for reliability reasons. Such supply voltage scaling is extremely beneficial to digital circuits and memory in reducing the heating issues as well as increasing the energy efficiency at the cost of slower operation speed. To overcome the reduced speed, parallelism is an effective method for digital circuits [2].

For analog circuits, there are many challenges in addition to the speed reduction such as the smaller voltage headroom, the reduced SNR, and the increased effects of transistor variation at low voltages. To address these, several techniques have been reported such as sub-threshold operation [3], body driven circuits [4], and SAR-based operation [5], [6]. These techniques were all very successful and have achieved very good performance at ultra-low voltage (ULV); however, they all share a common drawback: slow operation speed.

Unfortunately for analog circuits, the excessive use of parallelism have some disadvantages such as an increase of area, a reduction of PVT margin, a degradation of performance, and an increase of input drive difficulty [7]. Therefore, in order to realize high-speed SoCs using advanced technologies, ULV high-speed analog design techniques are

necessary. In this paper, we propose an ULV clock-scalable high-speed pipeline ADC using dynamic amplifiers.

## II. CIRCUIT DESIGN

### A. Interpolated Pipeline Architecture

The pipeline architecture is suitable for high speed and moderate resolution conversion. However, the insufficient OpAmp gain of the scaled CMOS technologies makes designing high performance pipeline ADCs challenging. To address this issue, a pipeline ADC with a capacitive interpolation has been developed in [8] to shift the gain requirement from absolute accuracy to relative accuracy between open-loop amplifiers. By harnessing this relative gain accuracy property, dynamic amplifiers that are suitable for ULV operation can be used as residual amplifiers to realize an ULV high-speed pipeline ADC.

Fig. 1 shows the block diagram of the proposed ADC with dynamic amplifiers as its residual amplifiers. A fully differential scheme is implemented; however, a single-ended scheme is used in the paper for simplicity. In the first stage, an input signal,  $V_{in}$ , and a reference voltage,  $V_{ref}$ , are sampled by a pair of capacitor arrays. Then a 3-bit sub-ADC (CMP1) generates the first set of conversion data that are used to control the switches of the capacitor arrays. With the conversion data, these capacitor arrays behave like a pair of capacitor DACs (CDACs) generating the required residual voltages for the next pipeline stage.

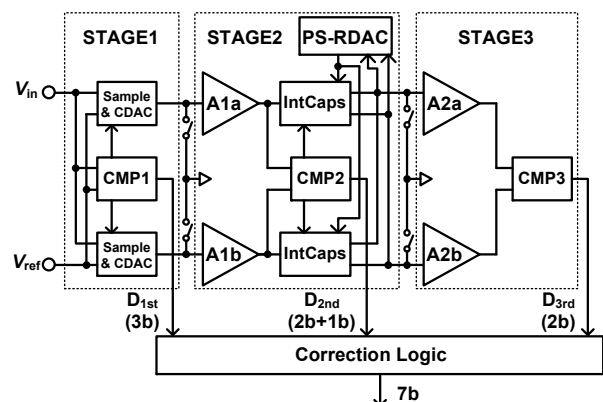


Fig. 1. Block diagram of the proposed ADC using dynamic amplifiers as residual amplifiers.

At the second stage, the residual voltages are first amplified by the dynamic amplifiers, A1a and A1b. The output signals of the amplifiers are stored on the interpolation capacitor arrays (IntCaps) and compared by another 3-bit sub-ADC (CMP2) using gate-width-weighted interpolation [9]. Again, the second set of conversion data controls the switches of the interpolation capacitors providing the required residual voltages for the final pipeline stage. The final stage consists of two more dynamic amplifiers, A2a, and A2b, with a 3-bit sub-ADC (CMP3) providing the final set of conversion data of the pipeline ADC.

Fig. 2 shows the capacitor arrays of the interpolation circuits. The input signals,  $V_{ia}$  and  $V_{ib}$ , are amplified by the dynamic amplifiers resulting in internal output voltages of  $V_{xa}$  and  $V_{xb}$ , respectively. These voltages are sampled on the interpolation capacitor arrays. During the interpolation phase, each capacitor is controlled by the sub-ADC to either connect to the input of the next pipeline stage or remain connected to the reference voltage provided by the pseudo-static RDAC (PS-RDAC) thus providing the interpolated values.

### B. Dynamic Amplifier with Common-Mode Detection

In this ADC, dynamic amplifiers are used as residual amplifiers to eliminate the unnecessary static current. Furthermore, dynamic operation allows the power consumption to be clock-scalable. In this work, a dynamic amplifier with a common-mode detector from [10] is modified for high-speed operation. The capacitive common-mode detector (CMD) is replaced by the inverter-based CMD, as shown in Fig. 3, to reduce the capacitive load on the amplifiers. The two inverters with the shorted outputs approximate the output common-mode voltage while the last inverter's threshold voltage determines when the triggering signal is activated. The gain of this amplifier is designed to approximately 3 times, which is sufficient for the interpolated pipeline architecture.

Fig. 4 shows the operation of the dynamic amplifiers with the interpolation capacitors directly acting as the load. When the clock is low, the output nodes are reset and pre-charged by the PS-RDAC and the internal output nodes,  $V_{xp}$  and  $V_{xn}$ , are reset to  $V_{DD}$ . When the clock turns high,  $V_{xp}$  and  $V_{xn}$  are discharged proportionally to the input voltages,  $V_{inp}$  and  $V_{inn}$ , until the internal output common-mode voltage ( $V_{xc}$ ) crosses a

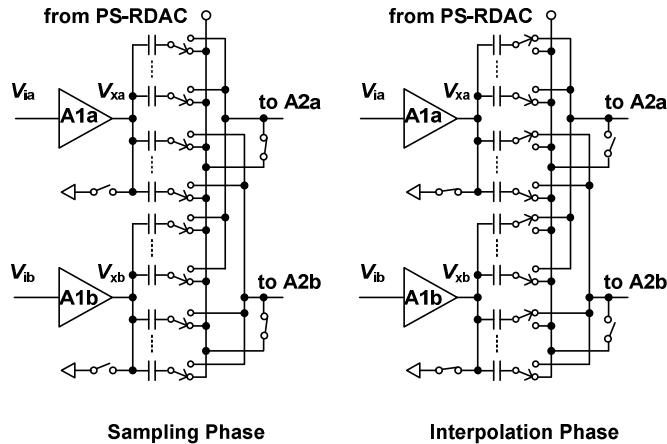


Fig. 2. Capacitor arrays to perform the interpolation.

pre-determined threshold voltage. Upon crossing this threshold voltage, the CMD is activated terminating the discharging providing stable output voltages for the interpolation capacitor arrays.

### C. Calibration

To realize the proposed design, the increased mismatch between transistors at ULV and the amplifier's sensitivity to the input common-mode voltage ( $V_{ic}$ ) all require compensation. This ADC uses the double-tail latched comparators from [11] with the timing calibration [7] to suppress the offset voltages of the comparators. To address the amplifier's sensitivity to  $V_{ic}$ , a 5-bit PS-RDAC is used to modify the output common-mode voltage ( $V_{oc}$ ) of the interpolation capacitor arrays. The schematic of the PS-RDAC and its operation diagram are shown in Fig. 5. This PS-RDAC draws much less static current than the required instantaneous current from the interpolation capacitors. As a result, a large capacitor is placed at its output node to act as a tank. When the amplifiers are activated, the interpolation capacitors draw current from the tank lowering the tank voltage,  $V_{RDAC}$ . When the amplifiers reset, the tank is slowly restored by PS-RDAC's weak static current. The final  $V_{oc}$  of the interpolation capacitors is automatically tuned to the ADC's common-mode voltage,  $V_{com}$ , by adjusting the PS-RDAC using comparators and logic during the startup calibration.

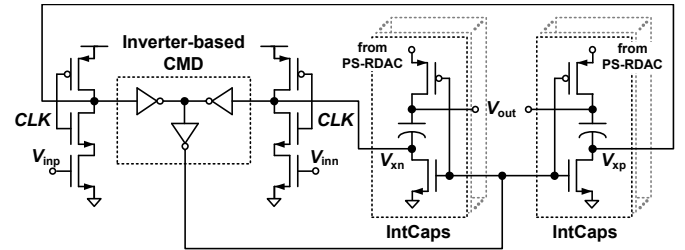


Fig. 3 Schematic of the dynamic amplifier with an inverter-based common-mode detector

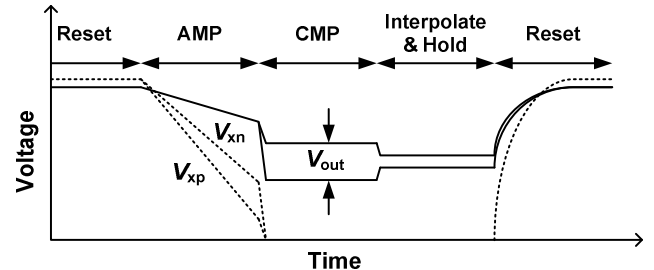


Fig. 4. Operation waveform of the modified dynamic amplifier with the interpolation capacitors as its load.

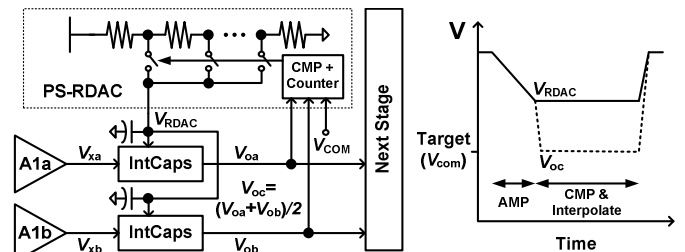


Fig. 5. Schematic of the proposed pseudo-static RDAC for the common-mode voltage control and its operation waveform.

### D. Self-Clocking Scheme

Asynchronous operation allows the circuit to allocate just the right amount of time to function correctly. This maximizes the overall speed of the circuit [12]. Fig. 6 shows the simulated timing diagram of the self-clocking scheme with some key steps. In step 1, the dynamic amplifier uses its triggering signal to initiate the following sub-ADC and to reset the following pipeline stage. Likewise, the sub-ADC is designed to notify the following stage's amplifiers upon its completion as shown in step 2. This asynchronous triggering mechanism continues in a pipeline fashion as illustrated by step 3. To utilize the conversion time effectively, a 75% duty cycle clock is generated on-chip from a  $2 \times f_s$  off-chip signal source. The ON cycle is self-allocated among the three operations: amplify, compare, and interpolate and hold. Upon completing each operation, it will initiate the subsequent operation resulting in a fully self-timed behavior maximizing the speed of the proposed ADC.

### III. MEASUREMENT RESULTS

The prototype ADC is fabricated in 90 nm CMOS technology with the low threshold voltage and the deep N-well options. The supply voltages are 0.55 V for the analog part and 0.5 V for the digital part. The power consumption is 2.43 mW at a conversion rate of 160 MS/s. The breakdown of the consumed power is as follows: 1.03 mW for the analog part, 1.33 mW for the digital part including the clock generator and the clock buffers, and 0.07 mW for the references and the peripheral circuits such as the PS-RDAC. Fig. 7 shows the measured results. DNL and INL are  $+0.63/-0.41$  LSB and  $+0.42/-0.42$  LSB, respectively. SNDR of at least 38 dB is measured up to 160 MS/s. The effective resolution bandwidth (ERBW) is up to 80 MHz. The resulting FoM is 240 fJ/c.s. The occupied area is  $0.25 \text{ mm}^2$  as illustrated by the chip photo in Fig. 8. From the measurement results, the proposed design achieves the highest speed among other state-of-the-art ULV ADCs as shown in the comparisons in Fig. 9 and Table I.

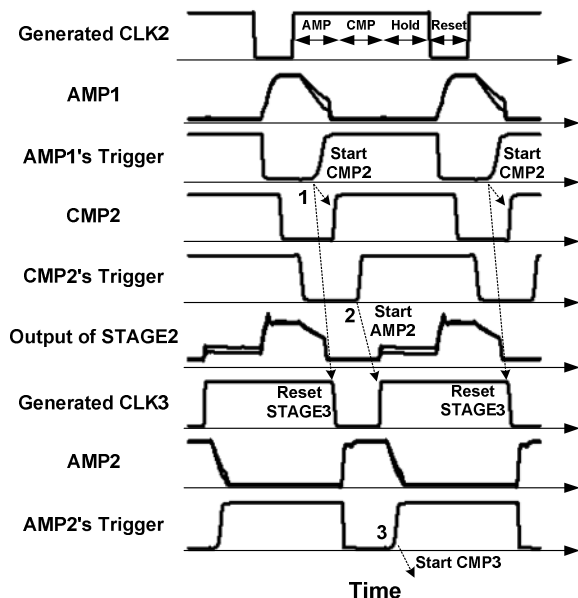
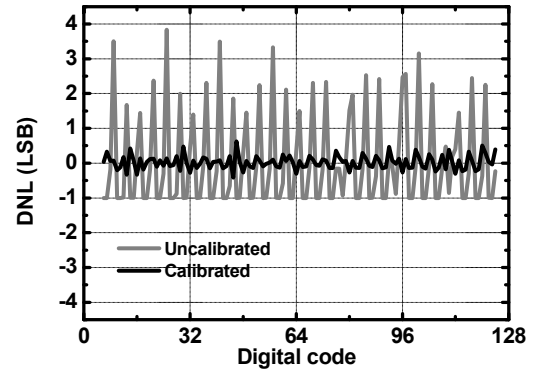
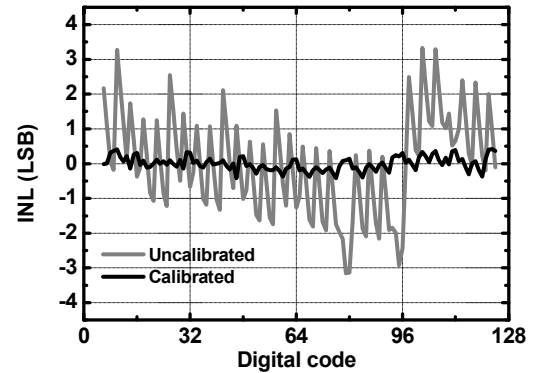


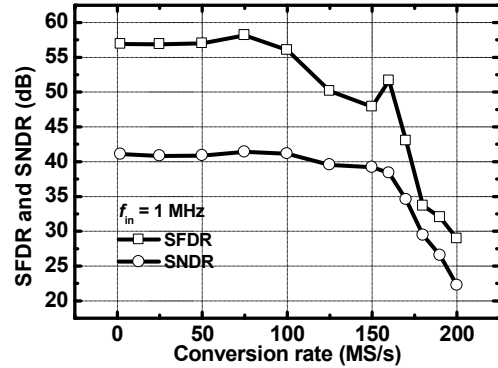
Fig. 6. Simulated timing diagram of the self-clocking scheme.



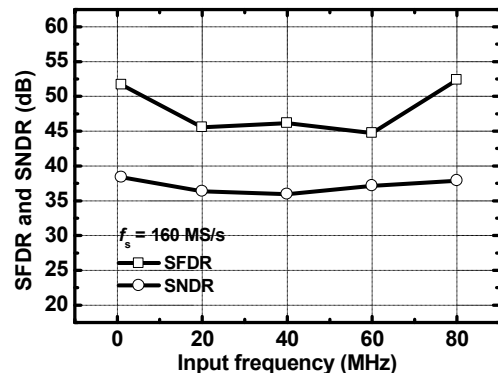
(a)



(b)



(c)



(d)

Fig. 7. Measured (a) DNL, (b) INL, (c) SFDR and SNDR vs. conversion rate, and (d) SFDR and SNDR vs. input frequency.

TABLE I: PERFORMANCE COMPARISON WITH OTHER STATE-OF-THE-ART ULTRA-LOW-VOLTAGE HIGH-SPEED ADCs

	[13]	[14]	[15]	[16]	This work
Architecture	Flash	Pipeline	Pipeline	Pipeline	Pipeline
Resolution (bit)	5	8	10	12	7
Supply voltage (V)	0.6	0.5	0.5	0.6	0.55/0.5*
$f_s$ (MS/s)	60	10	10	10	<b>160</b>
Power consumption (mW)	1.3	2.4	3.0	0.56	2.43
ENOB (bit)	4.01	7.7	8.5	10.8	6.0
FoM (fJ/c.-s.)	1060	1150	825	30.9	240
Technology (nm)	90	90	130	65	90
Active area (mm <sup>2</sup> )	0.11	1.44	0.98	0.36	0.25

\* 0.55 V for analog and 0.5 V for digital.

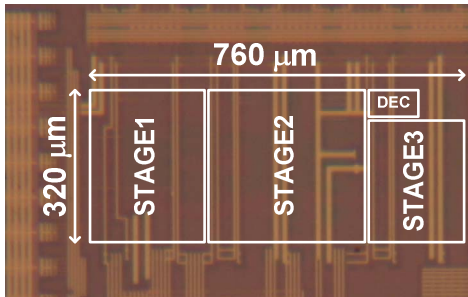


Fig. 8. Chip photo of the prototype ADC.

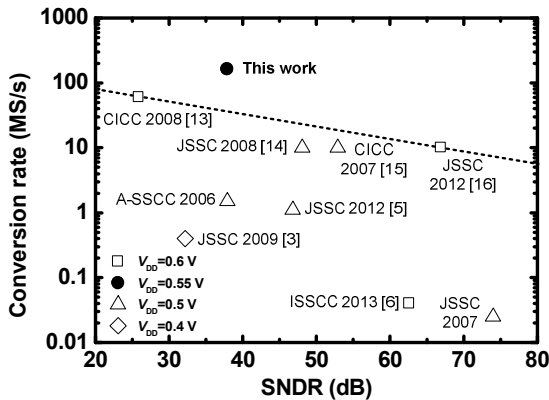


Fig. 9. Performance comparison chart showing the state-of-the-art ULV ADCs.

#### IV. CONCLUSION

In conclusion, this paper presents an ULV, clock-scalable, high-speed interpolated pipeline ADC that operates up to 160 MS/s. The proposed dynamic amplifier enables both clock scalability and high-speed operation at 0.55 V. The proposed ADC demonstrates the feasibility of ultra-low voltage high-speed analog circuit design.

#### ACKNOWLEDGMENT

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