A 0.84ps-LSB 2.47mW Time-to-Digital Converter Using a Charge Pump and a SAR-ADC

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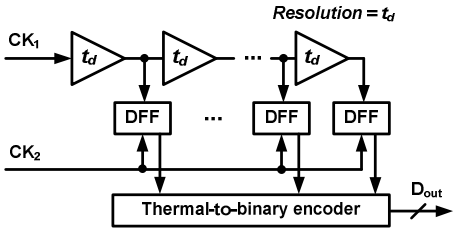
***Abstract*—We propose a time-to-digital converter (TDC) using a charge pump and a SAR-ADC. With this architecture, high time resolution is attainable by increasing the charging current or reducing the sampling capacitance. Thus, the resolution limitation in a delay-chain TDC does not exist. We propose to use a SAR-ADC attributed to its characteristics of compact structure, scalability, low power consumption, and small area. The prototype chip was fabricated in 65nm CMOS, achieving 0.84ps LSB, 2.47mW power consumption, and 0.06mm^2 area occupation. With 8-bit outputs, the DNL and INL are -0.7/1.0 LSB and -2.7/1.7 LSB, respectively.**

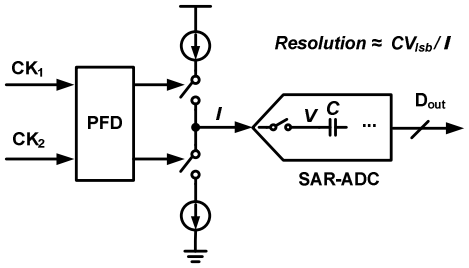
I. INTRODUCTION

Having been functioning in a time-of-flight measurement system for decades, time-to-digital converters (TDC) are increasingly demanded since the advent of all-digital PLLs (ADPLL). Technology scaling shortens the delay of logic gates, endowing delay-chain TDCs' (Fig.1 (a)) applications in more and more systems. However, the time resolution with a logic gate delay fails to satisfy low-jitter ADPLLs that typically require pico-second resolution of a TDC. Thus, advanced techniques are demanded to break this limitation while keeping low power consumption and small area.

Various techniques have been proposed to enhance the time resolution. A Vernier TDC shrinks the resolution to the difference of two logic gate delays but it is vulnerable to PVT variations. Although a DLL calibration loop can be used for global calibrations, local mismatches still cause jitters that degrade the effective resolution and the linearity [1]. In a pipeline TDC, time amplifiers (TAs) are utilized to amplify the time residue for further quantization in following stages but the nonlinearity and mismatches of TAs require much calibration effort [2]. Against jitter and nonlinearity issues, oversampling and noise-shaping TDCs are proposed. However, the input signal bandwidth is inherently low, or on the other hand, the resolution is limited by the oversampling ratio (OSR) [3]. A statistic TDC utilizes the process variations of timing arbiters to accumulate a high-gain transfer function. Due to this characteristic, however, the detectable range is short and the performance is heavily dependent on the technology used [4]. All these solutions address the time quantization in the time domain which is still "rough" with technologies commonly used.



(a) Conceptual block diagram of delay-chain TDC



(b) Conceptual block diagram of proposed TDC

Fig. 1. (a) Dealy-chain TDC and its resolution limitation, and (b) proposed TDC and its potential of high resolution.

In this paper, we propose a solution exploiting the charge domain for high time resolution. Although some analog circuits are employed, they are kept simplified and compact for the balance between performance and power/area overhead. Meanwhile, our proposal still benefits from technology scaling, which will be described in the following sections.

II. PROPOSED SOLUTION

A. Concept and Conventional Issues

The conceptual block diagram of our proposal is shown in Fig. 1(b), where time interval is translated to charges on a capacitor and then the charges are quantized by an ADC. From a simplified equation: $t_{res} = CV_{lsb}/I$, the time resolution can be boosted by increasing the current, reducing the capacitance, or enhancing the

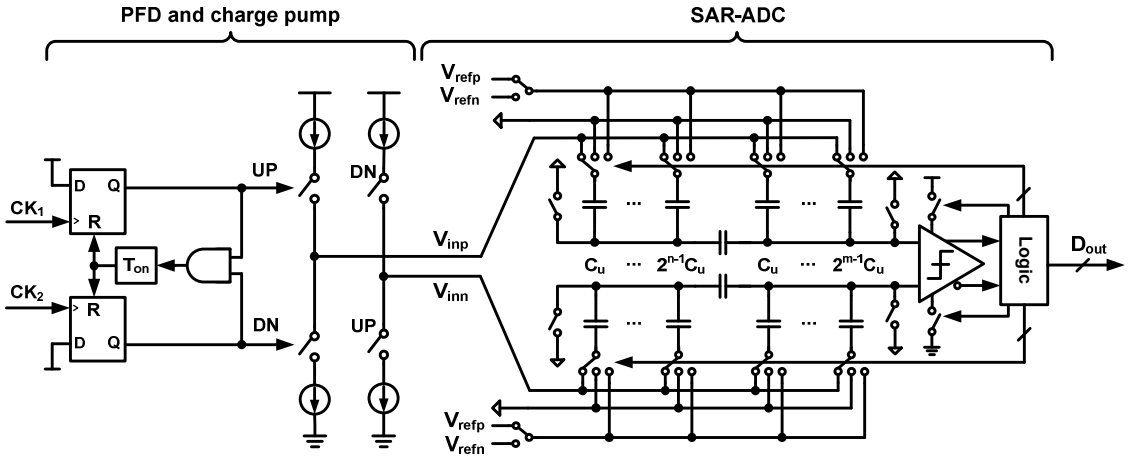


Fig. 2. Architecture of proposed TDC.

ADC's resolution. In the old days, however, the latter two approaches were impractical when implementing on an integrated circuit (IC) due to the low density of on-chip capacitors, and the unreasonably large power and area consumptions of an ADC. Consequently, on-chip solutions used a dual-slope-counter [5] or "semi-time-semi-voltage-domain" delta-sigma architectures where the signal bandwidths are limited [3][6].

B. Selection of the ADC and the Proposed Architecture

The type of the ADC affects the practicability of this proposal. A flash ADC is capable of extremely high speed with low resolution. To increase its dynamic range, the comparators increase exponentially so that significant power, area and calibration are involved. A pipeline ADC features high resolution and high speed. However, the amplifiers consume much power, and designing a high gain op-amp becomes tough with recent technologies. A delta-sigma ADC faces the similar situation due to its integrators, although it achieves extremely high resolution.

We propose to use a SAR-ADC attributed to its several advantages for the proposed TDC [7]. First, unlike other types of ADCs, it only contains one CDAC for both sampling and quantization, as well as one comparator. Thus, a compact structure is available. By using metal-oxide-metal (MOM) capacitors and a dynamic comparator, it squeezes power and area consumptions to be low with enough sampling rate for an ADPLL. Moreover, the binary-weighted CDAC suggests easier scalability of the resolution. The extension of the resolution is generally done by adding the capacitors other than the comparators or the op-amps that are required in other types of ADCs.

Fig.2 illustrates the architecture of our proposed TDC. A differential topology is used against the common-mode surges. An issue is that the voltage noise is also integrated during the sampling period. We will analyze this effect in the next section.

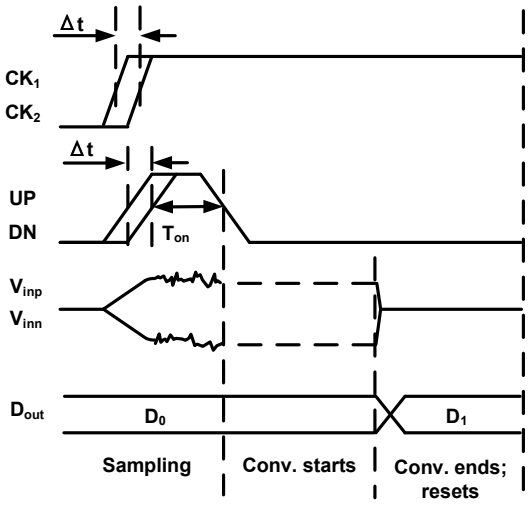


Fig.3 Timing diagram and the noise accumulation.

C. Timing, Noise, and Design Perspective

The major timing diagram of the proposed TDC is shown in Fig. 3. The rising edges of two input signals, CK_1 and CK_2 trigger PFD's outputs UP and DN to turn on the switches of the charge pump. It is known that the feedback delay, T_{on}, is used to remove the dead-zone effect but the voltage noise are accumulated on the capacitors during this period.

The accumulated average noise power can be calculated using (1), where C is the total sampling capacitance seen from the output of the charge pump, I_{cp} is the bias current of the current source, and g_{mn} and g_{mp} are the transconductances of NMOS and PMOS current sources, respectively.

$$\sigma_{vn}^{\ 2} = \frac{4kT\gamma}{2C^2} \cdot \frac{(g_{mn} + g_{mp})}{I_{cp}} \cdot I_{cp} \cdot T_{on} \qquad (1)$$

Considering the pseudo-differential topology, using $t=CV/(2I)$, we derive (2), where V_{lsb} is the LSB voltage resolved by the ADC, and $\sigma_{vn,diff}$ is the sum of noise power of two outputs.

$$\sigma_{vn,diff}^{\ 2} = 2 \cdot kT\gamma \cdot \frac{T_{on}}{C_{lsb}} \cdot \frac{V_{lsb}}{t_{res}} \cdot \frac{(g_{mn} + g_{mp})}{I_{cp}} \qquad (2)$$

Equation (2) gives a perspective of designing the proposed TDC, where g_m/I_{cp} is a design parameter for transistor sizing of the current sources. Generally, small values of g_m/I_{cp} and C are preferred for low noise and small area, which are fortunately the outcomes of the technology scaling. Small C requires short T_{on} to stop the noise accumulation, which is also practical thanks to the shrunk switch sizes.

III. Circuits Design

A. Charge Pump and Switched-Capacitor Replica Biasing

A cascode pseudo-differential charge pump is designed as shown in Fig. 4. Dummy branches are used to reduce charge sharing, and also serve as the replica biasing during reset period to equal currents of PMOS and NMOS transistors. It typically requires an amplifier in a feedback loop, consuming some power.

For a low power design, we propose to use switched-capacitor (SC) feedback circuitry to generate the bias voltage. The idea is same as SC common mode feedback, well applied in fully-differential amplifiers, except that only one node, V_m, is sensed. For simplicity, output common mode is not regulated since the actual charging time is short enough and the outputs are reset cyclically. Although it is vulnerable to common-mode surges during either UP or DN is turned on, the feedback provides some power supply rejection because either dummy branch is also on at the same time. Hence, the surge from the power supply is sensed from V_m, and V_{bp_fb} is regulated.

B. SAR-ADC

The topology of the SAR-ADC is shown in Fig. 2. MOM capacitors and a dynamic comparator are designed. We use 8-bit output from a 12-bit topology since a 12-bit SAR-ADC is being developed in another project. If an actual 8-bit topology is used, the size of the CDAC can be shrunk to 1/16, as well as its power consumption. Fig. 5 shows the image layout of 12-bit, 10-bit, and 8-bit CDAC, implying this area shrinking. The increase of the noise may be concerned. However, if we rewrite (2) into (3), we find that the noise to minimum signal ratio does not change if only the ADC's resolution is scaled by shrinking the CDAC. For example, from 12-bit to 8-bit, C is reduced to 1/16, and V_{lsb} is increased to 16 times as well, i.e. the required charges do not change, if the reference voltage is unchanged. Therefore, the time

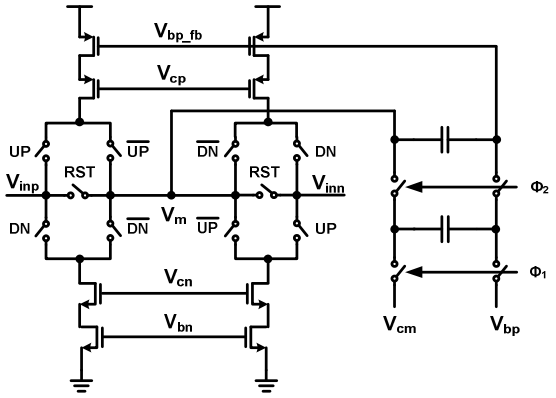


Fig. 4. Charge-pump with switched-capacitor replica biasing

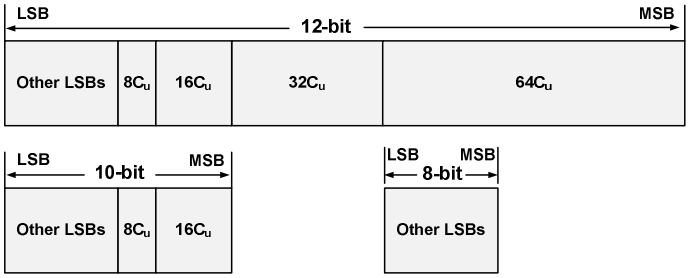


Fig. 5. Image layout of 12-bit, 10-bit, and 8-bit CDAC.

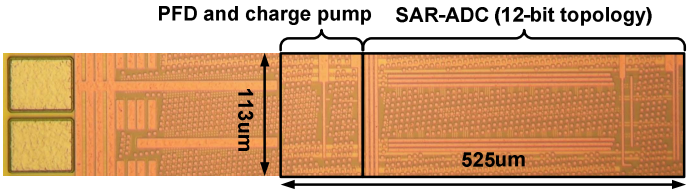


Fig. 6 Chip photo

resolution is not affected when scaling the SAR-ADC. To decrease this ratio, short T_{on} is important which is available with technology scaling as stated in section II.C.

$$\frac{\sigma_{vn,diff}^{\ 2}}{V_{lsb}^{\ 2}} = 2 \cdot kT\gamma \cdot \frac{1}{CV_{lsb}} \cdot \frac{T_{on}}{t_{res}} \cdot \frac{(g_{mn} + g_{mp})}{I_{cp}} \qquad (3)$$

IV. Measurement Results

A prototype IC has been fabricated in 65nm CMOS. The chip photo is shown in Fig. 6, with 0.06mm^2 core area. With 40MHz input clocks and 1.0V power supply, the total power consumption is 2.47mW, where about 0.9mW is consumed by the charge pump.

To measure the DNL and INL, two frequencies with nominal 5Hz difference were input to the TDC, creating time ramps. With histogram method, DNL and INL are calculated as -0.7/1.0 LSB and -2.7/1.7 LSB, respectively, with 0.83ps per LSB, as shown in

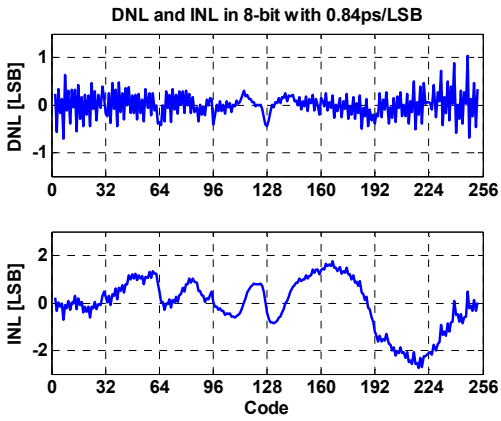


Fig. 7 Measured DNL and INL

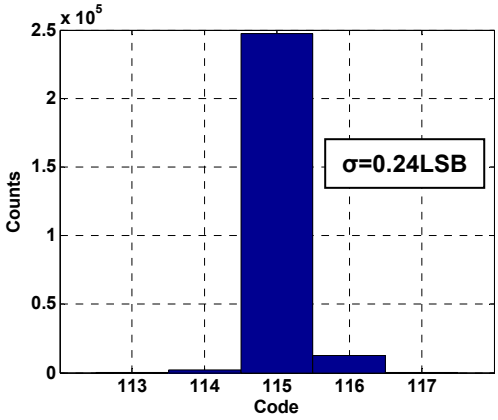


Fig. 8 Measured single-shot precision

Fig. 7. To measure the single-shot precision, one output from Agilent E4861B is split into two and fed to the TDC. The measured standard deviation is 0.24LSB as shown in Fig. 8, suggesting the TDC's low intrinsic noise.

The performance comparison is listed in Table I, manifesting the best balance of our work. Literature [2] has better resolution but its power and area overheads are 4 and 5 times larger than ours, respectively. Although [1] achieves smallest area and lowest power among others, its resolution is 5 times lower than ours. Since the SAR-ADC has a 12-bit topology, if it is optimized to 10-bit, we expect 2.5 times higher sampling rate, 1/2 conversion energy, and 1/4 area occupation in the next work, as listed in Table I. Again, this is reasonable according to (3) and the corresponding design methodology of the SAR-ADC.

V. Conclusion And Future Work

We have proposed a high resolution TDC using a charge pump and a SAR-ADC, proving that quantizing time in charge domain is practical to achieve high resolution with low power consumption and small area. We have given equations of the involved voltage noise, showing a method of the parameter decision, the scalability of the SAR-ADC, and the benefits from the technology scaling. The prototype has achieved 0.84ps LSB, 8-bit range, 2.47mW power consumption, and 0.06mm^2 area occupation. The performance can be further optimized by designing the SAR-ADC properly.

In the future, we will implement this TDC into an ADPLL where low in-band phase noise can be expected using this high resolution TDC with low power consumption and small area.

TABLE I. Performance Comparison

	[1]	[2]	[3]	[4]	This work	Next target
Type	Vernier	Pipeline	Delta-sigma	Stochastic	SAR-ADC	SAR-ADC
CMOS [nm]	65	130	130	65	65	65
Supply [V]	1.2	1.3	1.2	1.2	1.0	1.0
Resolution [ps]	4.8	0.63	3	3	0.84	0.84
Range [bits]	7	11	11	4	8	10
DNL [LSB]	<1	0.5	N/A	1.4	-0.7/1.0	N/A
INL [LSB]	3.3	2	N/A	1.5	-2.7/1.7	N/A
Frequency [MHz]	50	65	90 (OSR:16)	40	40	100
Power [mW]	1.7	10.5	3.2	8	2.47	4
Area [mm^2]	0.02	0.32	0.43	0.04	0.06	0.015

Acknowledgment

This work was partially supported by NEDO, MIC, CREST in JST, STARC, HUAWEI, Berkeley Design Automation for the use of the Analog FastSPICE(AFS) Platform, and VDEC in collaboration with Cadence Design Systems, Inc.

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