Proposal of layout-driven 1/2.8 size DAC design methodology

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Nov 19, 2013

Matsuzawa & Okada Lab.

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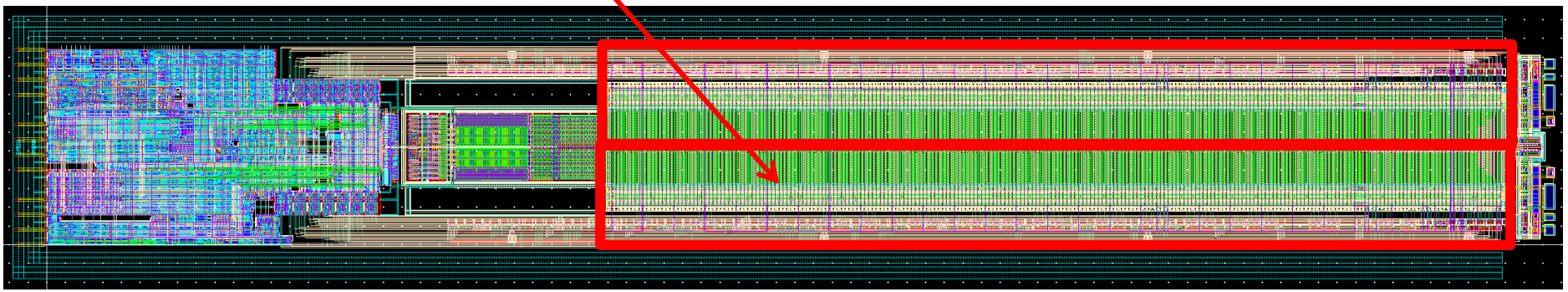
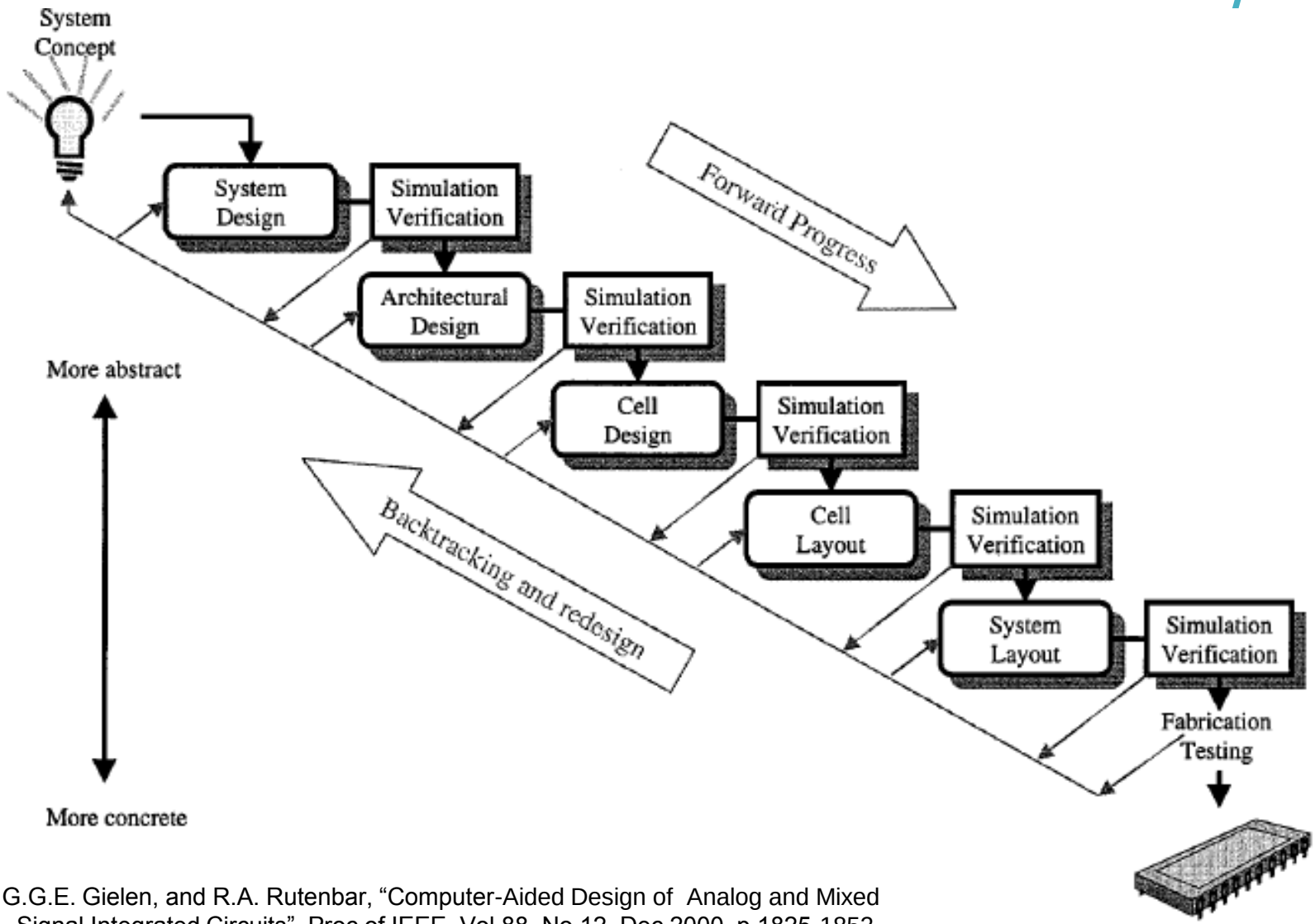
このDACの話をします



Abstract

- Typcal D-to-A converter (DAC) design flow is hierarchical; architecture →circuit →layout design.
- We propose a layout-driven architecture and circuit design.
- We have successfully designed a sub-micron wide slice including unit capacitor & unit switches.
- It earns scalable & smaller parasitic C,R,L, then significant higher speeds and lower powers.
- Our new silicon samples of 12bit 1Gsps DAC in a SAR ADC has demonstrated only 1/2.8 area of our previous design, and they have demonstrated +20% higher speeds.

Previous DAC design methodology



G.G.E. Gielen, and R.A. Rutenbar, "Computer-Aided Design of Analog and Mixed -Signal Integrated Circuits", Proc of IEEE, Vol.88, No.12, Dec 2000, p.1825-1852

Previous DAC design example

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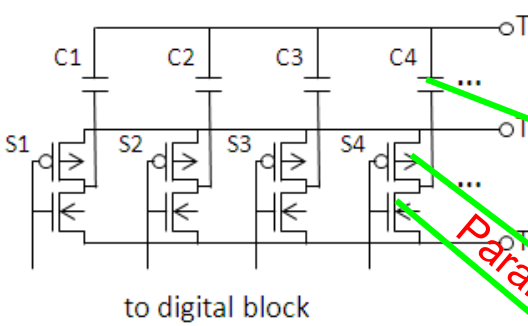

1. C1=20fF, C2=40fF, C3=80fF, C4=160fF, ...
2. S1 NMOS W/L=2um/Lmin, S2=x2, S3=x4, S4=x8, ...
3. S1 PMOS W/L=2um/Lmin, S2=x2, S3=x4, S4=x8, ...
4. Separate each capacitors or shield.
5. Separate between capacitors and digital block or shield.

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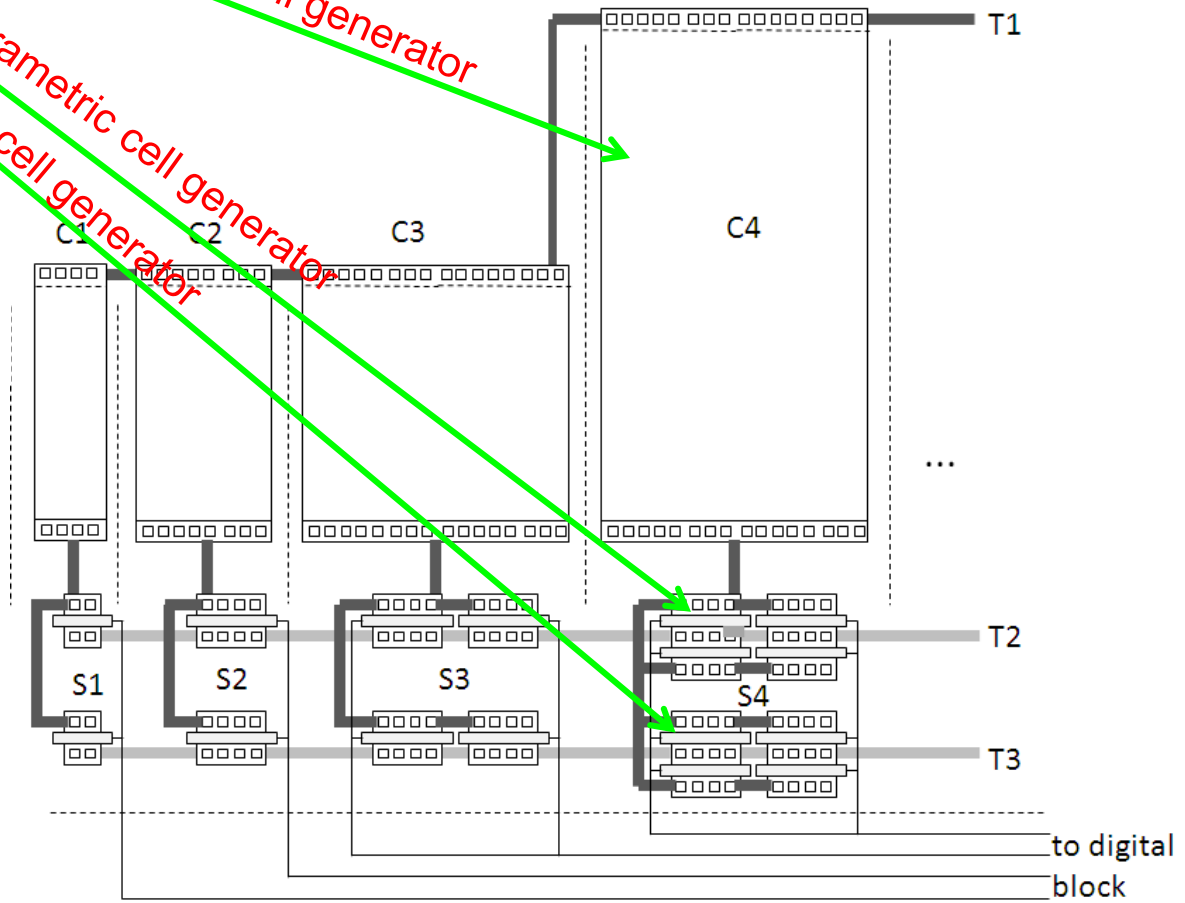

Previous DAC design concerns

- Top down design methodologies
  - Back-annotations & spice simulations can only guarantee final analog performances.
  - Even though, layout designs have most constrains, less freedom.
  - Layout designers use parametric cell generators in layout tools. Cell size+ order (1~10~μm) designs.
  - Layout designers never initiate better architecture and circuit designs.

Proposed DAC design methodology

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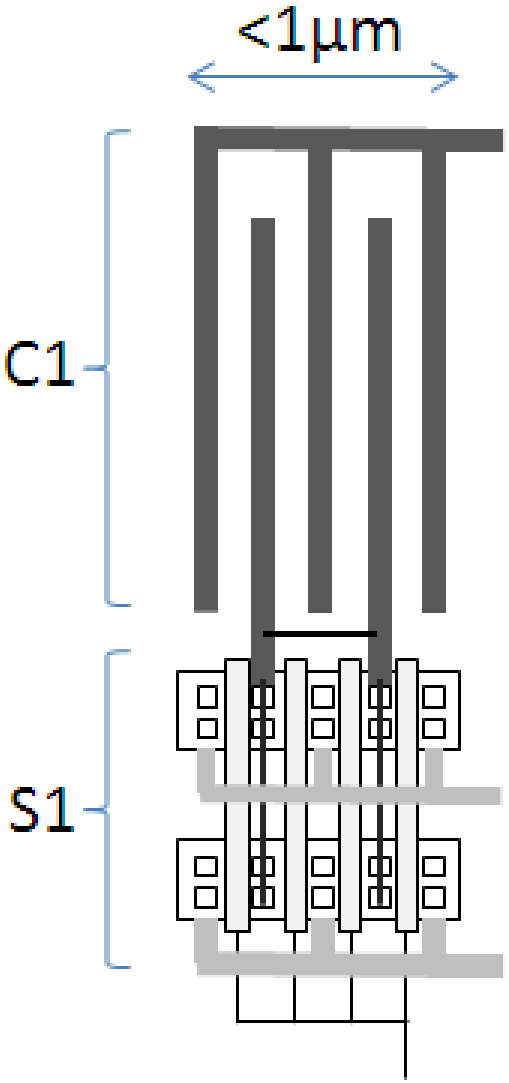
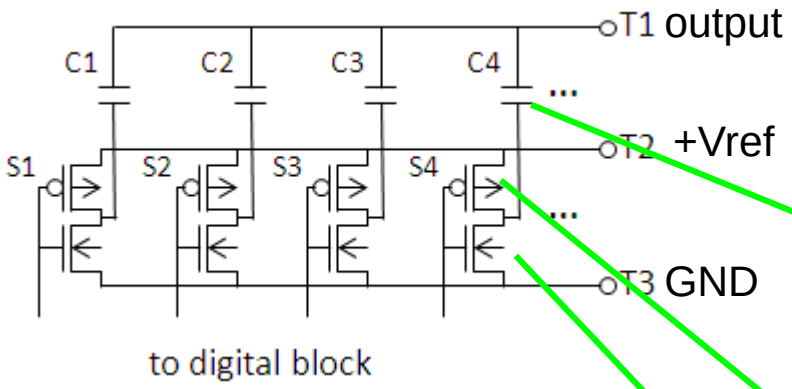
- Layout driven = Give layout 1st priority
  - Consider smallest size, better matching, higher speed, etc. without cell border at layout point of view
  - Common node T1 of capacitors instead of isolations and shields
  - Common source transistors w/o isolations
  - Use MOM capacitor (comb type)
  - Less wires
  - :

Proposed method: sub-micron slice

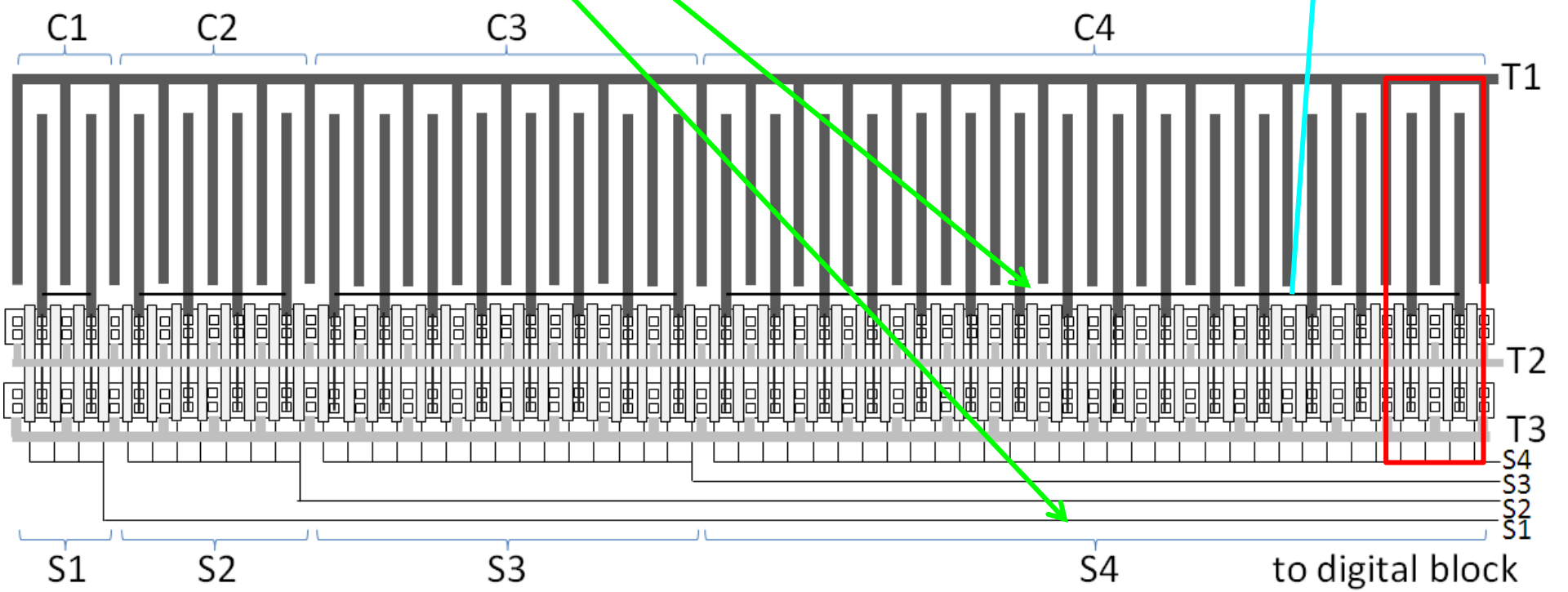
- sub-micron wide slice design
  = capacitor & switch in-line
  - <1μm pitch in deep sub-micron processes
  - No isolations, no shields except dummies on both sides
  - <<1μm wire lengths make significant small stray C,R,L. <1fF swing is available.
  - Total capacitance is determined by kT/C noise.



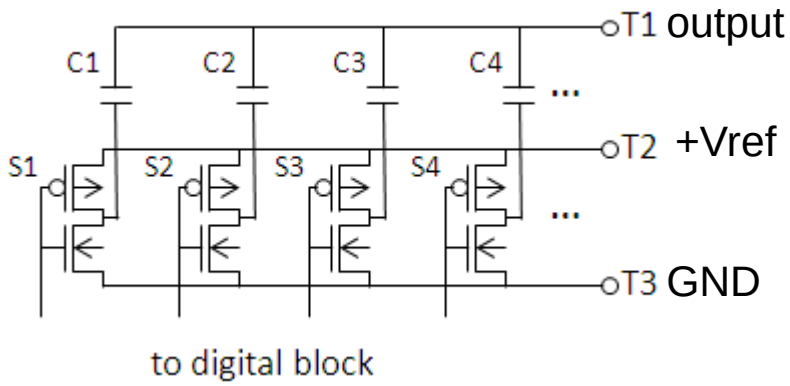
Proposed method: binary coded C-DAC



We can cut short bars due to same voltages



Proposed method: scrambled binary



Cancel gradient of capacitances, such as metal thickness.

Better INL, DNL

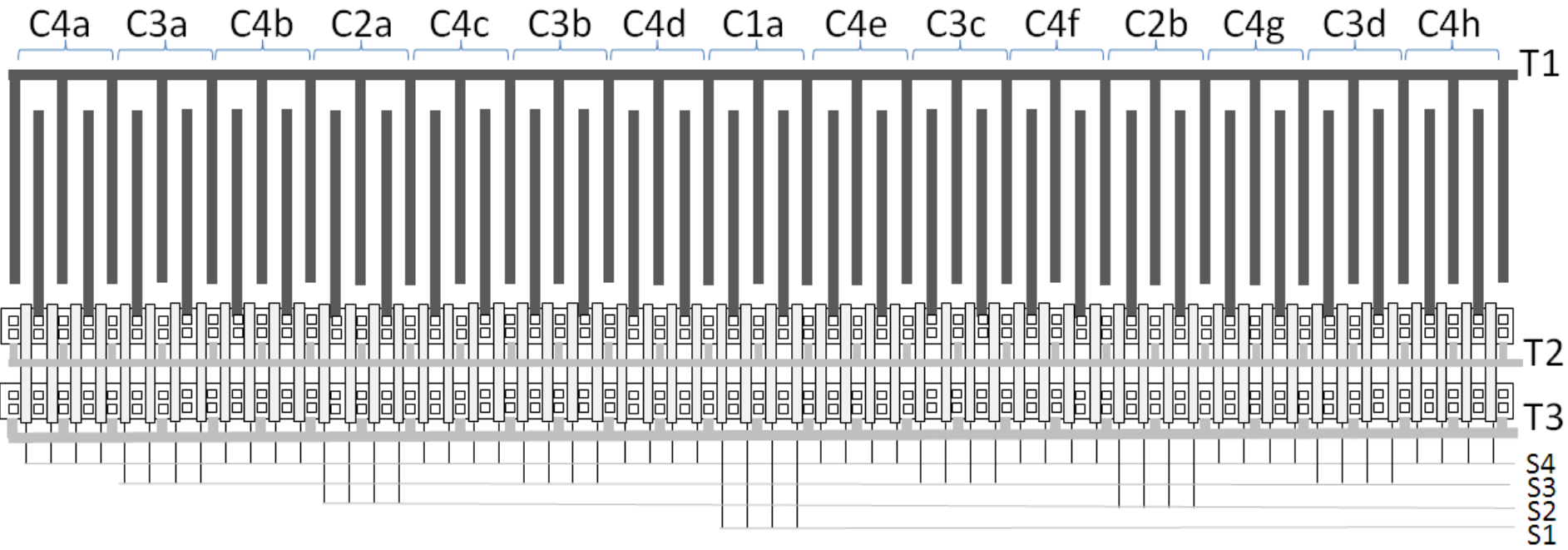
C1=C1a

C2=C2a+C2b

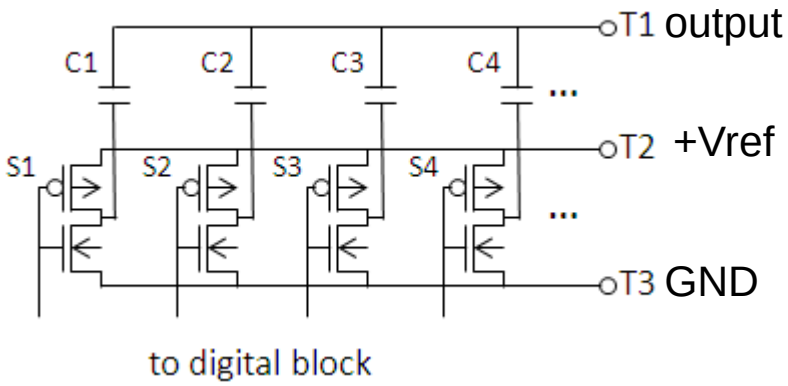
C3=C3a+C3b+C3c+C3d

C4=C4a+C4b+C4c+C4d+C4e+C4f+C4g+C4h

Controlled by switch logic connections.

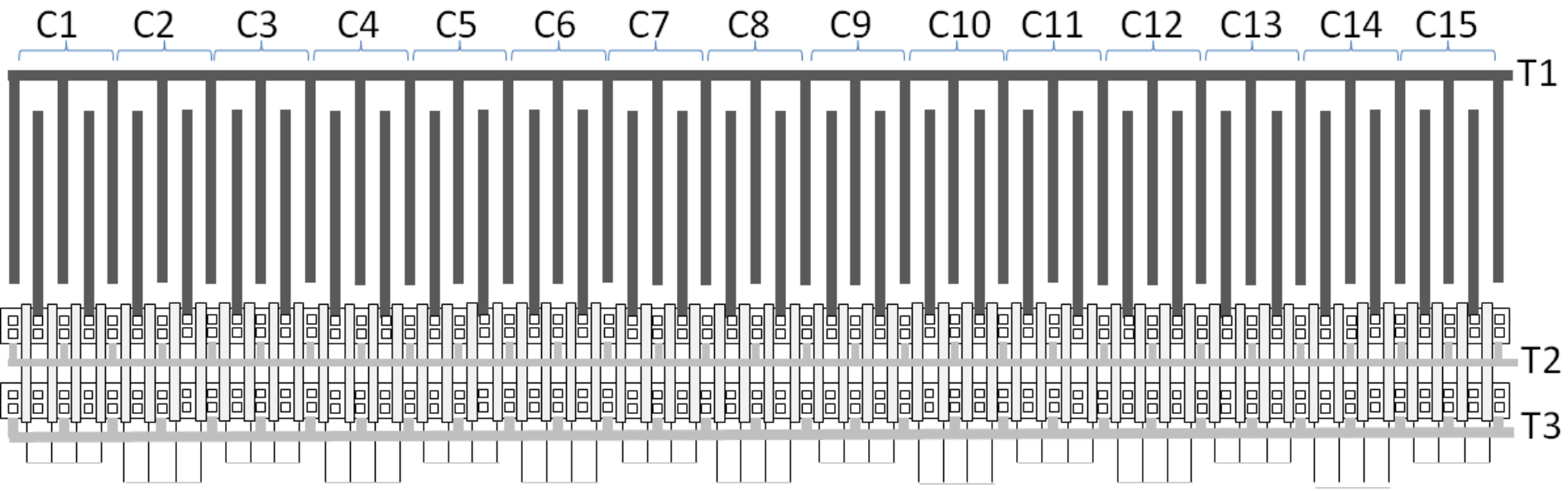


Proposed method: thermometer coded

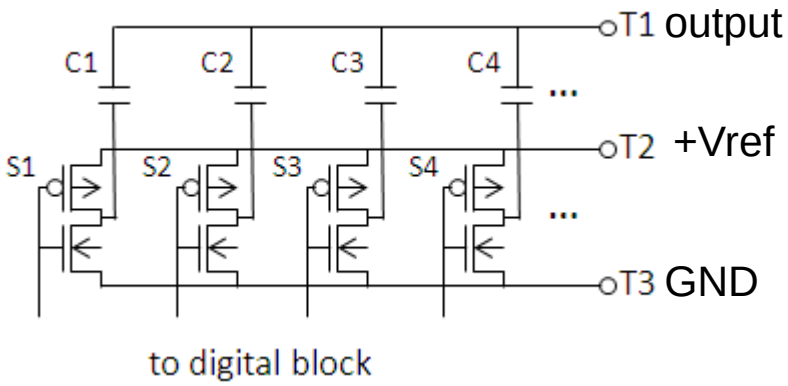


Equal valued capacitors.
Monotonicity is guaranteed.
The code operates to add one by one.

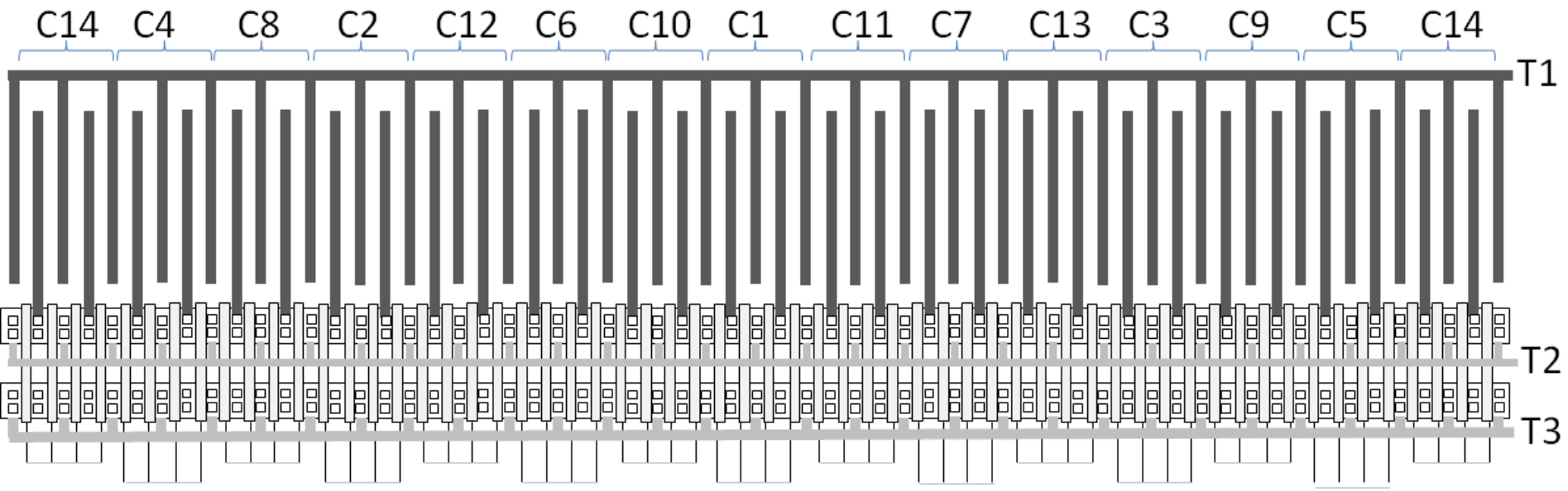
0: all off
1: C1 on
2: C1,C2 on
3: C1,C2,C3 on
:



Proposed method: scrambled thermometer

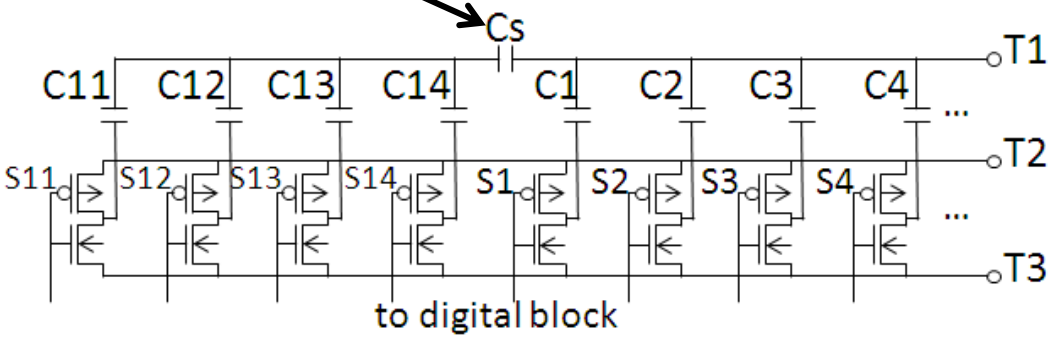


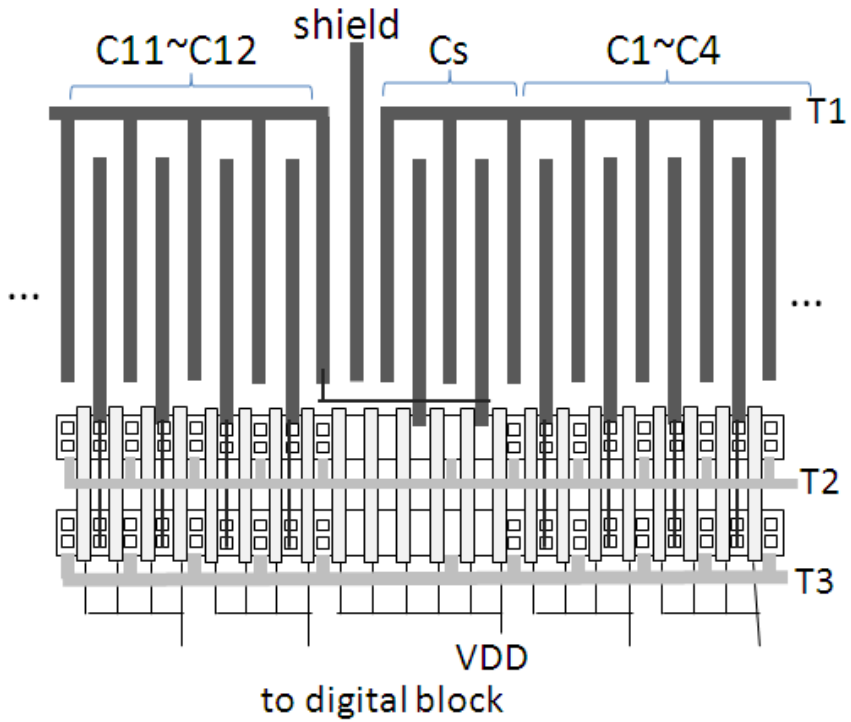
Monotonicity is guaranteed.
Better INL



Proposed method: scaling capacitor layout

- Scaling capacitor (2uint capacitance value) can be located in same slice except metal wires.
- It makes better match to keep same regularity.





Proposed method: experimental results

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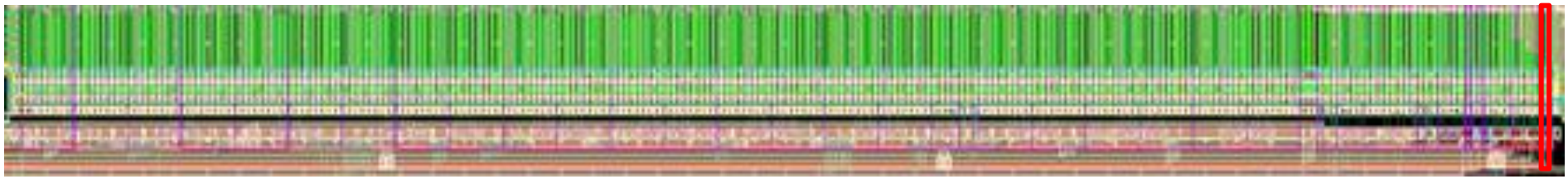
- Our silicon samples' experimental results
  - 12bit DAC in SAR ADC
  - DAC core size: 0.0035mm^2=230μm x 15μm (65nm) =1/2.8 of our previous design* (90nm)
  - Clock speed 1GHz. +20% higher then previous design*
  - Power consumption <2mW

*Z.Xu, M.Miyahara, A.Matsuzawa, "A 1ps-resolution Integrator -based Time-to-Digital Converter Using a SAR-ADC in 90nm CMOS", NEWCAS 2013 IEEE 11th International, 16-19

Layout



Proposed method: logic layout in slice

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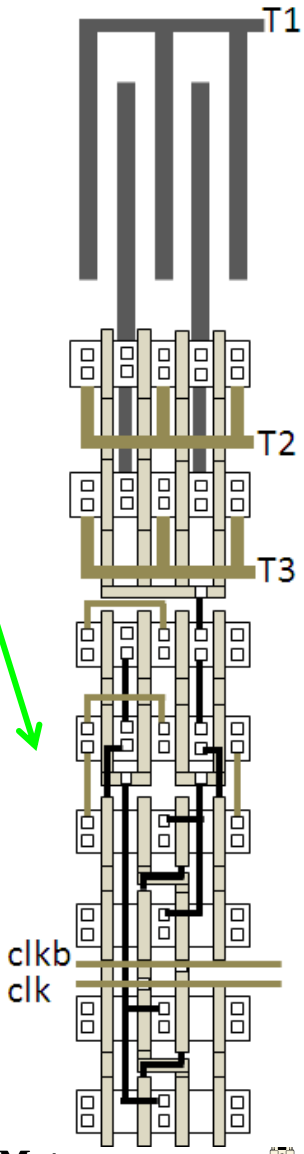
- Digital logic is also in sub-micron slice in-line, in addition to above
  - D flip-flop (DFF) is located in-line by using 4 gates x 6 rows
  - <several μm metal wire length. Much smaller stray C,R,L than previous. →Higher speed
  - Binary → thermometer coder can also be designed same size as DFF
  - Any logic can be created into 4 gate per slice



Proposed method: C+Sw+logic in slice

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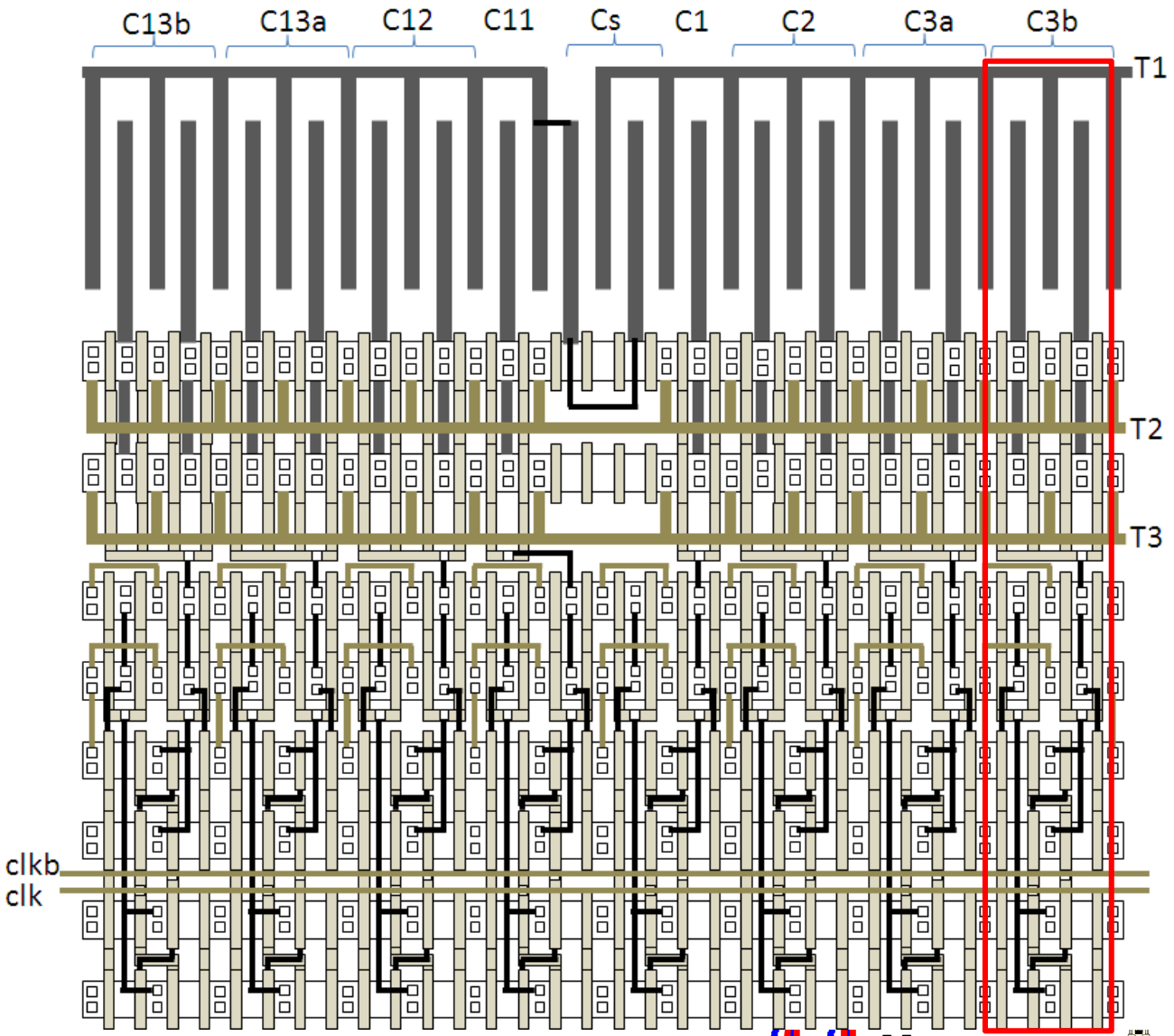
- Example of capacitor +switches +logic in slice.
- Half capacitor in a slice



Proposed method: Scalable along processes

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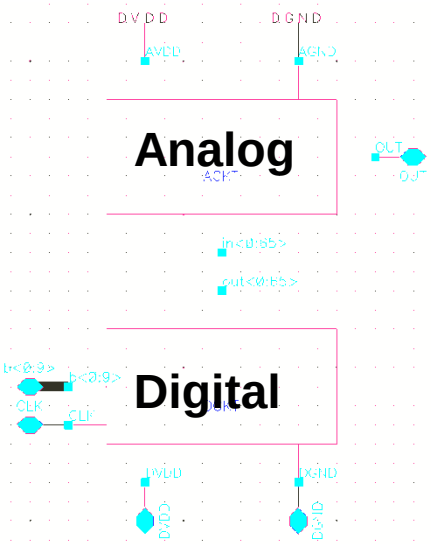
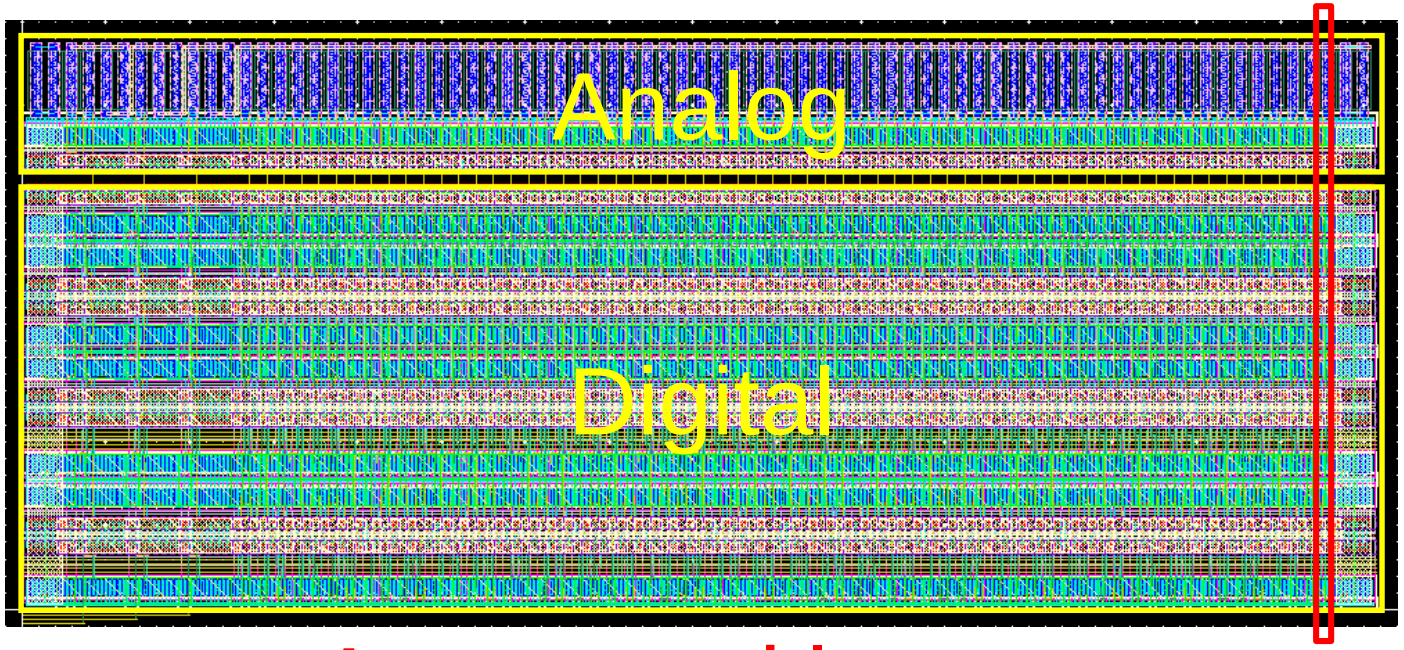
- Scalability along process nodes
  - Logic is scaled
  - MOS transistor switches are scaled
  - Metal width and gap of MOM capacitors are scaled
  - Metal wire width is scaled
  - Thermometer code arrows big capacitor mismatch (~50%error). Even smallest size capacitor can show enough performance

Hence, C-DAC by this method are scaled

Proposed method: R-DAC layout

- Apply to R-2R + segment 9bit DAC
  - 2R resistor based
  - R + switches + DFF + thermometer coder





Automated layout

"9ビットRDACの自動合成" 電子情報通信学会シリコンアナログRF研究会 2013年8月　盛他

Proposed method: R-DAC schematic

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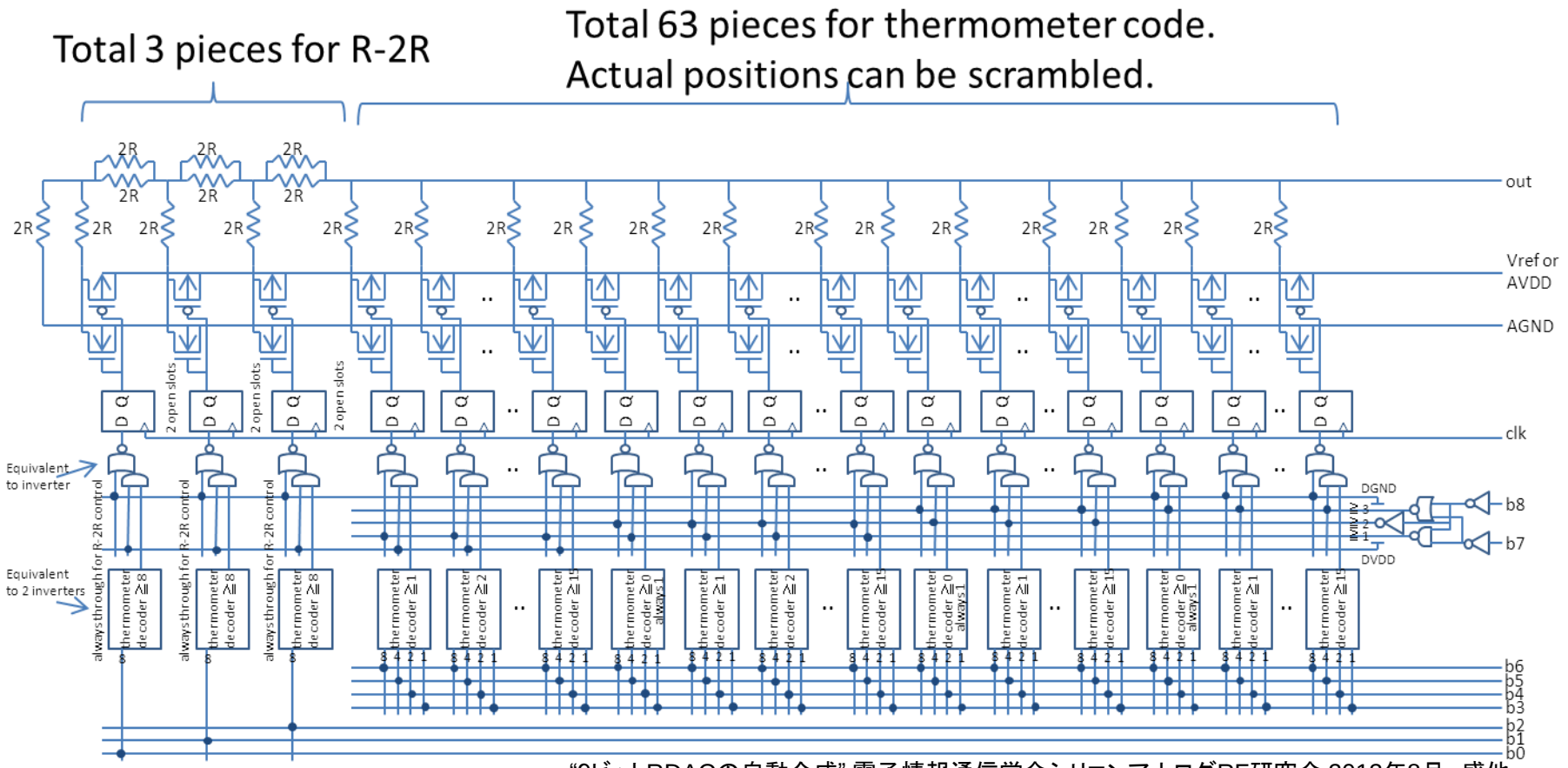
- Apply to R-2R + segment 9bit DAC
  - 2R resistor based
  - R + switches + DFF + thermometer coder



"9ビットRDACの自動合成" 電子情報通信学会シリコンアナログRF研究会 2013年8月　盛他

Conclusion

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- We proposed layout driven architecture and circuit design
  - Give layout 1st priority
  - Proposed sub-micron wide slice design
  - Quite small size (e.i. 1/2.8)
  - Known, quite small stray C,R,L
    →higher speed, lower power, etc.
    →<1fF switching is available.
  - Process scalable analog design