Proposal of layout-driven 1/2.8 size DAC design methodology

○菅原 光俊 *1*2, 盛　健次 *1*2, 李　承鍾 *1,　宮原　正也 *1, 松澤　昭 *1
Mitsutoshi Sugawara *1*2, Kenji Mori *1*2, S.J. Lee *1, Masaya Miyahara *1, Akira Matsuzawa *1
*1 Tokyo Institute of Technology 東京工業大学, *2 JST, CREST 独立行政法人科学技術振興機構
sugawara@ssc.pe.titech.ac.jp

Abstract: Previous D-to-A converter (DAC) design flow is architecture design → circuit design → layout design. We propose a layout-driven architecture and circuit design methodology to achieve leading edge DAC designs. Using the methodology, we considered the smallest size. We have successfully designed a sub-micron wide slice including unit capacitor and unit switches, shown in right figure. It earns extremely smaller parasitic capacitances, resistances and inductances, therefore significant higher speeds and lower powers are expected. Our new silicon samples of 12bit 1Gsps DAC in a SAR ADC has only 1/2.8 area of our previous design, and they have demonstrated +20% higher speeds.