Development of a scalable 12-bit SAR ADC
スケーラブル12bitSAR ADCの開発

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Matsuzawa & Okada Lab.

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- **Development goal**
  - **Frequency, performance, and power scalable ADC**
- **SAR ADC design**
  - **Circuit design**
  - **Capacitor design**
- **Measurement results**
- **Conclusion**

Goal: One ADC for versatile use

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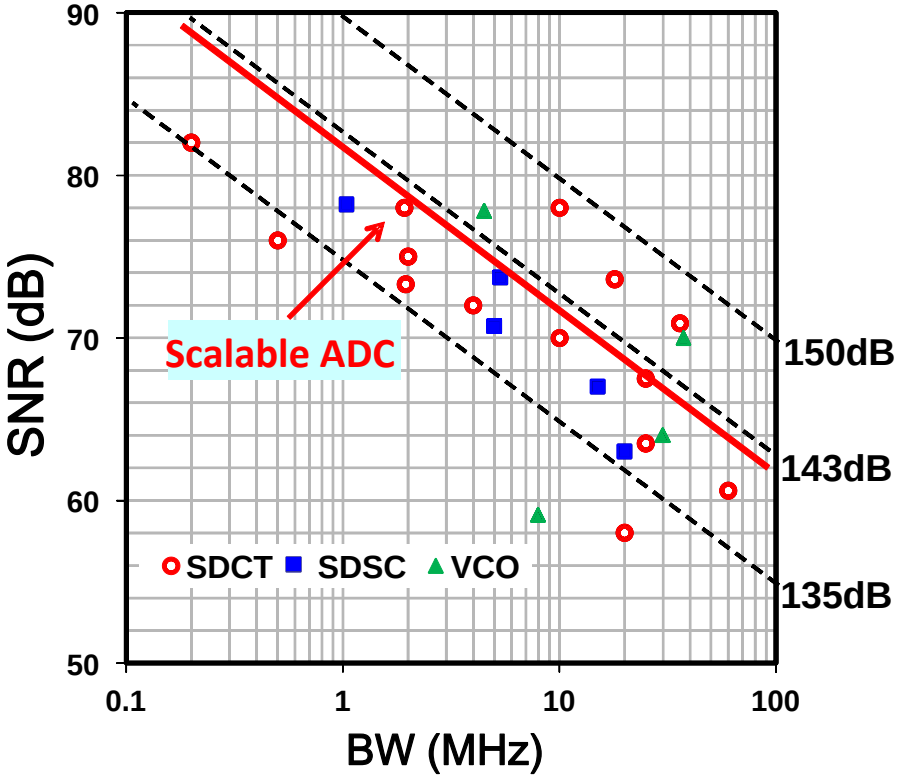
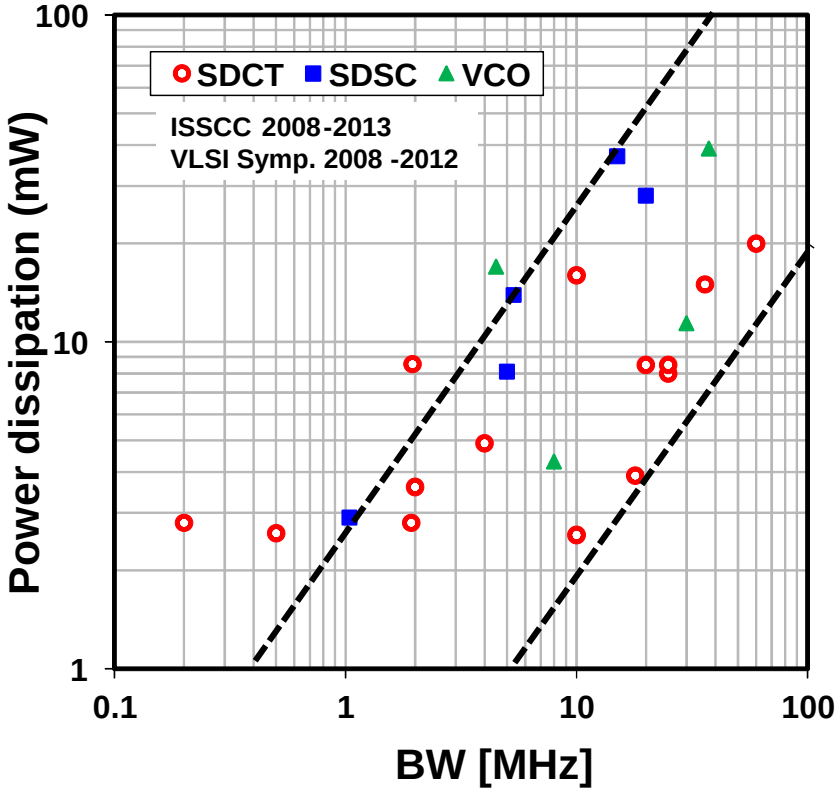
1. **Enough high SNR for wide signal bandwidth**
2. **Lowest power for wide conversion rate**
3. **Smallest occupied area**

$$SNR \approx SNR_0 - 10\log(BW)$$



$$P_d \approx K_1 \cdot BW \quad K_1: 0.2 \text{ -- } 3 \text{ (mW/MHz)}$$



Matsuzawa, A. "Digitally-Assisted Analog and RF CMOS Circuit Design for Software-Defined Radio," Chapter 7,Springer 2011.

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Block diagram of SAR ADC

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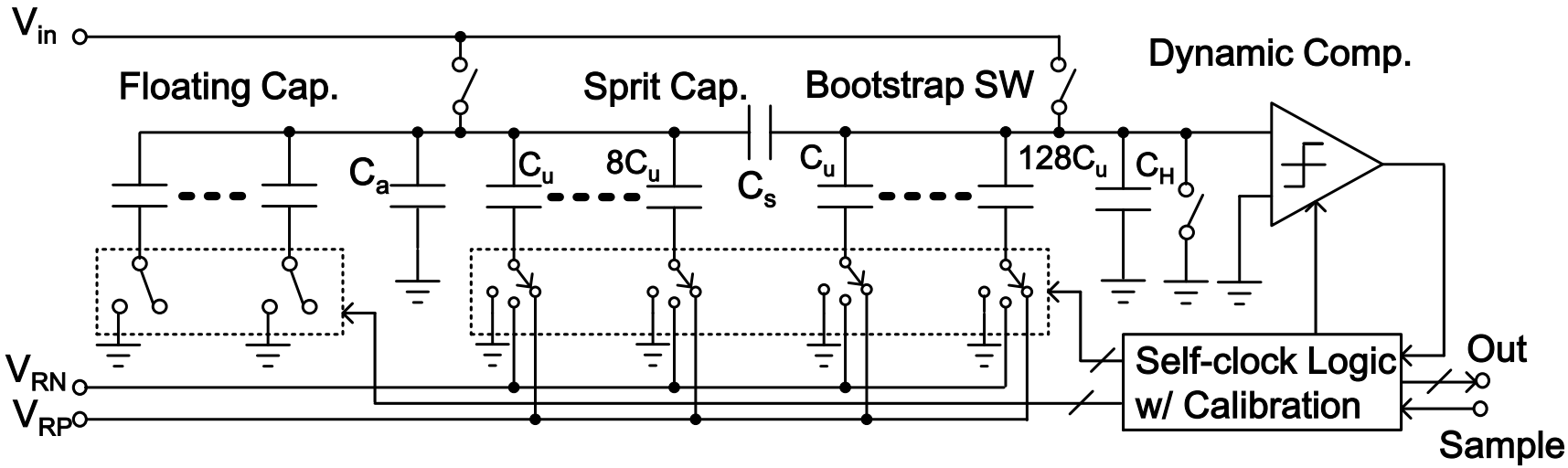
Sprit capacitor to reduce the total capacitance
Capacitance is determined by thermal noise
Calibration for mismatch Cap. and parasitic Cap.
Dynamic comparator to reduce power
Self clocking to avoid PLL and DLL



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Dynamic comparator

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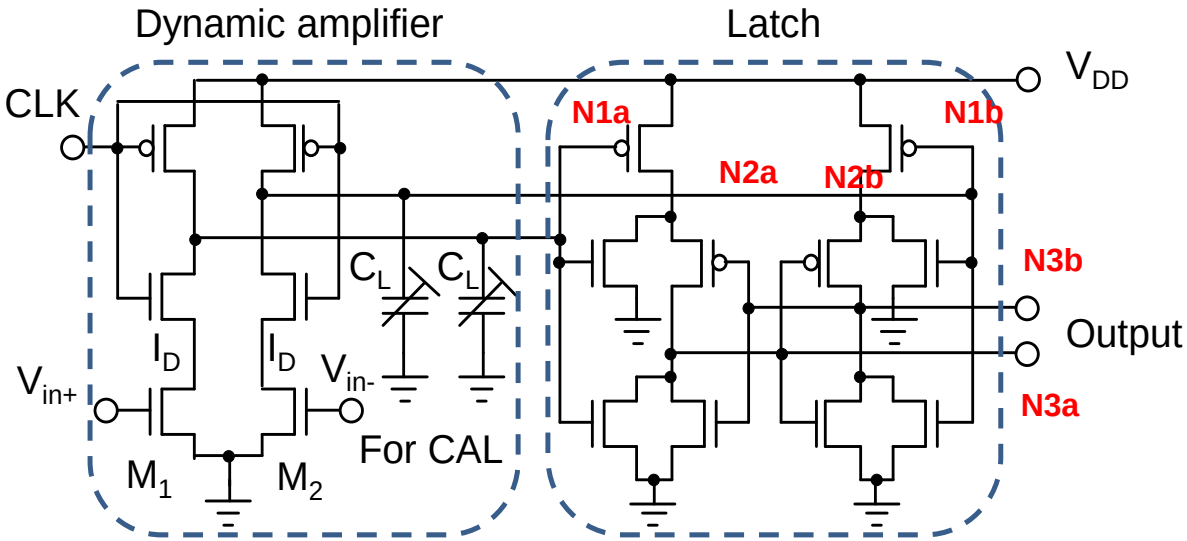
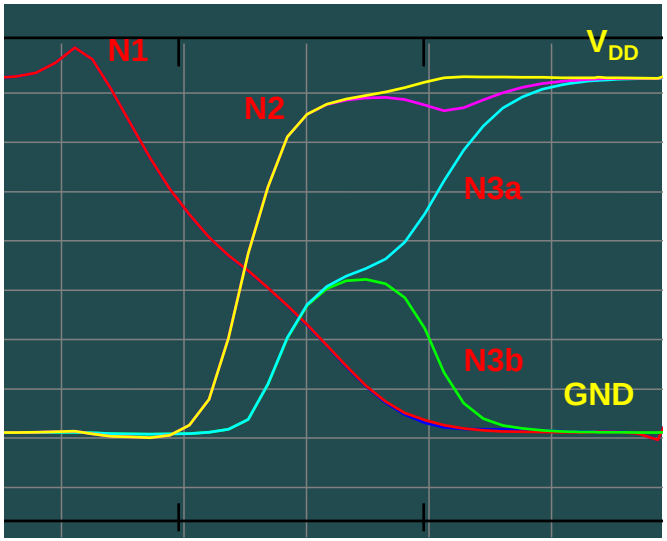
Low noise dynamic comparator to reduce power
No static current flows because of dynamic action
Load capacitance of the 1st stage determines the noise





M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," A-SSCC, Nov. 2008.

Yusuke Asada, Kei Yoshihara, Tatsuya Urano, Masaya Miyahara, and Akira Matsuzawa, "A 6bit, 7mW, 250fJ, 700MS/s Subranging ADC," A-SSCC, 5-3, pp. 141-144, Taiwan, Taipei, Nov. 2009.

Required capacitance and consumed Energy

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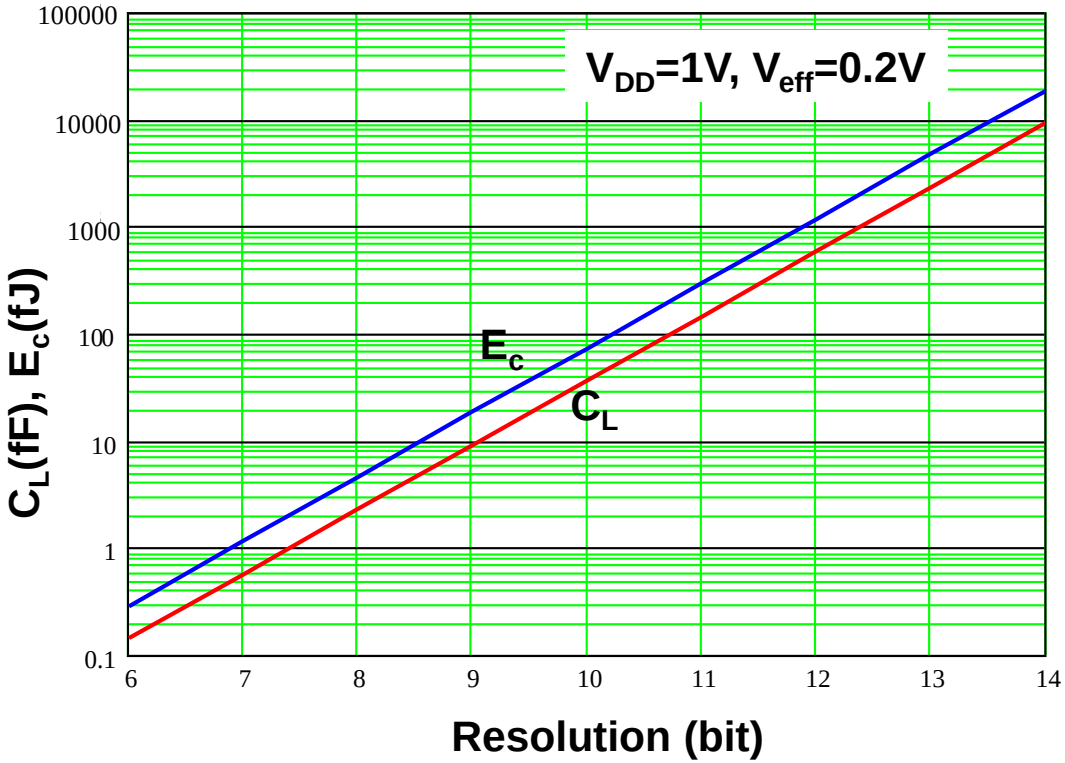
Proposed dynamic comparator can reduce the noise due to CMOS input of flip flop circuit, originally.
Node capacitance C_L should be increased for higher ADC resolution.

$$\overline{V_{n_i}^2} \approx 2\gamma \frac{kTV_{eff}}{C_L V_{DD}}$$

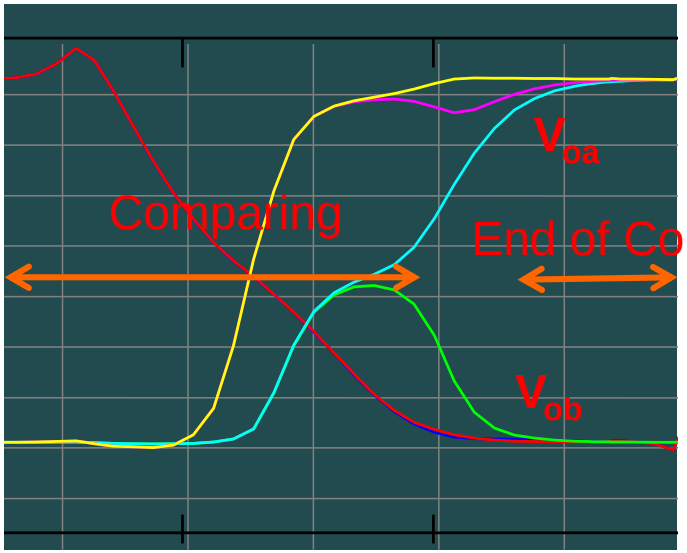
C_L=0.5pF is used

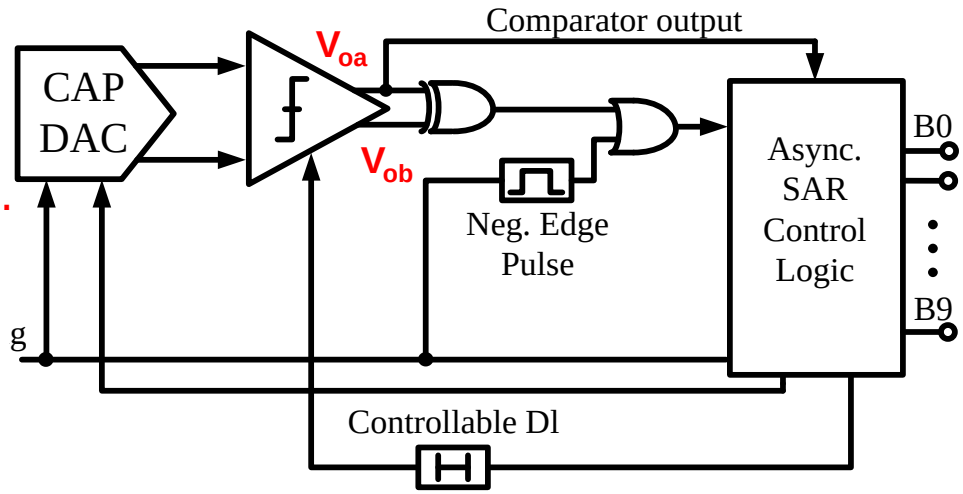


A. Matsuzawa, ASICON 2009, pp. 218-221, Oct. 2009.

Self clocking circuit

Nature of dynamic comparator
can detect the end of comparison.
The self clocking can avoid PLL and DLL.





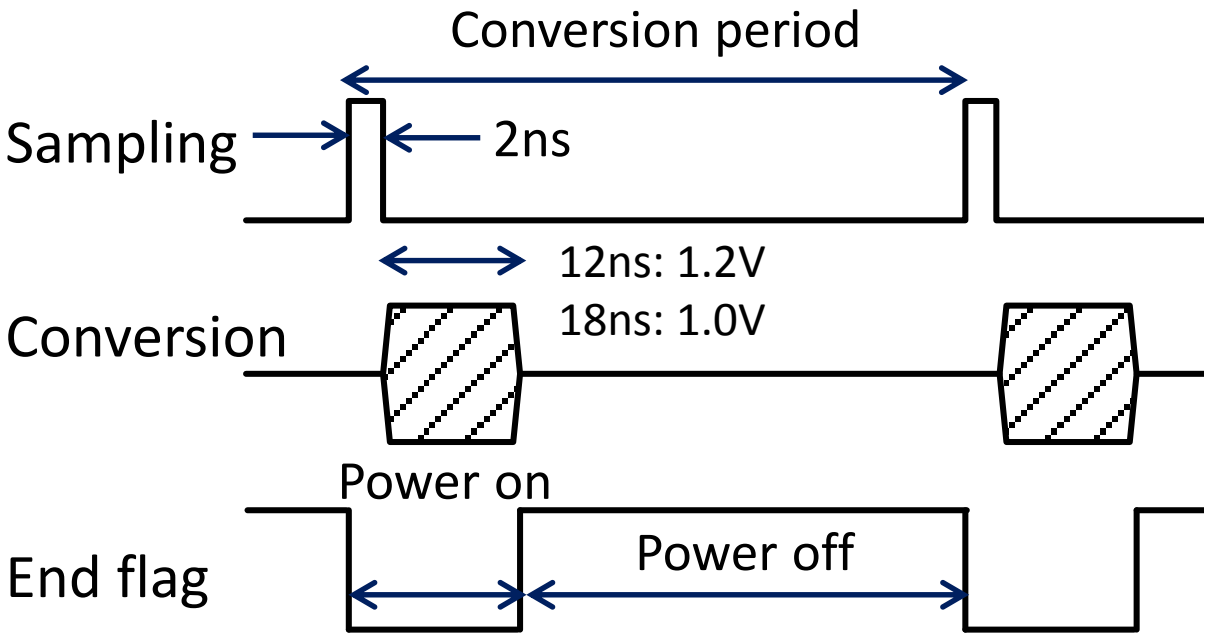
Self clocking circuit

Comparing period: Same Low states
End of comparison: Different logic states

Timing

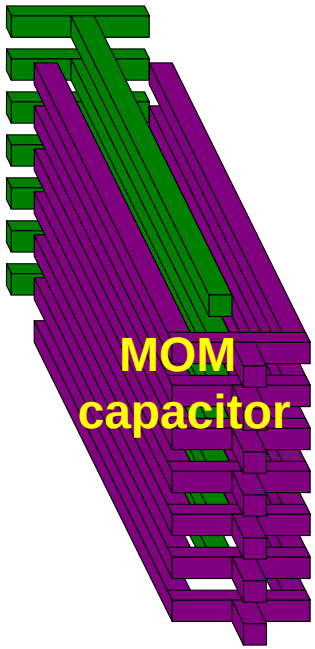
Only sampling pulse is required.

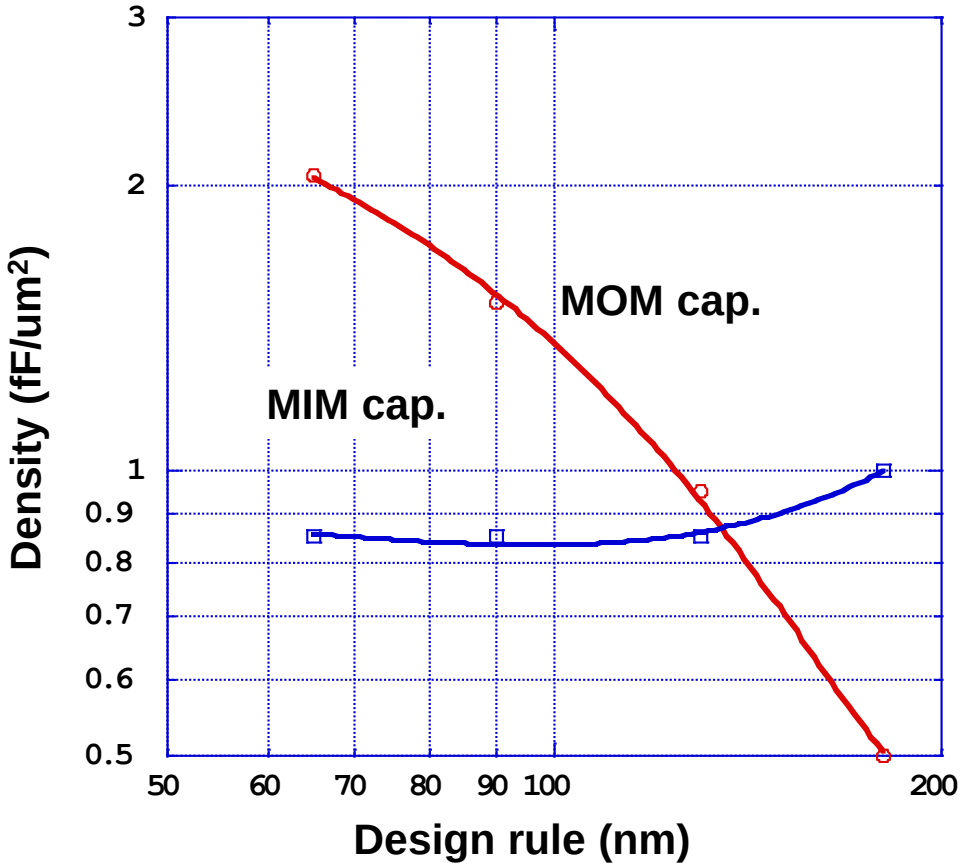
Conversion is finished within 12 ~ 18ns
Rest period can be used for power Shut off.



MOM capacitance

MOM capacitance is used to increase capacitor density and to reduce capacitor area.





Issue of MOM capacitor

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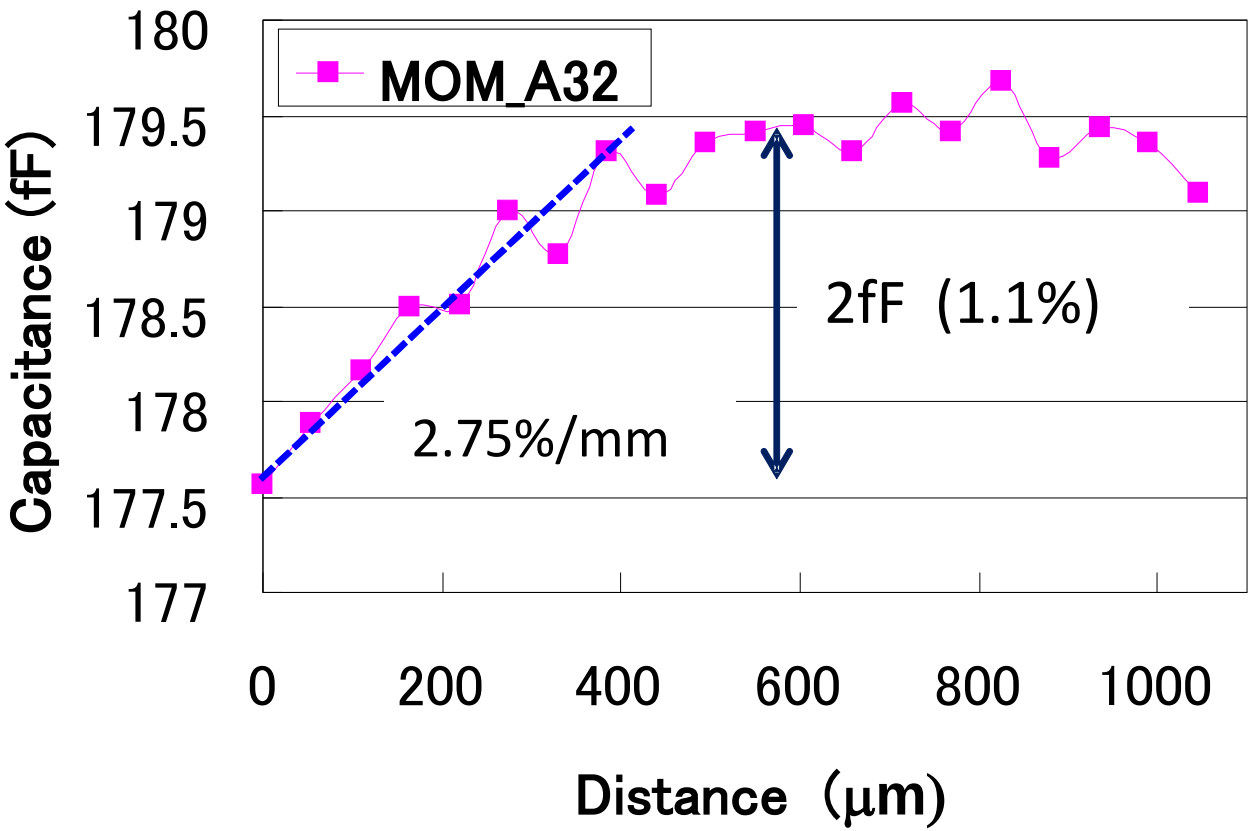
MOM capacitance has a large position dependence.
Calibration circuit is needed.



Linearity calibration

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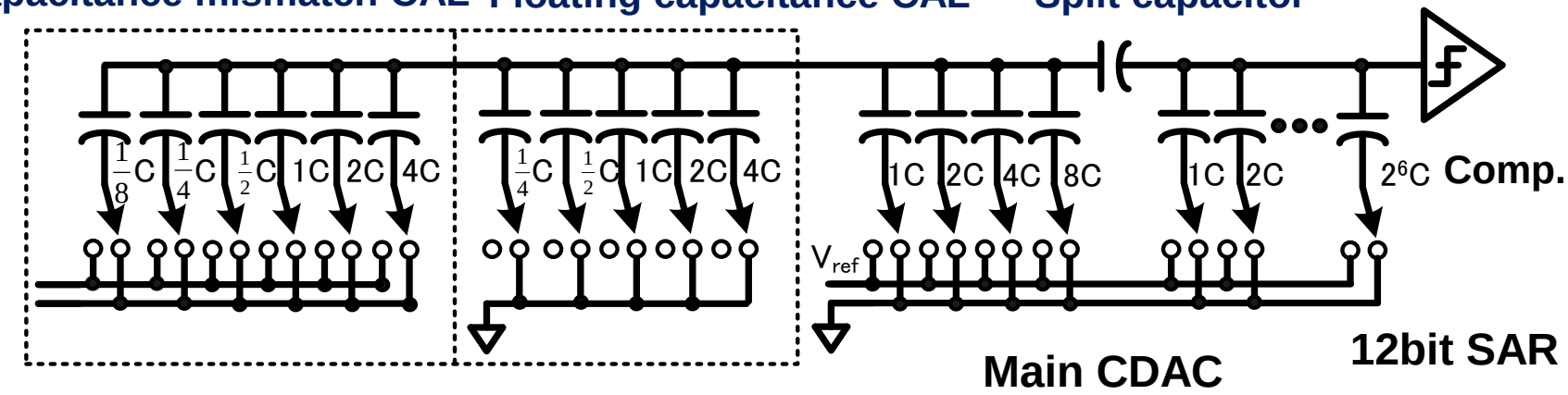
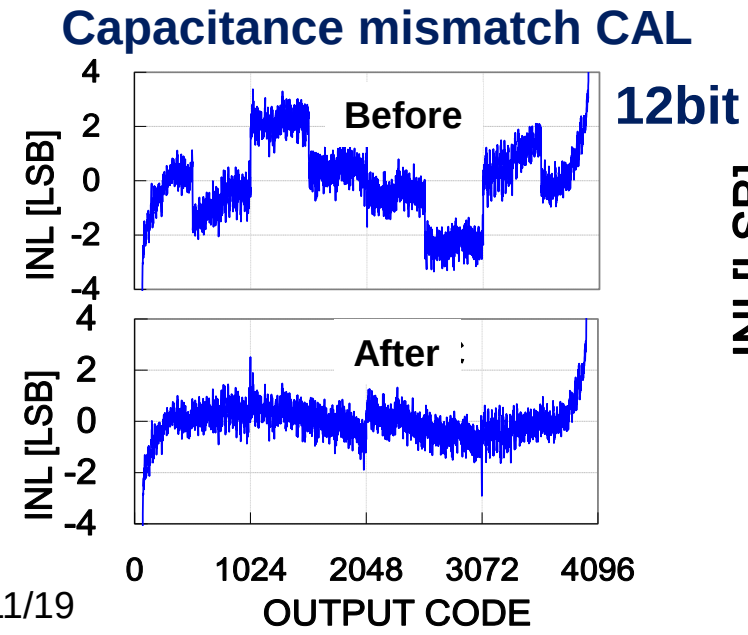
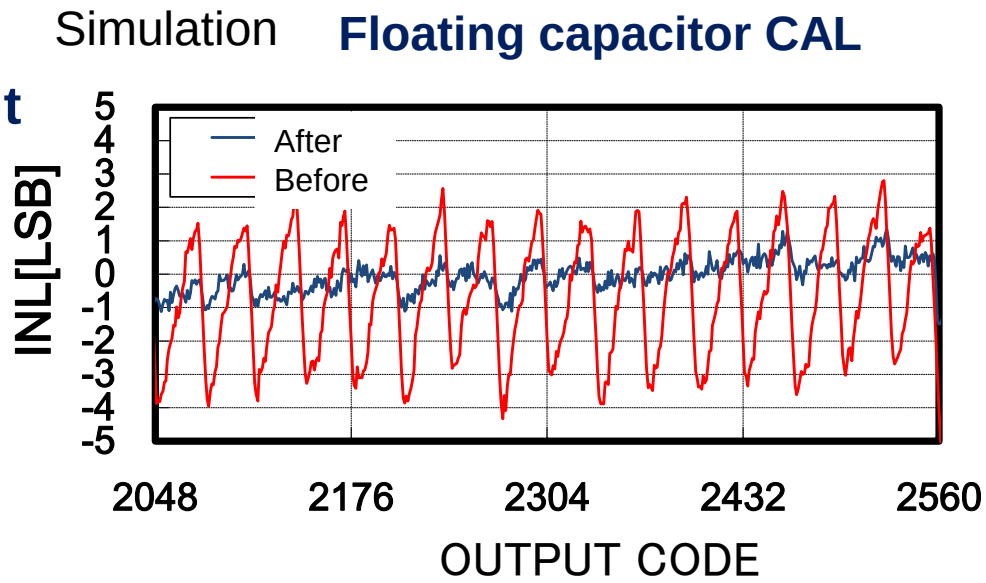
Capacitance mismatch and parasitic capacitance calibrations







Layout

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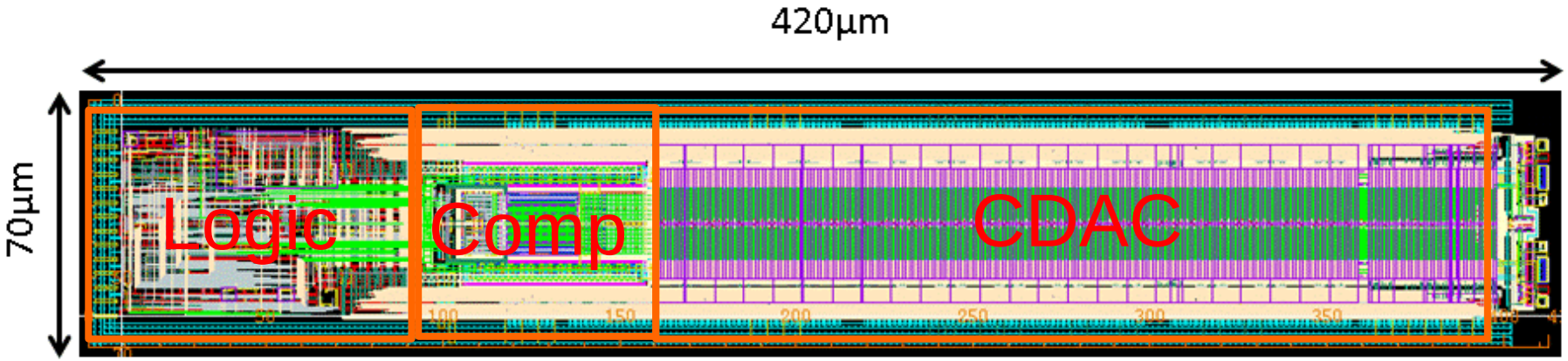
Small occupied area

Short cell for future interleaving architecture

65nm CMOS 0.03mm^2



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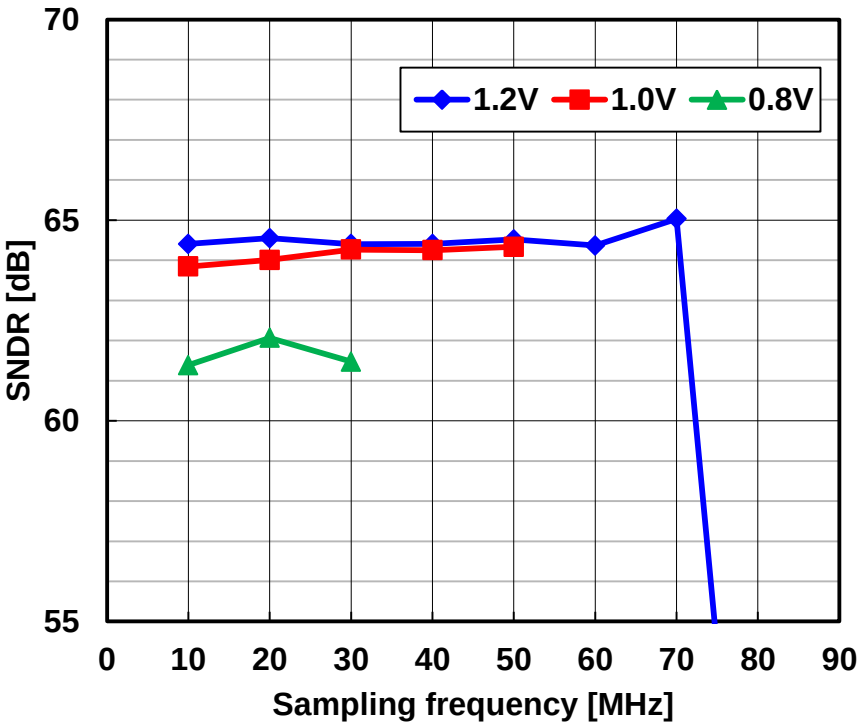
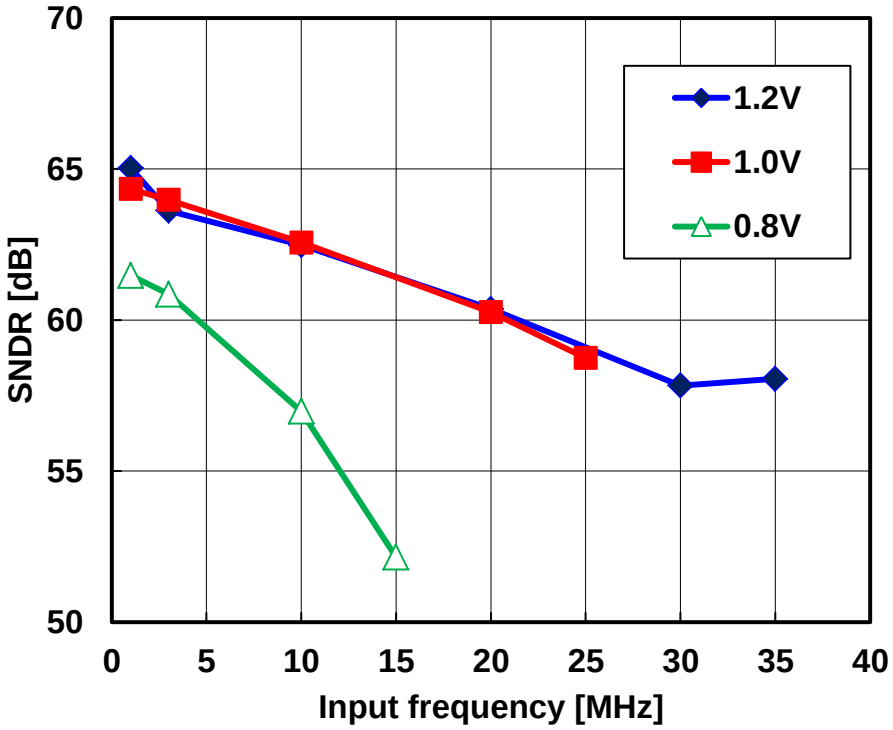
Measured results: SNDR

SNDR of 64dB is obtained for V_{dd} of 1.0V and 1.2V.
SNDR is degraded at V_{dd} of 0.8V.





Linearity improvement by Calibration

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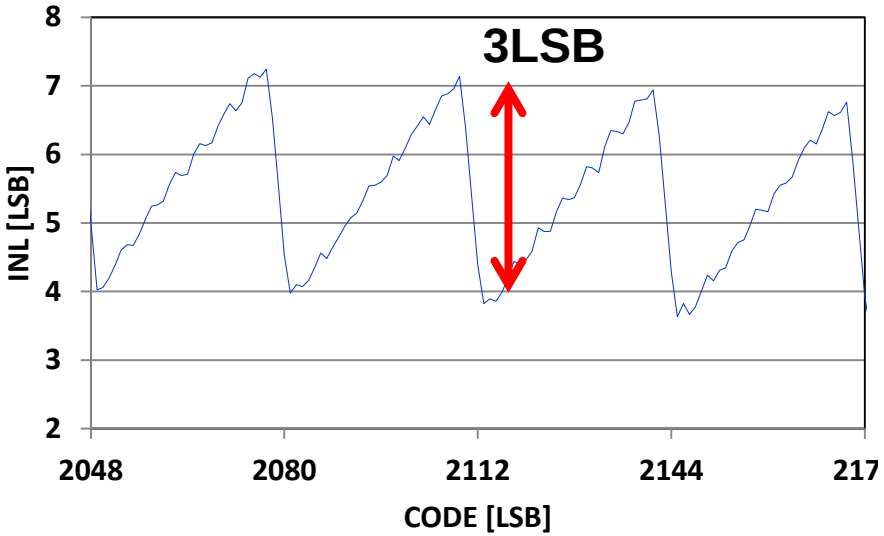
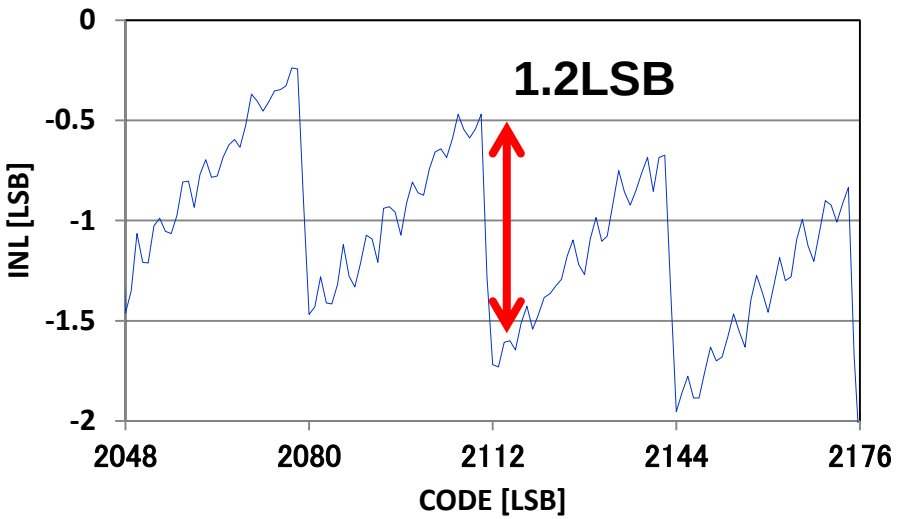
Parasitic capacitance of sprit capacitance causes the linearity error of 3 LSB without calibration, and it can be reduced to 1.2LSB with calibration.

Without CAL.



With CAL.



Power dissipation

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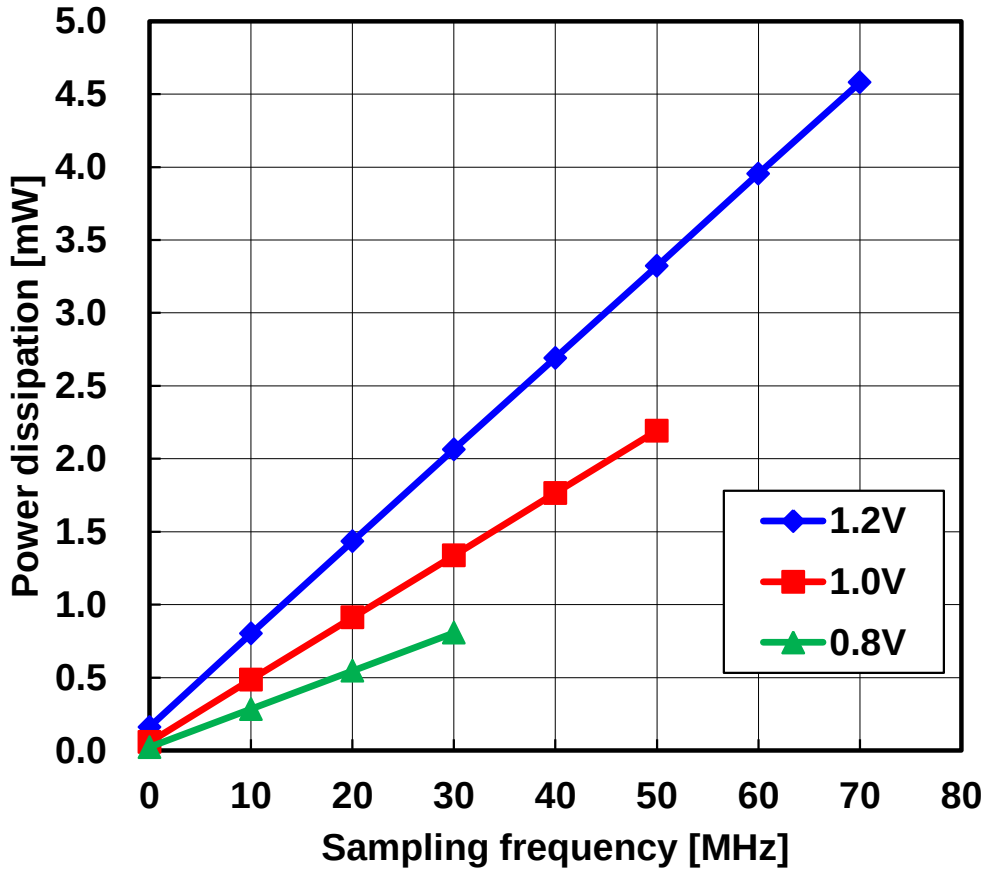
Power scalable ADC can be realized.

Power dissipation is very proportional to sampling frequency.
Low voltage operation is effective to reduce power dissipation.
High conversion frequency of 70MHz is achieved.



Performance comparison

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- Maximum conversion speed of 70MSps
- Lowest operating voltage of 0.8V
- Lowest power dissipation of 2.2mW at 50MSps
- Lowest FoM (DC) of 28fJ
- Smallest area of 0.03mm^2

12bit SAR ADCs

	This work			[3]	[4]
Resolution (bit)	12			12	12
V_{DD} (V)	0.8	1	1.2	1.2	1.2
fsample (MHz)	30	50	70	45	50
Pd (mW)	0.8	2.2	4.6	3	4.2
SNDR (dB)	62	64	65	67	71
FoM (fJ) Nyq/DC	81/28	62/33	100/45	36/31	36/29
Technology (nm)	65			130	90
Occupied area(mm^2)	0.03			0.06	0.1

[3] W. Liu, P. Huang, Y. Chiu, ISSCC, pp. 380-381, Feb. 2010.
[4] T. Morie, et al., ISSCC, pp.272-273, Feb. 2013.

SNR and P_d vs. signal bandwidth

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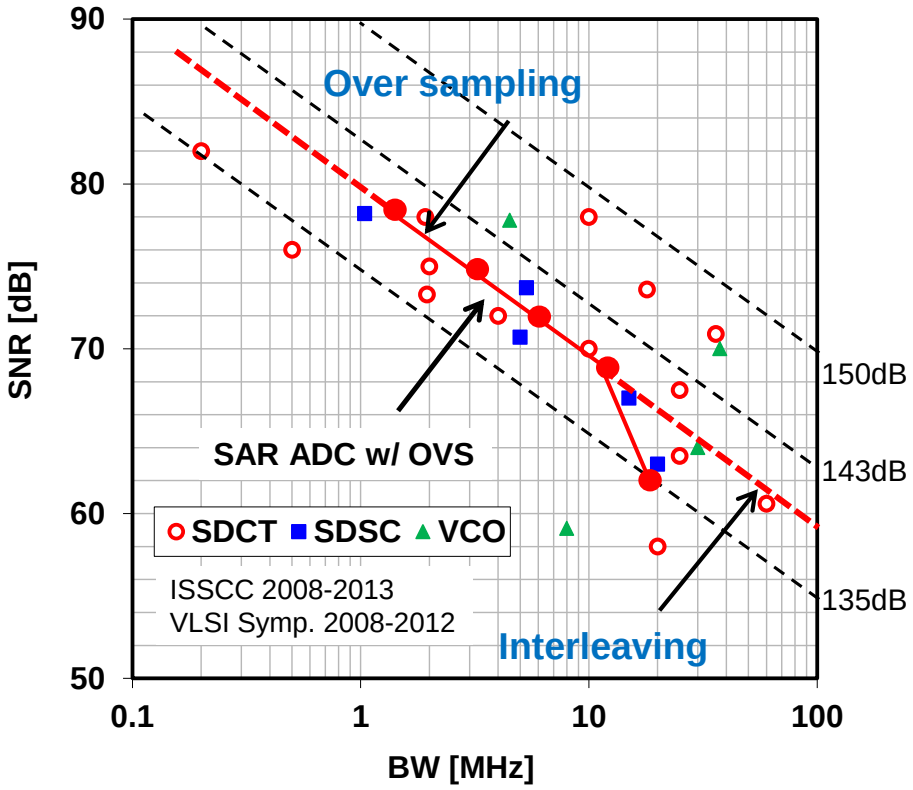
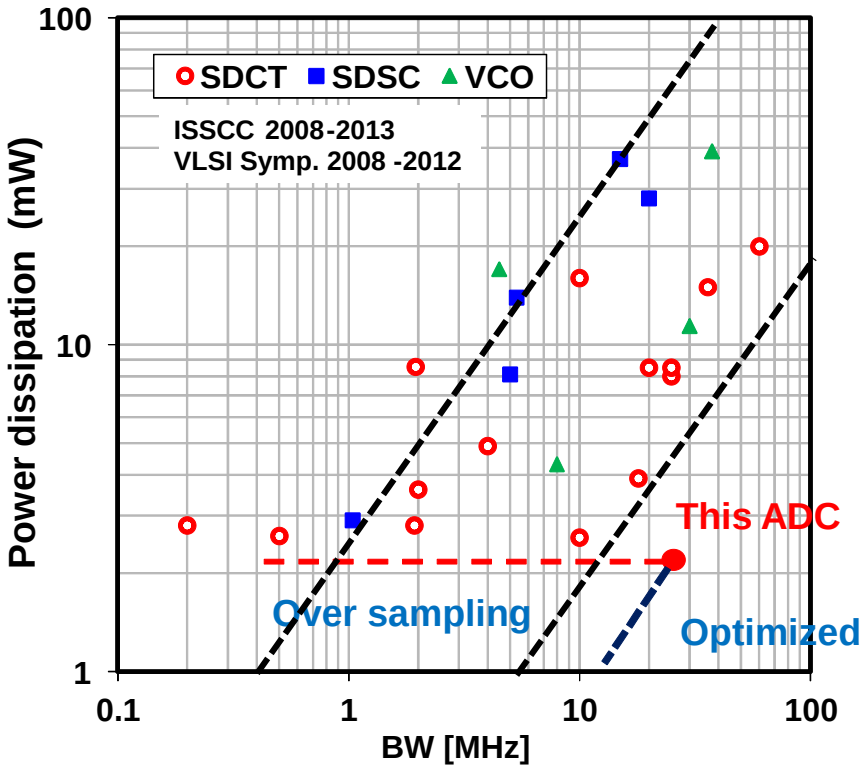
SNR of 70dB at 10MHz input and 78dB at 1.5MHz is attained by digital filter (Over sampling).
Frequency and performance scalable ADC is realized.
Power dissipation is the lowest and conversion rate scalable..
Interleaving will expand the BW in future.

1V, 50MSps Operation





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Conclusion

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- **12bit SAR ADC is designed**
  - **Low noise dynamic comparator**
  - **MOM capacitor**
  - **Mismatch Cap. and parasitic Cap. Calibration**
  - **Self clocking circuit**

- **The SAR ADC achieves**
  - **Maximum conversion speed of 70MSps**
  - **Lowest V_{dd} of 0.8V and P_d of 2.2mW at 50MSps**
  - **Smallest area of 0.03mm^2**

- **Frequency, performance and power scalable ADC**
  - **70dB for BW of 10MHz in, 78dB for BW of 1.5MHz**
  - **Power dissipation is perfectly proportional to sampling frequency**
  - **Expected expand of BW by interleaving**