A Sub-harmonic Injection-locked Frequency Synthesizer with Frequency Calibration Scheme for Use in 60GHz TDD Transceivers

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Abstract – A 58.1-to-65.0 GHz frequency synthesizer using sub-harmonic injection-locking technique is presented. The synthesizer can generate all 60GHz channels defined by IEEE 802.15.3c, wirelessHD, IEEE 802.11ad, WiGig, and ECMA-387. A frequency calibration scheme is proposed to monitor frequency shift resulting from environmental variations. Implemented in a 65nm CMOS process, the synthesizer achieves a typical phase noise of -117 dBc/Hz @10MHz offset from a carrier frequency of 61.56 GHz.

I. Introduction

Recently, several PLLs [1-4] have been reported for millimeter-wave wireless system. Among these publications, the PLL using sub-harmonic quadrature ILO is preferred due to the best phase noise performance at 60GHz. However, due to inaccurate device modeling at mm-wave band, it is difficult to guarantee the proper operation of the 60GHz ILO, especially including process-voltage-temperature (PVT) variations. Thus, this paper proposes a sub-harmonic injection-locked synthesizer with frequency calibration scheme to address the above mentioned issue [5].

II. Proposed 60GHz Frequency Synthesizer

A. General Consideration

Fig. 1 (a) and (b) shows a conceptual diagram of the 60GHz frequency synthesizer with digital calibration using Injection Locked Frequency Divider (ILFD), and a mixer for frequency reduction, respectively. For TDD systems, transmitter (TX) and receiver (RX) operate in different time slots. Thus, the calibration of 60GHz ILO for TX can be performed during RX time slots, and the calibration of 60GHz ILO for RX can be performed during TX time slots. However, the time duration is limited to 7.2 μs only for each TX and RX slot according to IEEE 802.11ad, imposing a strict requirement for the calibration time of the 60GHz ILO. Conventional mm-wave calibration method [1], as shown in Fig. 1 (a), is infeasible for calibrating ILO, since two calibration procedures (Step1: calibrate ILFD, step2: calibrate ILO) are required to carry out sequentially, which is time-consuming.

In order to reduce the calibration time, frequency down-conversion using mixer is employed as shown in Fig.1 (b). The process of calibration is carried out when the 20GHz PLL is locked. At the initial state or during TX time slots, the ILO for RX outputs its free-running frequency, and the output of ILO for RX is down-converted to a frequency around 20 GHz by a mixer, through doubling of the 20GHz PLL injection signal. After two separate divider chains, the frequency coming from the output of mixer and the 20GHz PLL are compared using digital calibration circuits. The output of digital calibration circuit directly controls the digital code for a digital-to-analog converter, giving rise to adjust the ILO free running frequency. After several reference cycles, the 60GHz ILO free-running frequency is closed to the 3 times of the 20GHz PLL output.

B. Circuit Description

The proposed 60GHz frequency synthesizer mainly consists of a 20GHz PLL, a 60GHz Quadrature ILO [6], a frequency down-converting circuit, and a digital calibration circuit. The block diagram of proposed 60GHz synthesizer is depicted in Fig. 2. The down-converting circuit is composed of a frequency doubler, a mixer, and two notch filters as shown in Fig. 3. The frequency doubler is utilized for generating a second harmonic of the input signal from the 20GHz PLL. The single-ended RF output from the frequency doubler at frequency around 40GHz and differential LO output signal from ILO at frequency around 60GHz are mixed through a single-balanced mixer. Output signal of the mixer carries 20GHz output and undesirable signals caused by strong LO input power. Thus, notch filters are implemented to suppress the 60GHz LO feedthrough from the input stage of the mixer. Finally, output signal goes through buffers and divider chain before performing digital calibration.

III. Measurement Results

The frequency synthesizer is fabricated in a 65nm CMOS process. The core chip area is 1.9mm×2 mm. When the frequency of reference clock is 24MHz, the synthesizer can generate all 60GHz channel bands: 58.32GHz, 59.4GHz, 60.48GHz, 61.56GHz, 62.64GHz, 63.72GHz, and 64.8GHz. The frequency synthesizer consumes 72mW from a 1.2V power supply. If the intermittent operation is disabled, the calibration circuits including down-converting circuits and digital circuits consume 65mW additionally. As shown in Fig. 4, the typical measured phase noise is -96 dBc/Hz @1MHz offset, and -117 dBc/Hz @10MHz offset at a carrier frequency of 61.56 GHz. The chip microphotograph is shown in Fig.5. Table I compares the proposed synthesizer with the state-of-art publications.

IV. Conclusion

A 60GHz frequency synthesizer with background calibration which can support IEEE 802.15.3c, wirelessHD, IEEE 802.11ad, WiGig, and ECMA-387 TX/RX front end is reported. With careful design, the proposed synthesizer can be suited for millimeter-wave TDD systems.

Acknowledgements

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References

[1]K. Scheir, *et al.*, "A 57-to-66GHz Quadrature PLL in 45nm Digital CMOS,"*ISSCC*, 2008.
[2]C. Marcu, *et al.*, "A 90 nm CMOS Low-Power 60 GHz Transceiver With Integrated Baseband Circuitry," *JSSC*, 2009.
[3]H. Hoshino, *et al.*, "A 60-GHz Phase-Locked Loop with Inductor-less Prescaler in 90-nm CMOS," *ESSCIRC*, 2007.
[4]A. Musa, *et al.*, "A Low Phase Noise Quadrature Injection Locked Frequency Synthesizer for MM-Wave Applications," *JSSC*, 2011.
[5] W. Deng, T. Siriburanon, A. Musa, K. Okada, and A. Matsuzawa, "A 58.1-to-65.0GHz Frequency Synthesizer with Background Calibration for Millimeter-wave TDD Transceivers," *IEEE European Solid-State Circuits Conference* (*ESSCIRC),* pp. 201-204, Sep. 2012.
[6]K. Okada, *et al.*, "A 60GHz 16QAM/8PSK/QPSK/BPSK Direct Conversion Transceiver for IEEE 802.15.3c," *ISSCC*, 2011

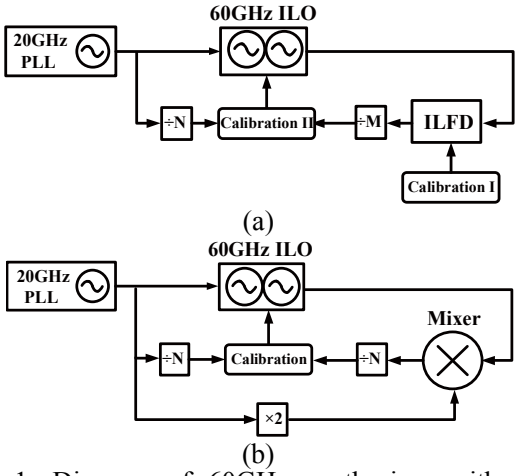

Fig.1. Diagram of 60GHz synthesizer with (a) conventional calibration method, and (b) proposed calibration method.

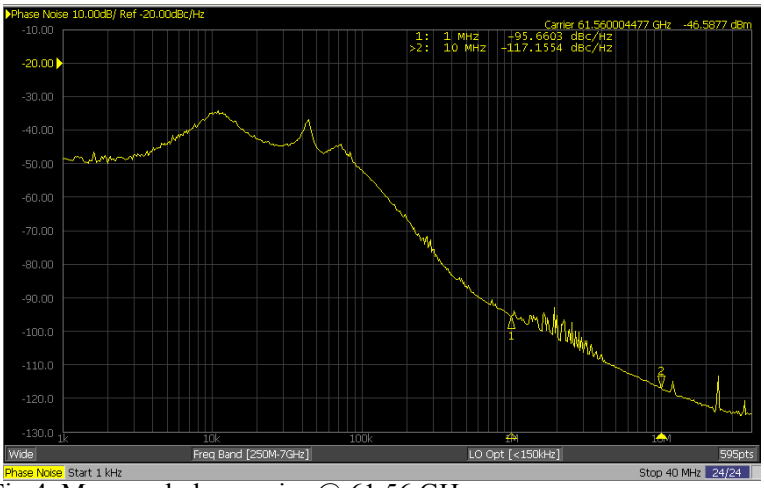

Fig.4. Measured phase noise @ 61.56 GHz.

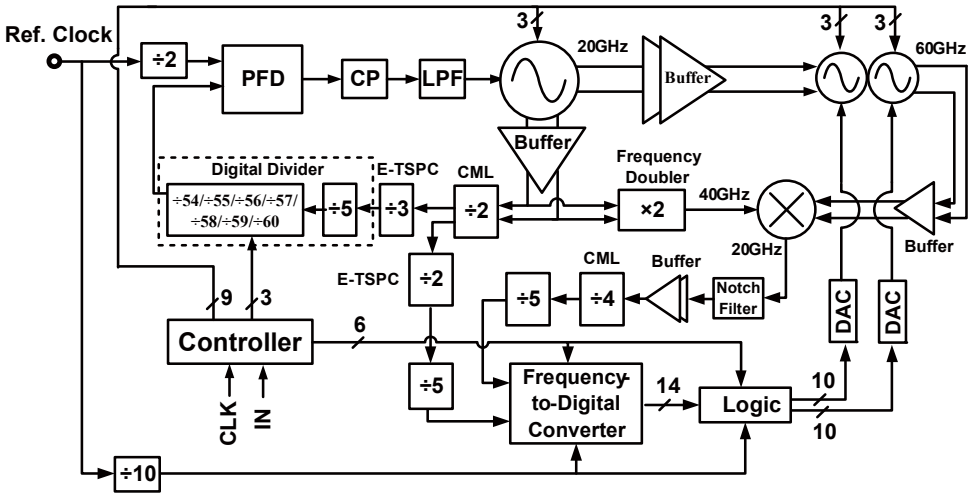

Fig.2. Block diagram of the proposed 60GHz frequency synthesizer.

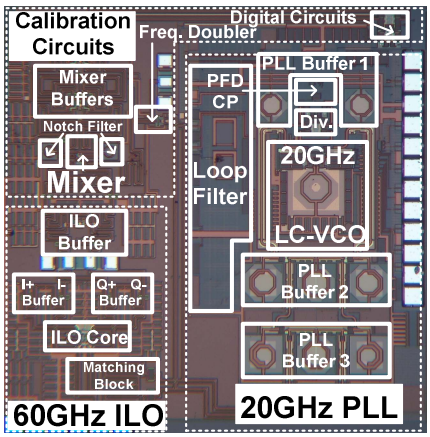

Fig.5. Chip micrograph

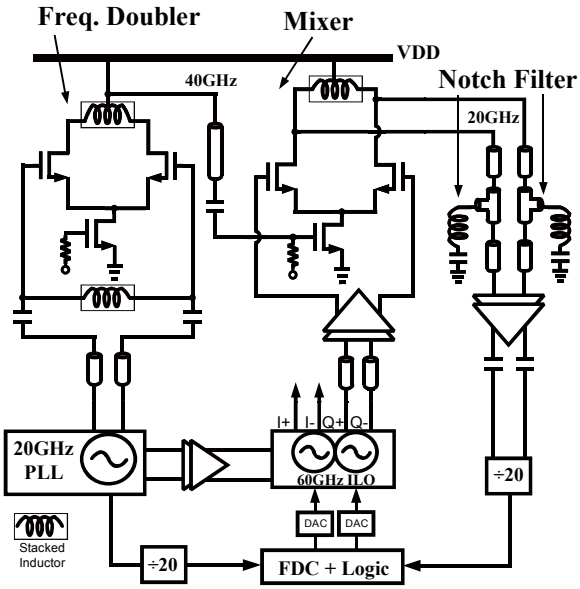

Fig.3. Schematic of down-converting circuits.

TABLE I PERFORMANCE COMPARISON BETWEEN THE-STATE-OF-THE-ART 60GHZ FREQUENCY SYNTHESIZERS

	Features	Freq. [GHz]	Phase Noise [dBc/Hz]	Pdc [mW]	Background Calibration
[1]	QVCO @ 60GHz Foreground Calibration	57-66	-75@1	78	No
[2]	Push-push VCO@30GHz Hybrid Coupler	59.4-64	-73@1 -112@10	76	-
[3]	Sub-harmonic Injection	58-63	-73@1 -112@10	80	No
[4]	Diff. VCO @ 60GHz	61-63	-80@1 -112@10	78	No
This work	Sub-harmonic Injection Background Calibration	58.1-65.0	-96@1 -117@10	72	Yes