A Fractional-N Harmonic Injection-locked Frequency Synthesizer with 10MHz-6.6GHz Quadrature Outputs for Software-Defined Radios

Wei Deng, Ahmed Musa, Kenichi Okada, and Akira Matsuzawa
Dept. Physical Electronics, Tokyo Institute of Technology
2-12-1-S3-27, Ookayama, Meguro-ku, Tokyo 152-8552 Japan.
Tel/Fax: +81-3-5734-3764, E-mail:deng@ssc.pe.titech.ac.jp

Abstract – This paper presents an area-efficient frequency synthesizer with a quadrature phase output using a fractional-*N* injection-locking technique for software-defined radios. A background calibration scheme is proposed to compensate for the PVT variations. Implemented in a 65nm CMOS process, this work demonstrates 10 MHz to 6.6 GHz continuous quadrature frequency coverage, while only occupies a small area of 0.38 mm^2 and consumes 16-26 mW depending on output frequency, from a 1.2 V power supply. The normalized phase noise achieves –135.3 dBc/Hz at 3 MHz offset, and -95.1 dBc/Hz in-band phase noise at 10 kHz offset, from a 1.7 GHz carrier frequency.

I. Introduction

Software-defined radios (SDR) are expected to receive various modulated frequency channel in a wide frequency spectrum from 10 MHz to 6 GHz. In order to support the frequency-agility property, frequency synthesizers for SDR need to cover a very wide range of output frequencies with proper channel spacing, performing low phase noise and low power consumption throughout the entire tuning range, while consuming small chip area.

Several approaches have been proposed in literature for wideband frequency synthesizer [1-4]. These methods, however, suffer from large chip area due to the employment of at least two or more LC resonators, large power consumption, and non-quadrature output. In this paper, an area/power efficient frequency synthesizer with quadrature output [5] is realized using fractional-N injection-locking method and digital calibration technique.

II. Proposed SDR Frequency Synthesizer

Fig. 1 shows the architecture of the frequency synthesizer. The core delta-sigma fractional-N PLL has a frequency coverage from 7.2 to 10.3 GHz. Unlike the present SDR frequency synthesizers with two or more LC resonators inside, the core PLL in this work employs only one LC resonator oscillating at high frequencies where small inductors are used, leading significant reduction of chip area. For frequencies between 1.5 GHz and 6.6 GHz, a fractional-N ILFD with a modulus of 4/3, 3/2, 5/3, 2, 5/2, 3, 4, 5 is used to divide down the frequency of the core PLL output signal [6]. Then lower frequencies are generated by a programmable output divider chain with a modulus of 2^N, N=0, 1…7. By using a 16-bit delta-sigma modulator in the core PLL, a frequency resolution lower than 10 kHz is achieved over the entire frequency range.

In the presented frequency synthesizer, the core PLL with a minimum tuning range of 14.3% is sufficient, since the following fractional-N ILFD relaxes the requirement for tuning range [6]. Generally speaking, direct-injection method is capable of divide-by-N operation. Nevertheless, odd-numbered division suffers from considerably narrow locking range, since multiple outphased injections disturb the injection-locking operation as shown in Fig. 2. In this work, input signal from the core PLL is injected to I-part of the ring oscillator through a gating stage to remove wanted injections, which helps to improve the locking range. Fig. 3 shows the detailed schematic of fractional-N ILFD. The quadrature outputs are generated by a dual-coupled differential ring oscillator.

It is seen that gating function can help to eliminate unwanted injections, however, the locking range is still limited, far from enough to guarantee the proper operation of fractional-N injection, especially including PVT variations. Thus, a digital calibration scheme is proposed to compensate the environmental variations. Noted the fractional divide ratio is preset by activating the corresponding path in MUX1 and MUX2. The calibration circuit works as a frequency-locked loop (FLL). After several reference cycles when the FLL is settled, the ratio between the core PLL frequency and the ILFD free-running frequency is approximately equal to the preset fractional division ratio. This FLL can run as a background calibration to monitor the ILFD frequency over environmental variations.

III. Measurement Results

This frequency synthesizer is implemented in a 65nm CMOS process. Fig. 4 shows the synthesizer output spectrum at 9.36 GHz. The reference spur is -64 dBc. Fig. 5 shows the measured phase noise at 8.928 GHz. Fig. 6 shows shows the chip micrograph, which only occupies 0.38mm^2. Table I summaries and compares the synthesizer performance. The total power consumption is 16-26 mW depending on various output frequencies.

IV. Conclusion

This paper presents an area/power efficient frequency synthesizer with a quadrature phase output [5]. With carful design, the proposed frequency synthesizer can be well suited for software-defined radios and cognitive radios.

Acknowledgements

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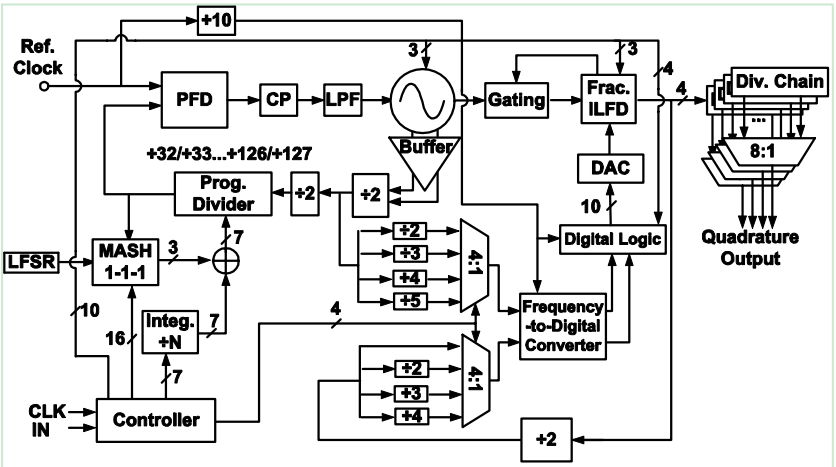

Fig.1. Detailed block diagram of the proposed SDR synthesizer.

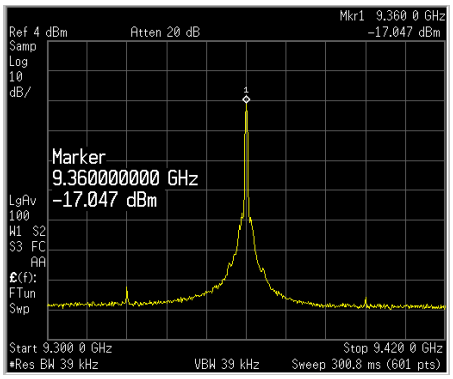

Fig.4. Measured spectrum at 9.36 GHz.

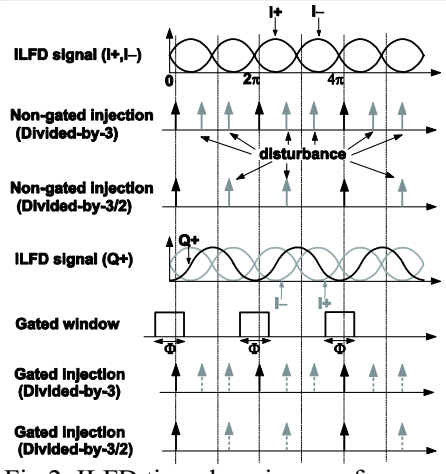

Fig.2. ILFD time domain waveforms.

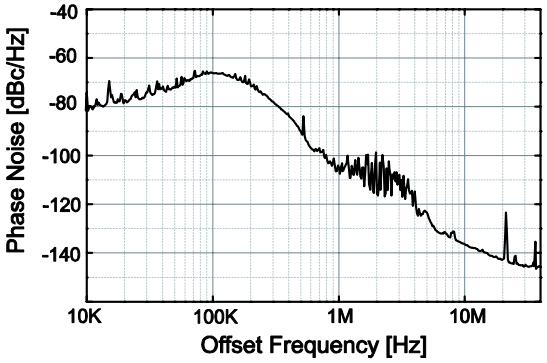

Fig.5. Measured phase noise at 8.928 GHz

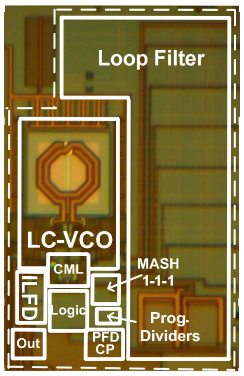

Fig.6. chip micrograph.

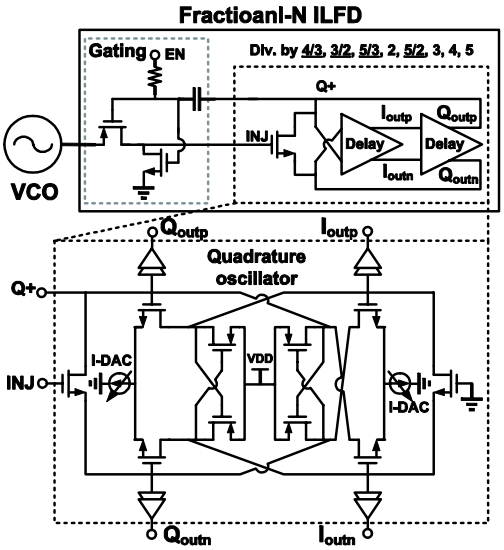

Fig.3. Schematic of fractional-N ILFD.

TABLE I COMPARISON BETWEEN THE-STATE-OF-THE-ART SDR SYNTHESIZERS

	[1]	[2]	[3]	[4]	This work
Frequency [GHz]	0.125-32	0.6-4.6, 5-7, 10-14, 20-28	0.05-10, 19-22,38-44	0.1-5	0.01-6.6
In-band phase noise @ 10 kHz offset [dBc/Hz]	-91.6	-109.9	-91 to -98	-94	-95.1
Out-band phase noise @ 3MHz offset [dBc/Hz]	-137.2	-136.5	-139.6	-136	-135.3
Area [mm^2]	4.4[1]	4.8[1]	3	0.41	0.38
Power [mW]	1283	680	33-83	33	16-26
Numbers of LC resonator	4	2	2	2	1

1. Area including pads.
2. Normalized to 3 MHz from values reported at other frequency offsets.
3. Normalized to 1.7 GHz from values reported at other carrier frequency.