A Comparison between Common-source and Cascode Topologies for 60GHz Amplifier Design in 65nm CMOS

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1. Introduction

Although RF front-end amplifiers are implemented at low noise amplifiers and power amplifiers with different specifications due to the different functions they perform, sufficient gain and low power consumption are the general requirements. For the design consideration, the active device structure and models should be optimized at 60 GHz.

Both common-source (CS) and cascode topologies are utilized in millimeter-wave (MMW) circuit design. CS topology, which has reasonable power gain and small noise figure, is widely used in MMW amplifier designs. The good isolation between input and output of cascode topology is also attractive in mm-wave amplifier design.

In this paper, the comparison of CS topology, cascode topology, and a gain-boost cascode topology which uses a transmission line (TL) at the gate of the common-gate transistor are carried out considering the gain, the isolation and the stability factor in 65nm CMOS process. The peak maximum gain per current densities in the cascode and CS topologies are verified by measurement results. A one-stage amplifier using cascode topology is implemented.

2. Comparison between the CS and cascode topologies

At lower frequency, the cascode topology has the advantage of higher gain performance than the CS topology. As the operation frequency increases, cascode transistors have a larger parasitic capacitance which reduces the inter-stage impedance and gain. A gain-boost technique with using the inductance L_{TL} at the common-gate transistor of the cascode topology is reported in [1], which can increase the power gain of this topology. In order to compare the performances of the CS topology, cascode topology, and the gain-boost cascode topology in MMW ranges, three topologies as shown in Fig. 1 are fabricated using 65-nm CMOS technology. The transistor M1 in the three topologies is the same one, which uses the asymmetric-layout technique in [2]. The transistor M2 uses the common layout provided by foundry. In Fig. 1(c), 80 μm guide micro-strip transmission line (MSTL) [3] is utilized instead of the inductance. The self-bias technique is used in the cascode topologies by added a large resistance and a capacitor as shown in Fig. 1(b) and Fig. 1(c).

The measurement results including the maximum gain, the isolation and the stability factor are shown in Fig. 2. The bias voltage V_{g1} is 0.6 V, both the V_{g2} and the supply voltage V_{dd} are the 1.2 V. Fig. 2 (a) shows that the maximum gain of the cascode topology decreased faster than the CS topology as the frequency increases. The same maximum gain can be obtained around 60 GHz. The gain-boost cascode topology achieves a 3-dB higher maximum gain than the CS and the common cascode topologies. Both the cascode topology and the gain-boost cascode topology have about -30dB reverse isolation at 60GHz while the reverse isolation of CS topology is only -13dB at 60GHz as shown in Fig. 2(b). The stability factor is shown in Fig. 2(c). Common cascode topology and the gain-boost cascode topology have much better stability factor than the CS topology at 60GHz. However, the stability factor of gain-boost cascode topology becomes worse when the frequency is higher than 80GHz.

The supply voltage is limited at 1.2V in the 65nm CMOS process. When biased at current densities between 0.15mA/μm and 0.4mA/μm, the gain becomes almost insensitive to I_d and V_{GS} variation [4]. The constant current density biasing technology can be used to control the current density for a higher maximum and reasonable power consumption. Fig. 3(a) shows the simulated maximum gains which change as the different biases in the CS topology, the common cascode topology and the gain-boost cascode topology. When the bias is between 0.6V and 0.8V, the maximum gain of the both cascode topologies is around the peak maximum gain. However when the bias is larger than 0.6V, the maximum gain of the CS topology is almost flat. The measurement results of the maximum gains which biased from 0.6V to at 0.8V in the cascode topologies and 0.6V to 0.9V in the CS topology are shown in Fig. 3(b). The peak maximum gain bias voltage of the cascode topologies occurred at 0.7V, while the CS topology is 0.8V. The measured power consumption and calculated current density are shown in Fig. 3(c). As the bias increases, the power consumption and the current density increase, while the maximum gain does not increase any more when up to the peak point. The current density which is less than the peak maximum gain per current density can be chosen for a reasonable maximum gain and power consumption.

3. One-stage amplifiers using gain-boost cascode topology

The stability factor of the gain-boost cascode topology becomes worse while the frequency is higher than 80GHz. In order to verify this issue, a one-stage amplifier using the gain-boost cascode topology is implemented. The input and

output impedance matching are realized by the MSTL. The measurement results of the one-stage amplifier with 0.15 mA/μm current density are shown in Fig. 4. The power gain is about 7dB and the amplifier is unconditional stable up to 110GHz.

4. Conclusion

The gain-boost cascode topology has higher maximum gain and better reverse isolation than the CS topology at 60GHz. The peak maximum gain per current densities in the cascode and CS topologies are verified by the measurement results. The one-stage amplifier using the gain-boost cascode topology obtains a 7dB power gain and unconditional stability with 0.15 mA/μm current density.

Acknowledgements

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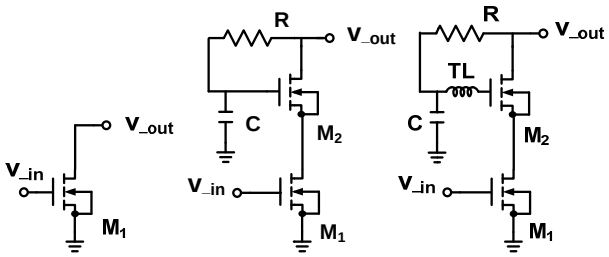
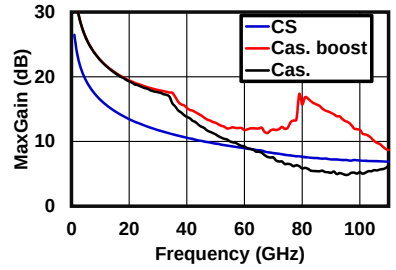
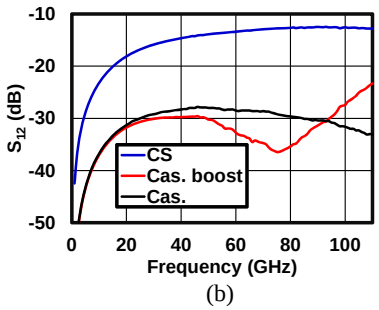


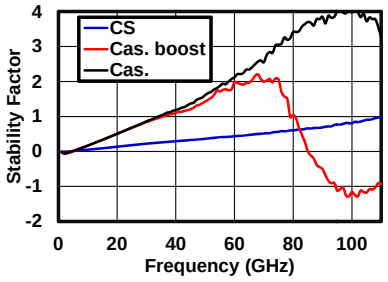
Fig. 1 (a) CS topology, (b) cascode topology, (c) Gain-boost cascode topology.



(a)

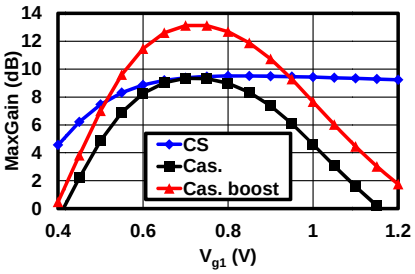


(b)

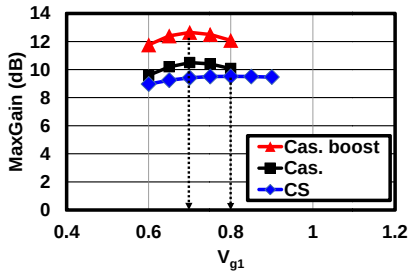


(c)

Fig. 2 The measured maximum gain, S_{12} and stability factor of the CS, cascode, and gain-boost cascode topologies, (a) maximum gain, (b) S_{12}, (c) stability factor.



(a)



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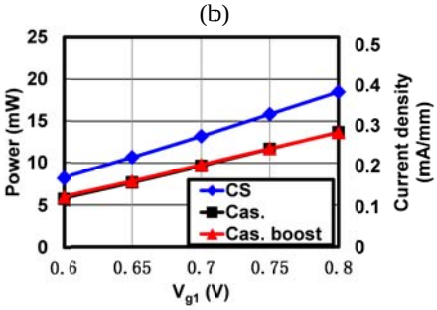

(c)

Fig. 3 (a) Simulated maximum gain with different bias voltages, (b) measured maximum gain with different bias voltages, (c) measured power consumption and current density.

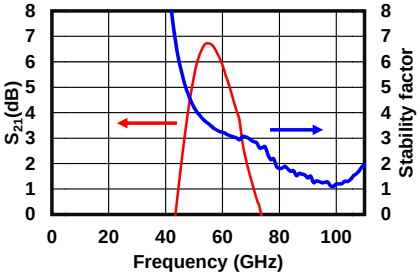

Fig. 4 Measure power gain and stability factor of one-stage amplifier.