A 60GHz PVT-tolerant Injection-locked Frequency Synthesizer with a Background Frequency Calibration Technique

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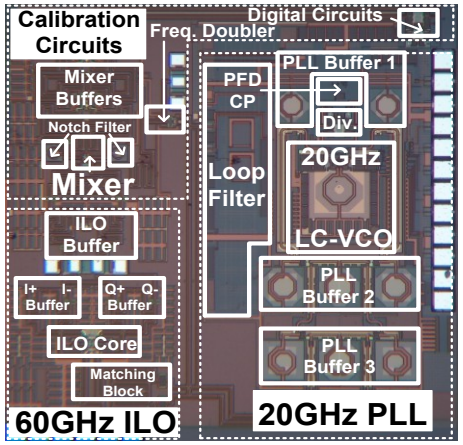
A 58.1-to-65.0 GHz frequency synthesizer using sub-harmonic injection-locking technique with background frequency calibration technique for Time Division Duplex (TDD) transceivers [1]-[2] is presented. The synthesizer is capable of supporting all 60GHz channels which are specified by IEEE 802.15.3c, wirelessHD, IEEE 802.11ad, WiGig, and ECMA-387 for short-range high-speed wireless communications. A frequency calibration scheme is proposed to monitor a frequency shift of quadrature injection locked oscillators which is caused by environmental variations. The proposed synthesizer is implemented in a 12-metal 65nm CMOS process, the synthesizer achieves a phase noise of -96 dBc/Hz @1MHz offset from a carrier frequency of 61.56 GHz.



[1] W. Deng, T. Siriburanon, A. Musa, K. Okada, and A. Matsuzawa, "A 58.1-to-65.0GHz Frequency Synthesizer with Background Calibration for Millimeter-wave TDD Transceivers, " *IEEE European Solid-State Circuits Conference* (*ESSCIRC),* pp. 201-204, Sep. 2012.

[2] T. Siriburanon, W. Deng, A. Musa, K. Okada, and A. Matsuzawa, "A Sub-harmonic Injection-locked Frequency Synthesizer with Frequency Calibration Scheme for Use in 60GHz TDD Transceivers," *IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC)*, Yokohama, Japan, Jan. 2013 (Accepted).