An 84 mW 0.36 mm^2 Analog Baseband Circuits for 60 GHz Wireless Transceiver in 40 nm CMOS

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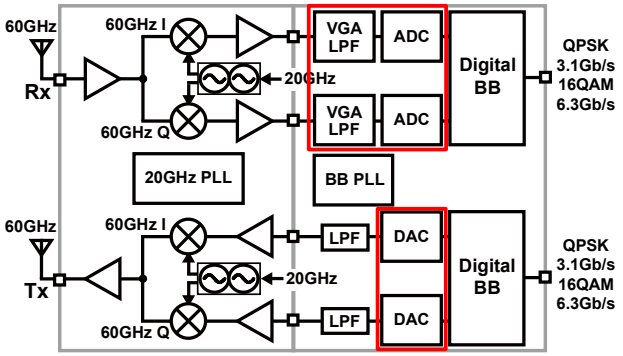
1. Introduction

Developing an analog baseband circuitry for 60 GHz wireless transceiver in 40 nm digital CMOS.



Target Specifications

Transceiver

Modulation	QPSK, 16QAM
Data rate	3.1 Gb/s (QPSK)
	6.3 Gb/s (16QAM)
Distance	> 1 m (QPSK)

ADC

Resolution	5 bit
Sampling rate	2304 MS/s
DNL, INL	< 0.5 LSB
SNDR	> 25 dB

VGA

Gain range	0 - 40 dB
-3dB Bandwidth	~1000 MHz
Input referred noise	< 4 nV/√Hz
SFDR@100MHz	< 40 dBc

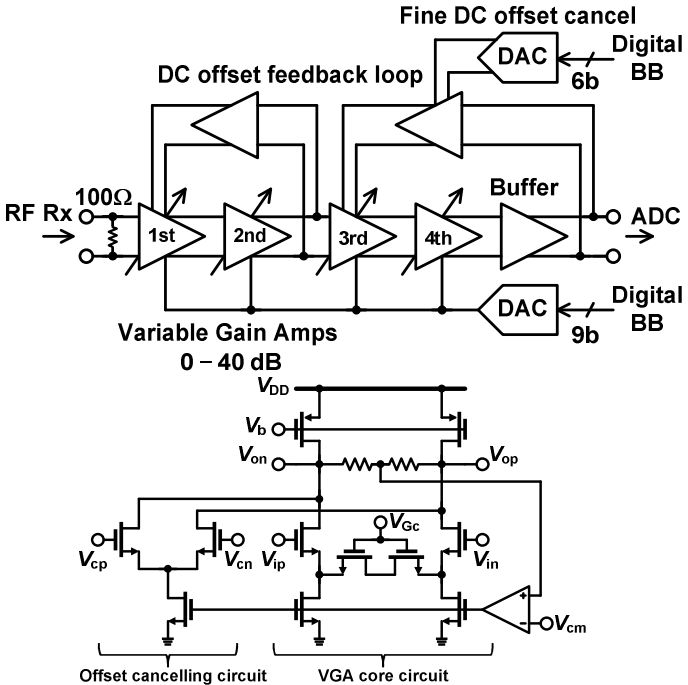
DAC

Resolution	6 bit
Sampling rate	3456 MS/s
DNL, INL	< 0.5 LSB
SFDR	> 39 dBc

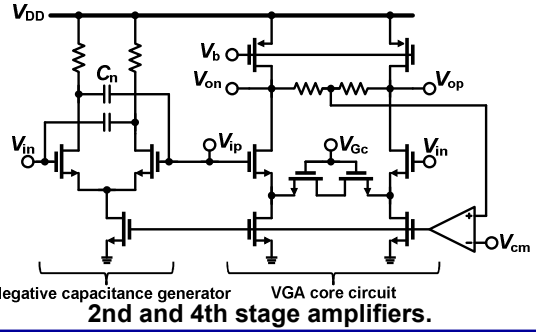
Design Items
VGA : Variable Gain Amplifier
ADC : Analog to Digital Converter
DAC : Digital to Analog Converter

- **LPF function is implemented in VGA.**
- **S/P(1/8) and P/S(1/16) circuits are implemented in ADC and DAC respectively.**

2. Variable Gain Amplifier

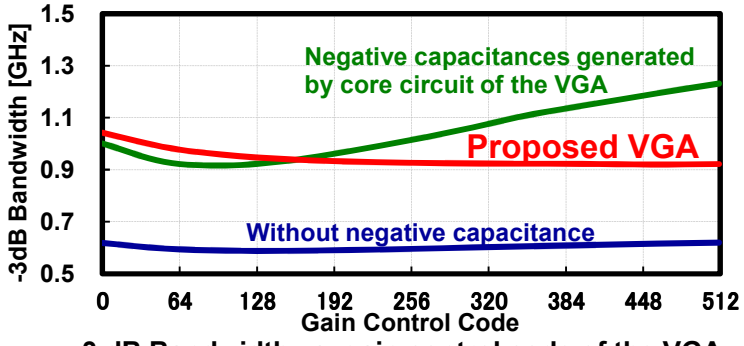


1st and 3rd stage amplifiers.

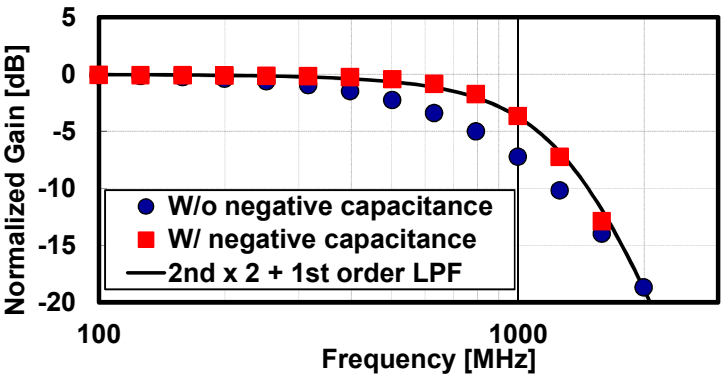


2nd and 4th stage amplifiers.

- **0 - 40dB gain range.**
  - **Source degeneration resistors are controlled by 9bit DAC.**
- **1GHz Bandwidth with LPF function.**
- **Negative capacitance used for increasing BW.**
  - **Fixed negative capacitance used for BW flatness.**



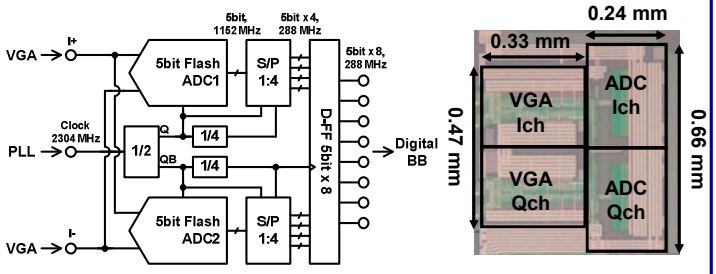
-3 dB Bandwidth vs. gain control code of the VGA

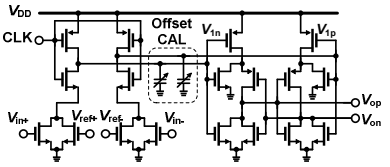


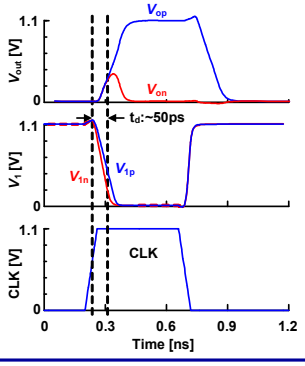
Frequency characteristic of the VGA at 20dB Gain

3. Analog to Digital Converter

5bit, 2304MS/s, 12mW Flash ADC



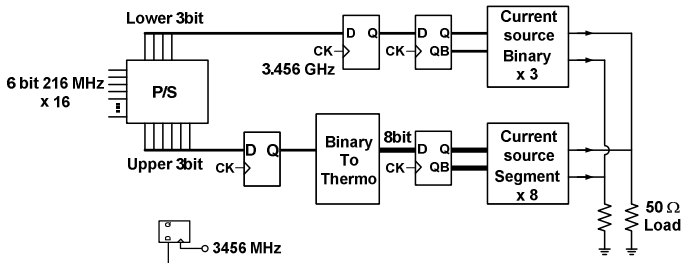


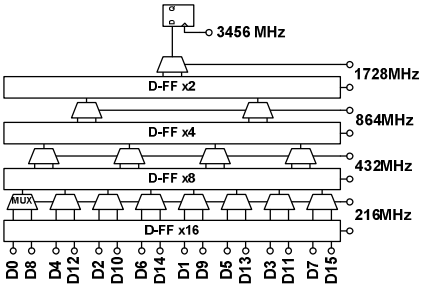


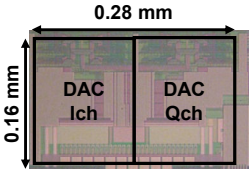
- 2x interleaved flash ADC.
- Integrated self-calibration of comparator offset.
- Dynamic amplifiers with latch circuit is used as a S/H.
  - Relax the VGA drivability.

4. Digital to Analog Converter

6bit, 3456MS/s, 21mW Current steering DAC



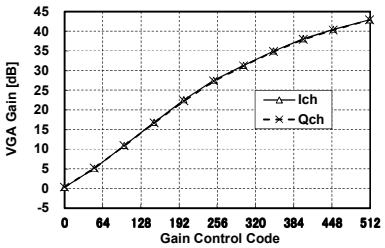




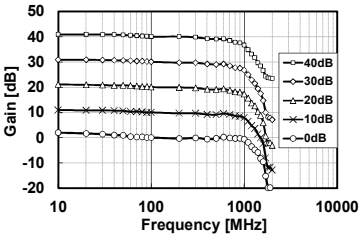
- Driving a 50 Ω resistive load => 11mW for driving load
- 3bit Binary +3bit Segment structure.
  - Small glitch energy and area
- Integrated P/S(16:1,216MHz:3456MHz) circuit.

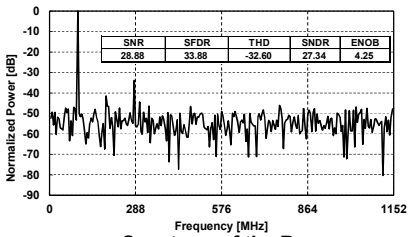
5. Measurement Results

Analog baseband Measurement results

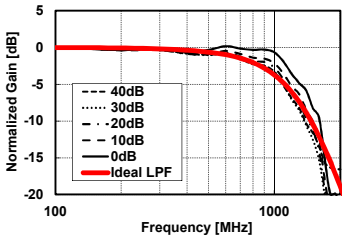


VGA gain vs. Gain control code.

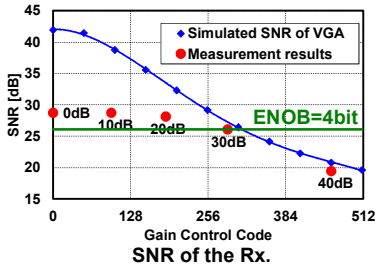




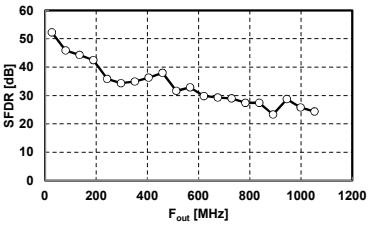
Spectrum of the Rx.



Frequency characteristic of the Rx.



SNR of the Rx.



SFDR of the DAC.

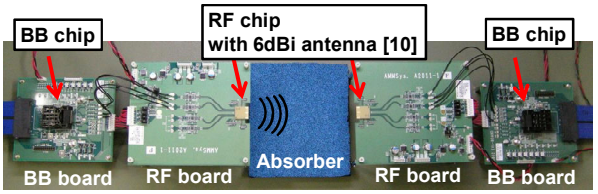
VGA performance summary

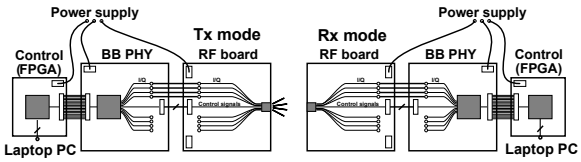
Work	Tech.	LPF Order	f-3dB	Gain	Linearity	Noise	Supply	Power
This work	40nm	2thx2+1th	920MHz@40dB 1150MHz@0dB	0dB ~40dB	IIP3=8.3dBm @0dB gain	IRN= 3.8nV/√Hz	1.1V	9mW
[1]S. D'Amico et al. -RFIC 2011	90nm	6th	915MHz@0dB	0.1dB ~19.6dB	IIP3=5.6dBm @0dB gain	IRN= -145 dBm/Hz	1V	9.5mW@0dB 10.8mW@20dB
[2]C. Wu et al.- ISSCC 2004	0.18μm	N/A	2GHz	-16dB ~34dB	N/A	N/A	1.8V	40mW
[3]H. Lee et al.- IEEE TMTT	0.18μm	N/A	900MHz	-39dB ~55dB	1dBcp= -10.8~-59.1dBm	NF= 6.8dB~67dB	1.8V	20.52mW

ADC performance summary

Work	Type	Integrated mmW SoC	Cal.	Fs [GS/s]	SNDR [dB]	Power [mW]	FoM [fJ/-c.s.]	Process [nm]	Area [mm²]
This work	Flash	Yes	Int.	2.3	27.3	12	274	40	0.06
[4]K.Deguchi, et al., VLSI 2007	Flash	No	-	3.5	31.2	98	946	90	0.149
[5]E. Alpman, et al., ISSCC 2009	SAR	No	Int.	2.5	34.0	50	489	45	1
[6]Y. Nakajima, et al., VLSI 2007	Folding	No	Int.	2.7	33.6	50	474	90	0.36
[7]B. Verbruggen, et al., ISSCC 2010	Pipeline	No	Ext.	2.2	31.1	2.6	40	40	0.03
[8]T. Ito, et al., A-SSCC 2010	Flash	No	Int.	3.0	27.6	36	600	65	0.25
[9]T. Mitomo, et al., ISSCC 2012		Yes		2.88		68.5	1200	65	-

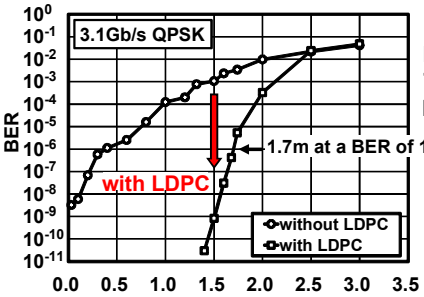
Transceiver Measurement results





[10] R. Suga, *et al.*, *EuMC* 2011

Measurement setup

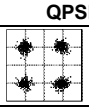
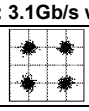
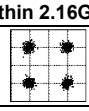
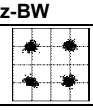
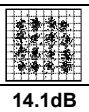
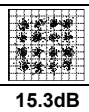
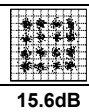
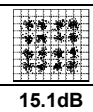


P_{DC}(16QAM/QPSK)
Tx:515mW/368mW
Rx:621mW/525mW

Energy efficiency
180pJ/bit

Communication distance

RF+BB Constellation

	ch1	ch2	ch3	ch4
	QPSK: 3.1Gb/s within 2.16GHz-BW			
Constellation				
SNR	14.8dB	14.8dB	15.9dB	15.8dB
BER	<10^{-11}	<10^{-11}	<10^{-11}	<10^{-11}
	16QAM: 6.3Gb/s within 2.16GHz-BW			
Constellation				
SNR	14.1dB	15.3dB	15.6dB	15.1dB
BER	5.0×10^{-3}	8.4×10^{-4}	6.7×10^{-4}	8.3×10^{-4}