# An 84 mW 0.36 mm$^2$ Analog Baseband Circuits for 60 GHz Wireless Transceiver in 40 nm CMOS

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***Abstract* — This paper presents low-power, small area analog baseband (ABB) circuits for 60 GHz wireless transceiver in 40 nm CMOS. The ABB circuits consist of 0-to-40 dB VGAs and 5-bit 2304 MS/s flash ADCs for the receiver, and 6-bit 3456 MS/s DACs for the transmitter. The VGAs also work as 2-2-1 order low-pass filters by using negative capacitance generator. The receiver demonstrates SNDR of 27.3 dB at 2304 MS/s with 16 dB VGA gain. The DAC demonstrates SFDR of 40 dB at 3456 MS/s up to 200 MHz. VGAs, ADCs and DACs consume 18 mW, 24 mW and 42 mW from a 1.1 V supply, respectively. The entire ABB circuits occupy an area of 0.36 mm$^2$.**

## I. Introduction

The commercialization of ultra-high speed communication systems for short distance ranges often require using 2.16GHz x 4 channels because these channels are license-free based on IEEE 802.15.3c. Several RF transceivers with direct conversion method have been reported recently [1]-[2]. In this paper, the analog baseband circuit to connect between the RF transceiver and the digital baseband circuit is introduced. The target specification of this analog baseband is 3.1 Gbps communication speed for a distance of more than 1 m using QPSK modulation [3]. The receiver circuit consists of 0-40dB variable gain amplifiers (VGAs) with a 1 GHz cut-off frequency LPF function and 5-bit 2304 MS/s Flash ADCs. The cut-off frequency of the LPF function in the VGA has to remain constant even when the gain of the VGA changes. To improve the bandwidth of conventional amplifiers, a negative capacitance generator (capacitance neutralization technique) is usually used [4]-[5]. However, the capacitance of the conventional negative capacitance generator is changed by the gain of the amplifier resulting in a change in the amplifier's frequency characteristic. Due to this reason, the conventional negative capacitance generator is not suitable for VGAs as a constant frequency characteristic is the target. To solve this problem, a new VGA using negative capacitance generator, which is not affected by the change of the gain of the VGA, is introduced. The flash ADC is implemented using dynamic comparators with capacitive offset cancelation to achieve low power consumption by eliminating pre-amplifiers. Instead of conventional S/H circuit, which consists of switches and capacitors, the dynamic amplifier with latch circuit is used as a S/H to relax the demands on the VGA buffer. The transmitter is implemented by 6-bit 3456 MS/s current DAC with 3-bit thermometer and 3-bit binary output. Each circuit structure and measurement results are discussed in following sections.

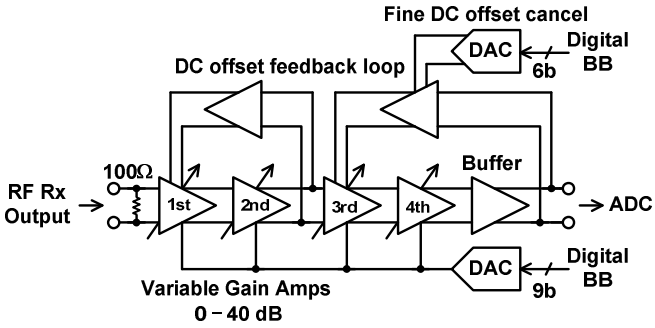
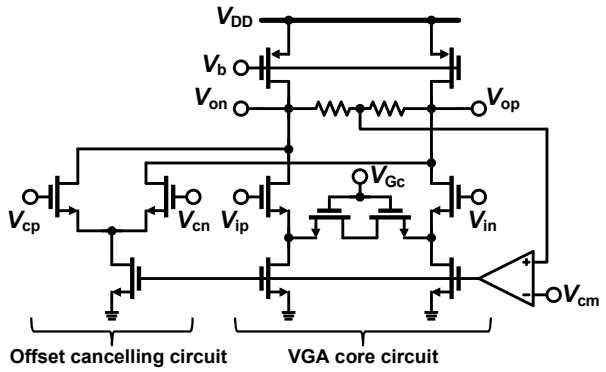


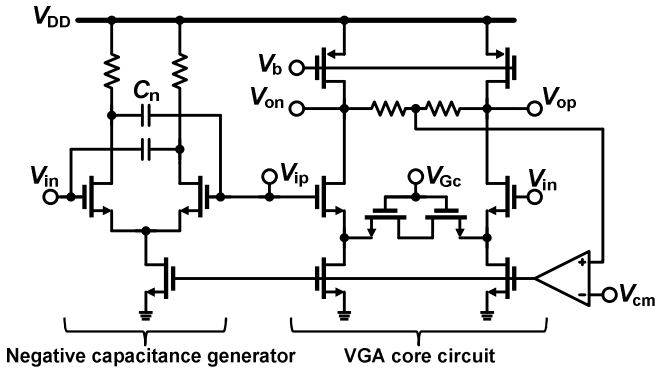

Fig. 1. Block diagram of the proposed variable gain amplifier.

## II. Variable Gain Amplifier

Figure 1 shows the structure of the VGA. Several methods have been reported to realize variable gain [4]-[6]. Those methods can be classified into two groups: changing the output resistance and changing the transconductance of the amplifier. In the proposed VGA, changing transconductance is implemented to incorporate filter function, which should not be affected by the changes in the gain of the VGA. There are two popular methods to control transconductance of an amplifier, one is controlling the source degeneration resistance, and another is controlling the gate voltage of the cascode transistor. Of the two methods, introducing cascode structure is not suitable for recent low supply voltage system such as 1.1 V due to the degraded output swing range. Therefore, the proposed VGA controls the source degeneration resistor as shown in figure 2 (a) and (b). By controlling $V_{GC}$ voltage using a DAC, the gain of the VGA can be changed.




(a) The proposed variable gain amplifier with the offset cancelling circuit for 1st and 3rd stage amplifiers.




(b) The proposed variable gain amplifier with the negative capacitance generator circuit for 2nd and 4th stage amplifiers.

Fig. 2. Schematic of the proposed variable gain amplifier.

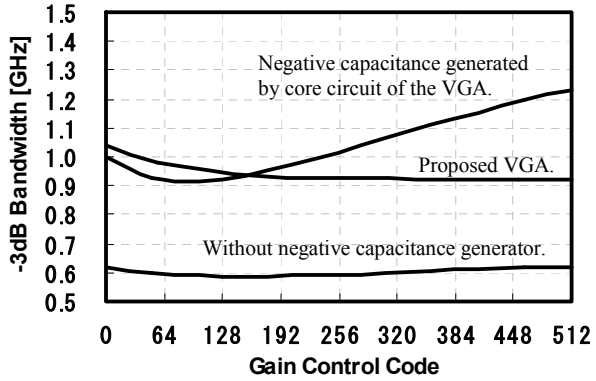



Fig. 3. -3 dB Bandwidth vs. gain control code of the VGA.

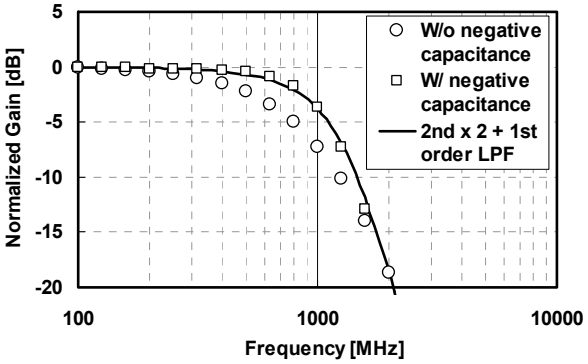



Fig. 4. Frequency characteristic of the VGA at 20dB gain.

Figure 2 (a) shows the first stage and the third stage amplifiers for realizing offset cancelation. Also, capacitance neutralization technique is incorporated into the VGA to extend bandwidth. The negative capacitance can be realized by positive feedback of capacitor to the input transistor in the VGA core circuit. A problem with this method is any changes in the gain of the VGA causes the negative capacitance to change, and also the bandwidth of the VGA. To solve this problem, the proposed VGA introduces a fixed-gain negative capacitance generator to the second stage and the fourth stage as shown in figure 2 (b).

Figure 3 shows the -3 dB bandwidth characteristic against gain variation of the VGA. The proposed VGA extends its bandwidth by introducing negative capacitance. Also, it can be recognized that the bandwidth remains almost constant in spite of gain variation as illustrated in figure 3. Figure 4 shows the frequency characteristic when the gain is set to 20 dB. The proposed VGA is implemented by two stages of second-order LPF and one stage of first-order LPF. Due to these LPFs, the proposed VGA shows a more drastic cut-off frequency slope than without negative capacitance technique.

## III. Analog to Digital Converter

Figure 5 shows the structure of the 5-bit 2304 MS/s ADC. This ADC consists of two interleaved flash ADCs. The output results of the ADC are transferred to digital baseband (DBB) after slowing down its data rate by serial-to-parallel (S/P) circuit as the operating frequency of DBB is only 288 MHz.

Figure 6 shows a double-tail latched comparator with capacitive offset cancellation for the flash ADCs [7]. The offset voltage of the comparator can be reduced by adjusting the capacitance at the output nodes of the first stage of the double-tail latched comparator. The maximum differential input swing of the ADC is 480 $mV_{PP}$; therefore, 1 LSB becomes 15 mV. To suppress ENOB degradation of the ADC to less than 0.2-bit, the comparator has to be designed to have an input-referred offset of less than 1/8 LSB at sigma, which is around 2 mV(σ). The offset voltage of the comparator is suppressed from 10 mV(σ) to 1.5 mV(σ) by capacitive offset cancelation. This means the comparator doesn't require other conventional offset cancelation technique such as introducing a pre-amplifier, thus, low power consumption

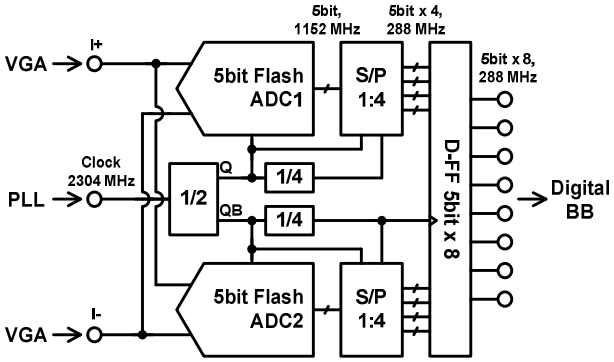



Fig. 5. The proposed 5-bit 2304MS/s ADC structure.

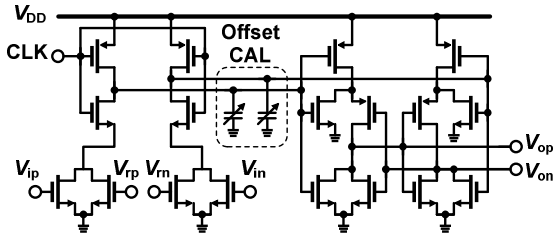



Fig. 6. Schematic of the dynamic comparator for ADCs.

also can be achieved. Another characteristic of the proposed ADC is the lack of a passive type S/H circuit, which basically consists of switches and capacitors. The passive type S/H circuit severely increases the requirement of the VGA output buffer. Furthermore, it increases power consumption. Alternatively, the sampling of the ADC is carried out by the dynamic comparators directly.

## IV. Digital to Analog Converter

Figure 7 shows the structure of 6-bit 3456 MS/s DAC. The digital data from the DBB are transferred at 216 MHz operating frequency with 16 parallel paths. To receive these data, the operating frequency of the DAC is increased up to 3456 MS/s by a parallel-to-serial (P/S) circuit. The proposed DAC consists of 3-bit thermometer and 3-bit binary structure to drive a 50 Ω resistive load. By introducing the combination of thermometer and binary structure, glitches are suppressed and a small core area is achieved.

## V. Measurement Results

The chip micrograph of the proposed analog baseband circuits, which are fabricated in 40 nm CMOS process, is shown in figure 8. The size of the VGA and the ADC is 0.16 $mm^2$ and the DAC is 0.04 $mm^2$. Each ADC and DAC includes a S/P and a P/S circuit, respectively. These circuits are implemented in a SoC; therefore, it is

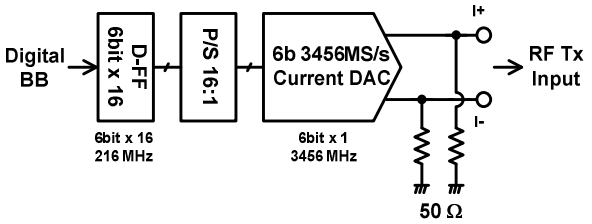



Fig. 7. The proposed 6-bit 3456 MS/s DAC structure.

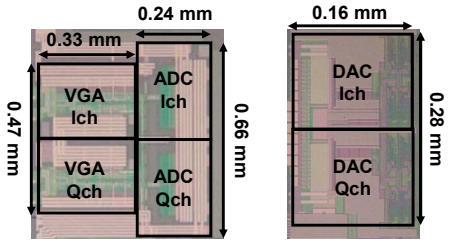



Fig. 8. Chip photo.

impossible to monitor the output of the VGA directly. Due to this reason, the ADC outputs are employed to measure the performance of the receiver circuit.

Figure 9 shows the VGA gain against gain set-up code. 100 MHz sine wave is utilized to measure the performance of the VGA. The measurement results show the gain of the VGA can be configurable from 0 dB to 42 dB. The maximum gain mismatch between Ich and Qch is only 0.3 dB; these two channels show very good matching.

Figure 10 shows the frequency characteristic of the receiver circuit. The measured gain of the VGA is plotted from 0 dB to 40 dB with 10 dB steps, which is standardized by the gain of 100 MHz input. The cut-off frequency of 1 GHz is nearly constant against the gain variation. The variation of -3 dB bandwidth is suppressed to less than +/-10 %. The gain curve also shows good flatness from 10 dB to 40 dB with small variation within +/-1dB from 3 MHz to 600 MHz. The DNL and INL are calculated by histogram method when 100 MHz sine wave is utilized as input signal and the gain of the VGA is set to 16 dB. The DNL and INL errors are less than +0.5/-0.5 LSB and +0.5/-0.63 LSB, respectively. The reason of INL degradation is likely due to the non-linearity of the VGA. Figure 11 shows the spectrum analysis with 100 MHz input signal and 16 dB VGA gain. The peak SNDR of 27.3 dB and ENOB of 4.25-bit are achieved. The VGAs and the ADCs consume 18 mW and 24 mW from a 1.1 V supply voltage, respectively. The power consumption of the ADCs includes the S/P circuits. FoM of 274 fJ/conv.step is obtained from the single ADC.

The DNL and INL of the DAC are +0.1/-0.13 LSB and +0.13/-0.13 LSB, respectively, which demonstrates very good linearity characteristic. Figure 12 shows the

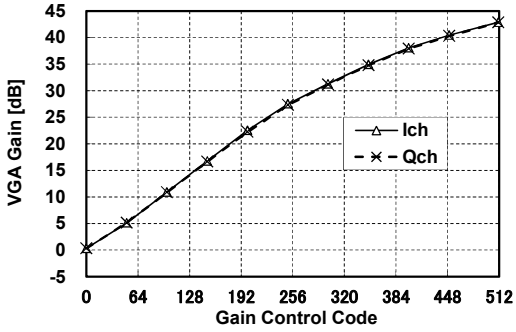


Fig. 9. The measured VGA gain vs. gain control code.

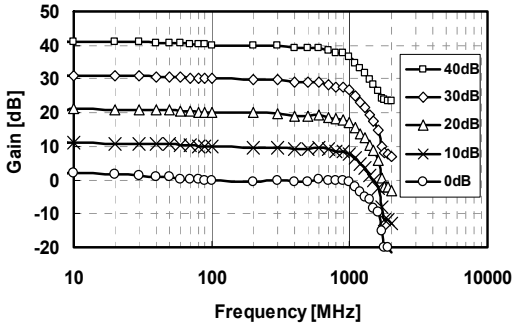


Fig. 10. The measured frequency characteristic of the receiver circuit.

measurement results of SFDR against output frequency: 52 dB is obtained at 27 MHz output frequency. The SFDR maintains above 40 dB until the output frequency reaches 200 MHz. The DACs consume 22 mW with 50 Ω loads and 20 mW for P/S circuits from a 1.1 V supply voltage.

## VI. Conclusion

This paper presents low-power analog baseband circuits for 60 GHz wireless transceivers in 40 nm CMOS. The VGAs also work as 2-2-1 order low-pass filters by using the negative capacitance generator. The receiver demonstrates SNDR of 27.3 dB at 2304 MS/s with 16 dB VGA gain. The DAC demonstrates SFDR of 40 dB at 3456 MS/s until 200 MHz. The ADCs, VGAs and DACs consume 24 mW, 18 mW and 42 mW from a 1.1 V supply, respectively. The entire analog baseband circuits occupy only 0.36 $mm^2$.

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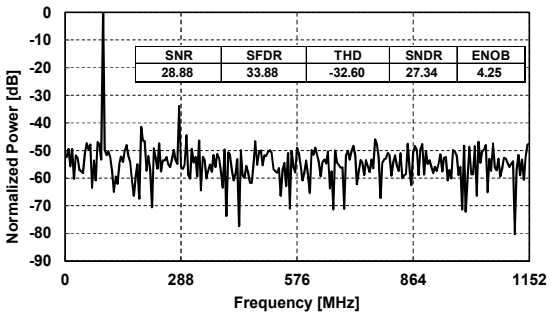

Fig. 11. Spectrum of the receiver measured with a 100 MHz.

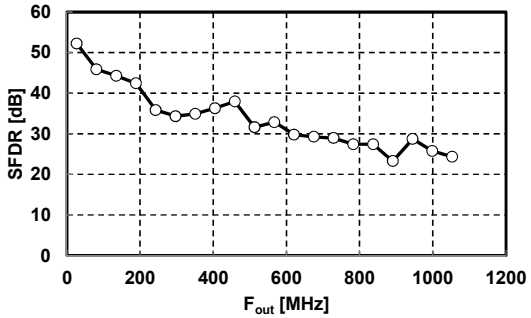

Fig.12. Measured SFDR vs. output frequency of the DAC.

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