Proposing

An Interpolated Pipeline ADC

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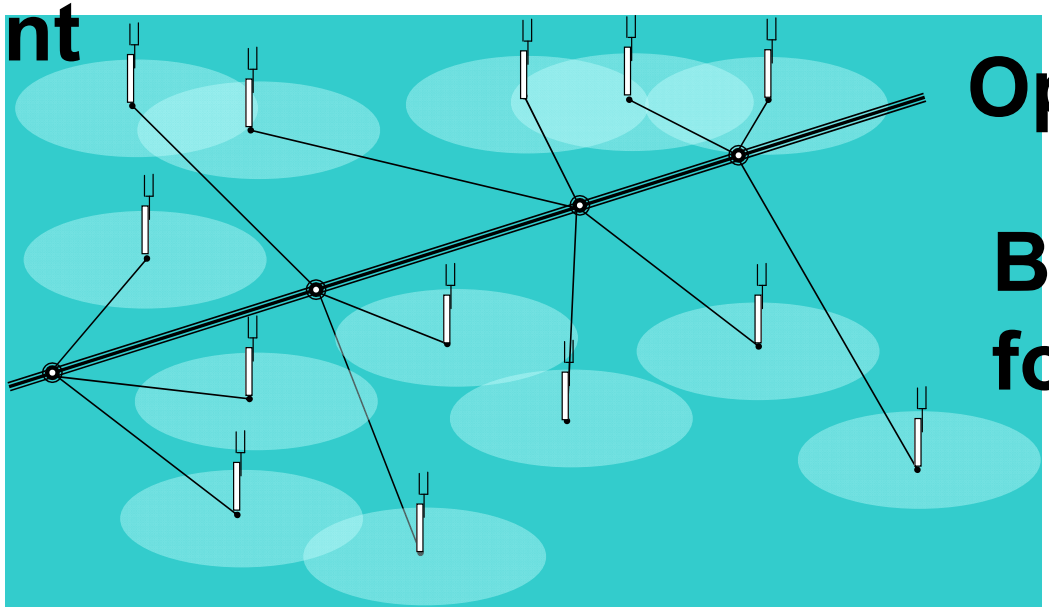
Background

38GHz long range mm-wave system

Role of long range mm-wave

Current

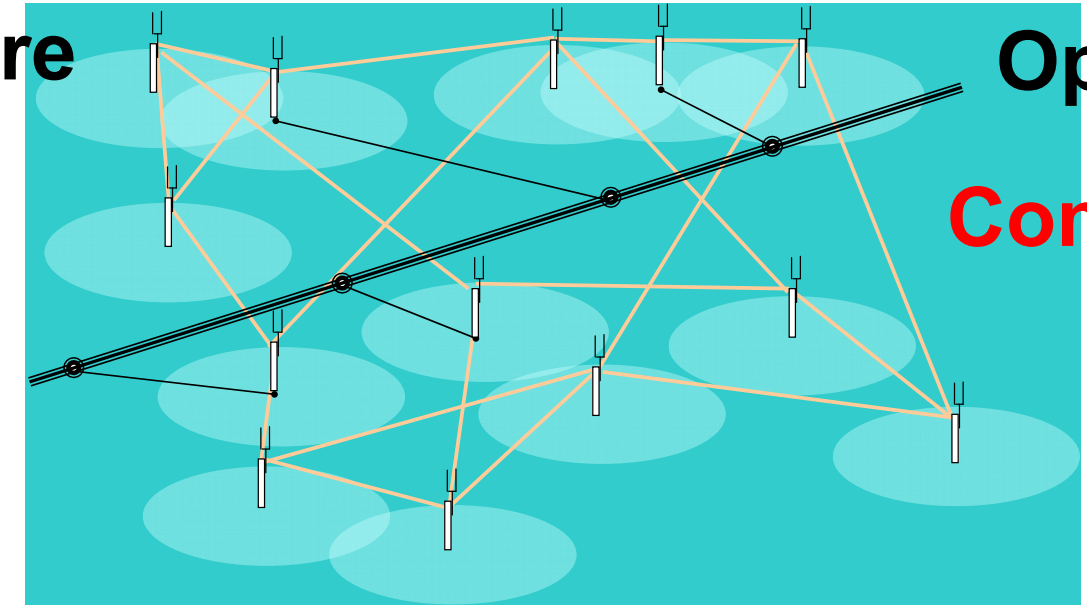


Optical fiber

Base stations
for WiFi and WiMAX

Not flexible

Future



Optical fiber

Connect with mm-wave

Very flexible

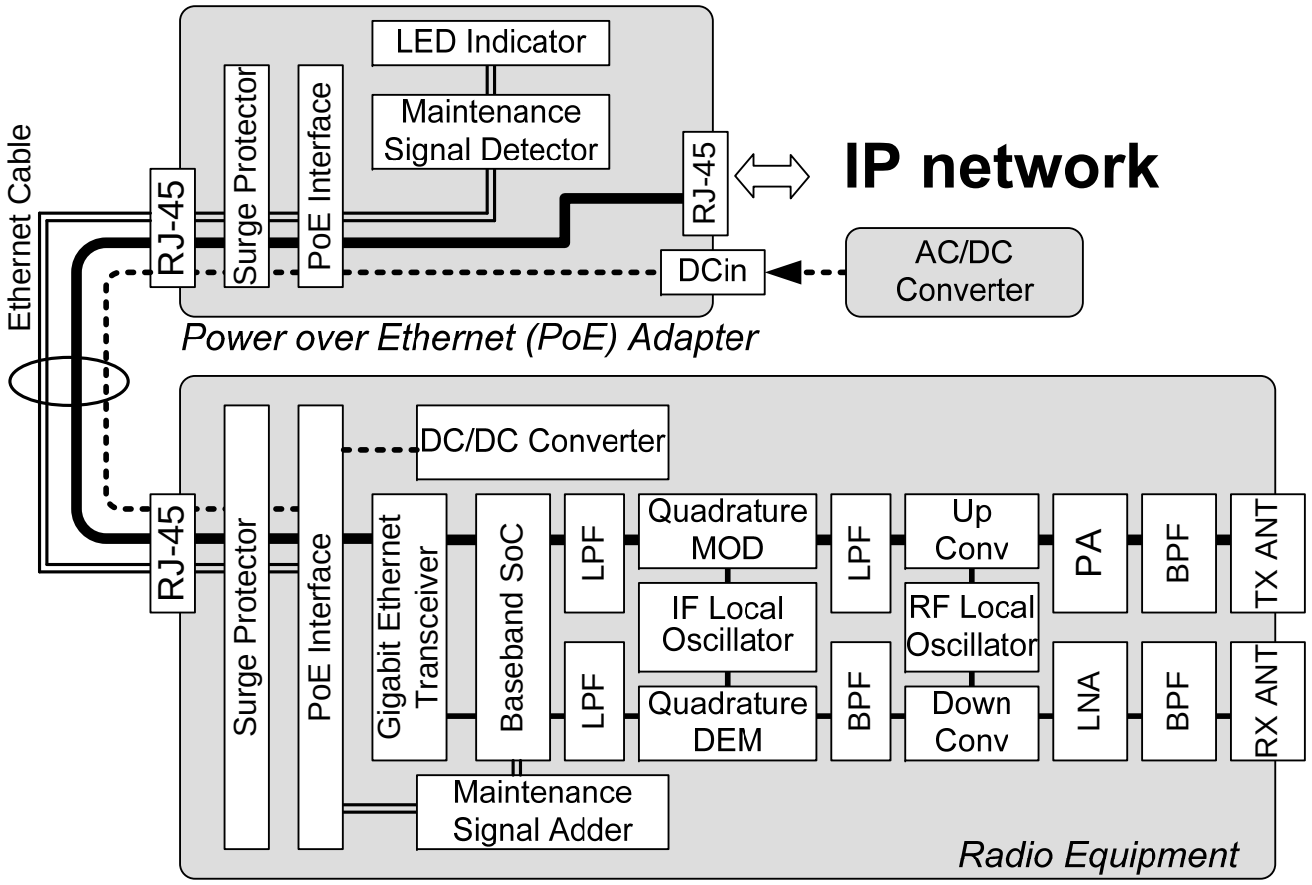
38GHz long range mm-wave system

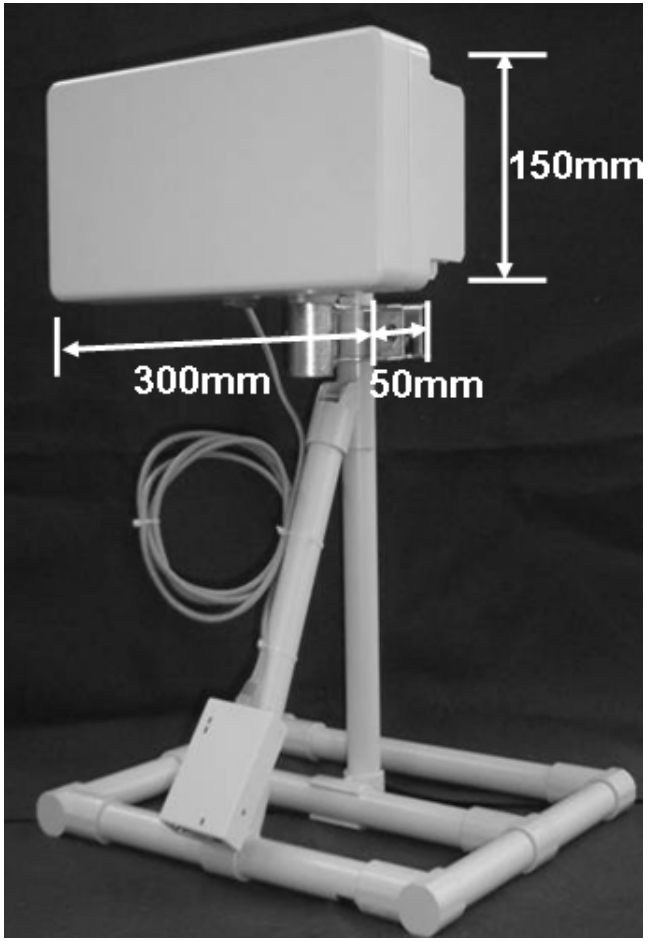
realized 1Gbps long range mm-wave systems

Current system: 80Mbps!!

System configuration

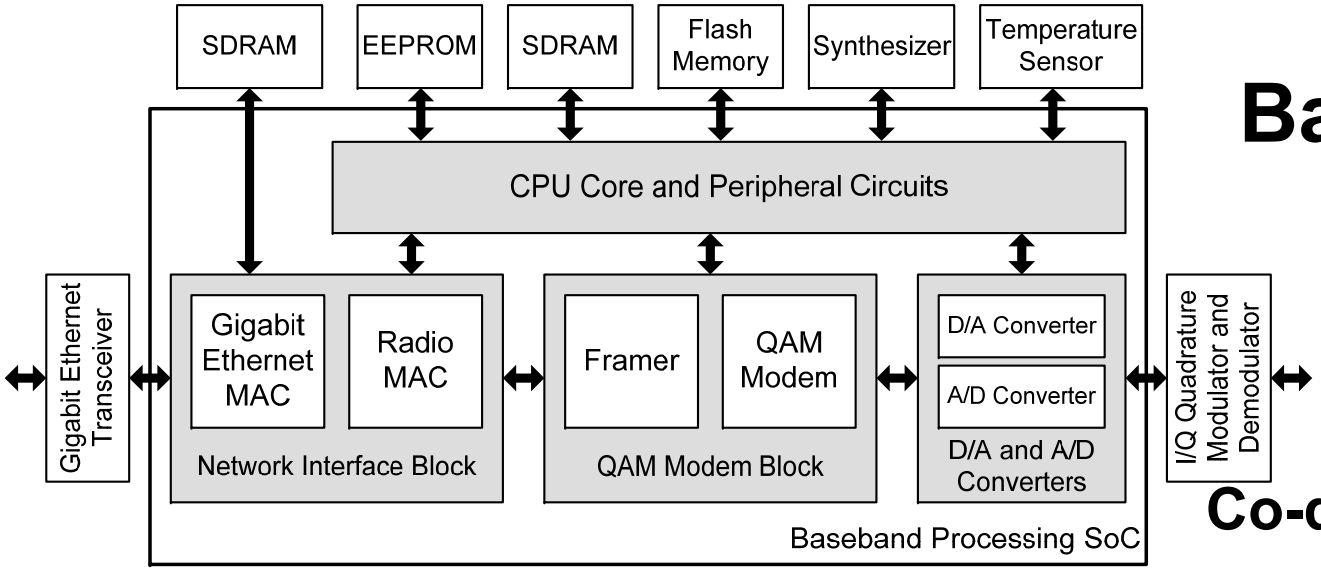
Compatible with Gbit Ethernet
Hole system is integrated with planar antenna





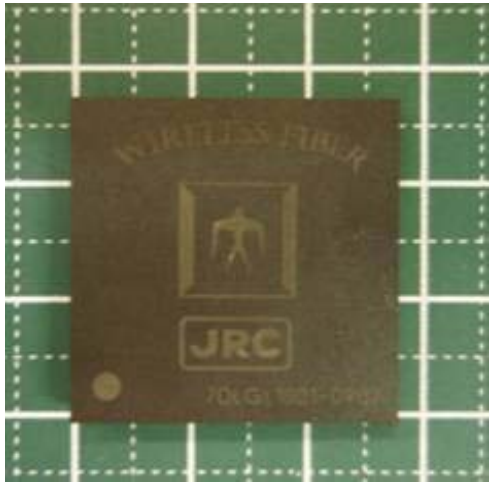
Mixed signal BB SoC

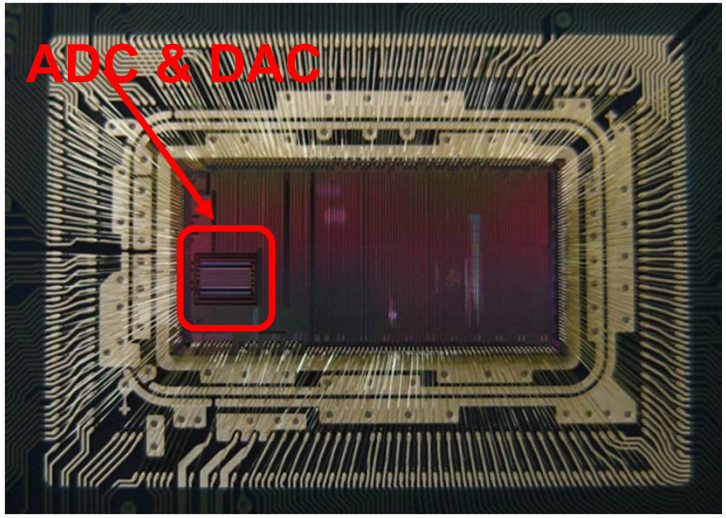
A mixed signal SoC has been developed to realize 64QAM (1Gbps) with BW of 260MHz.



Base band SoC

Co-developed with JRC





90nm CMOS
40M Transistors

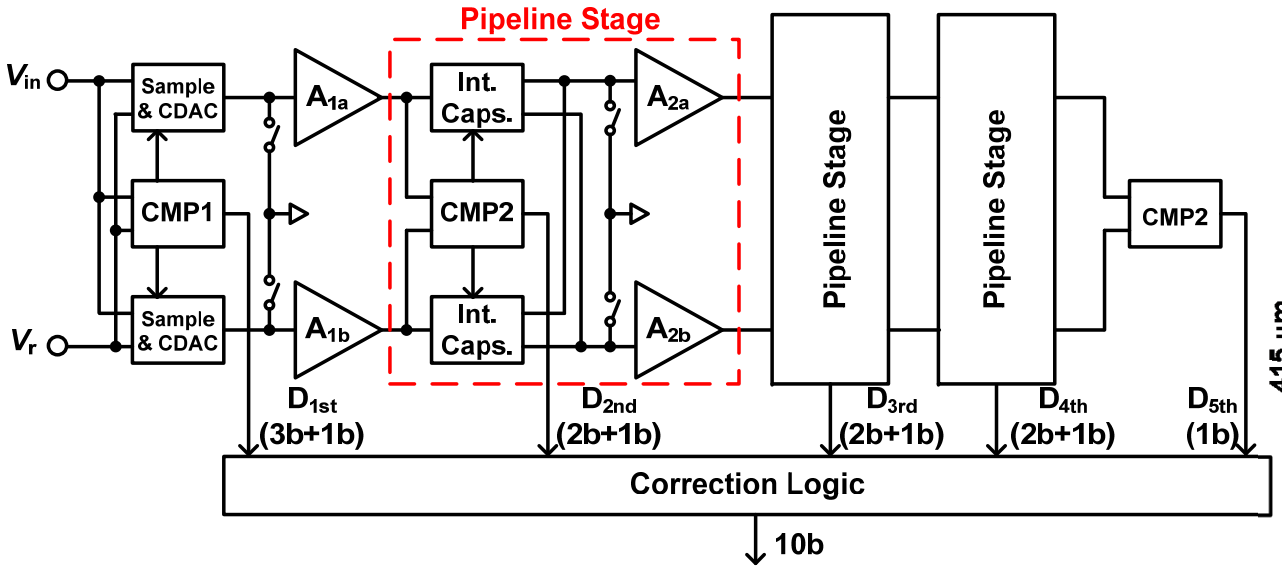
Developed ADC

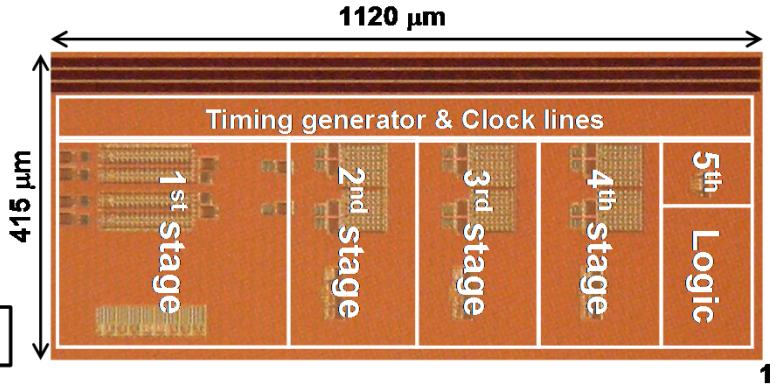
Developed new 10b ADC to address 64 QAM.

Interpolated pipeline scheme
No need of high gain OP amps

10b, 320 MSps, 40mW ADC

Suitable for low gain and low V_{DD} scaled CMOS

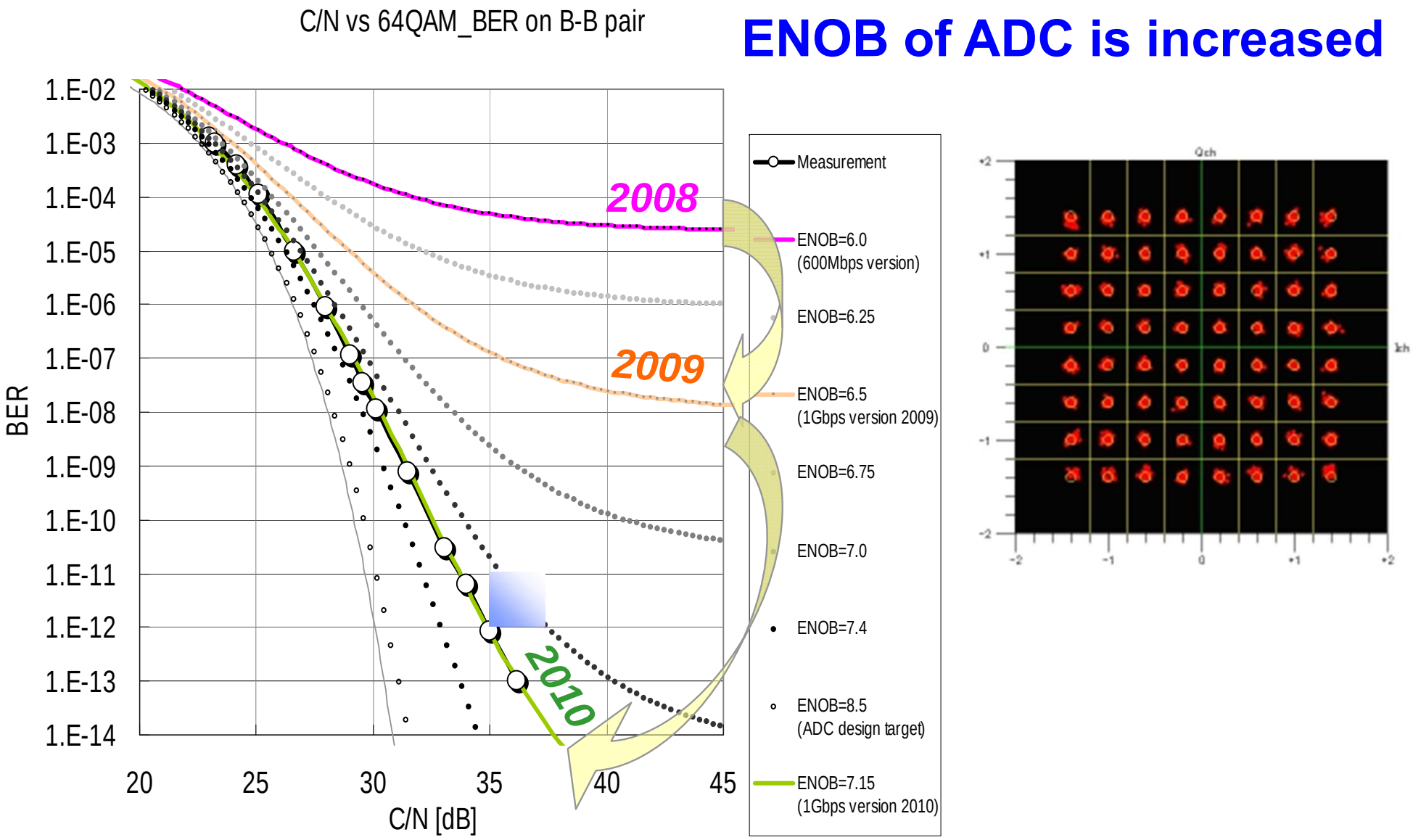




M. Miyahara, A. Matsuzawa, VLSI-CS, 2011.

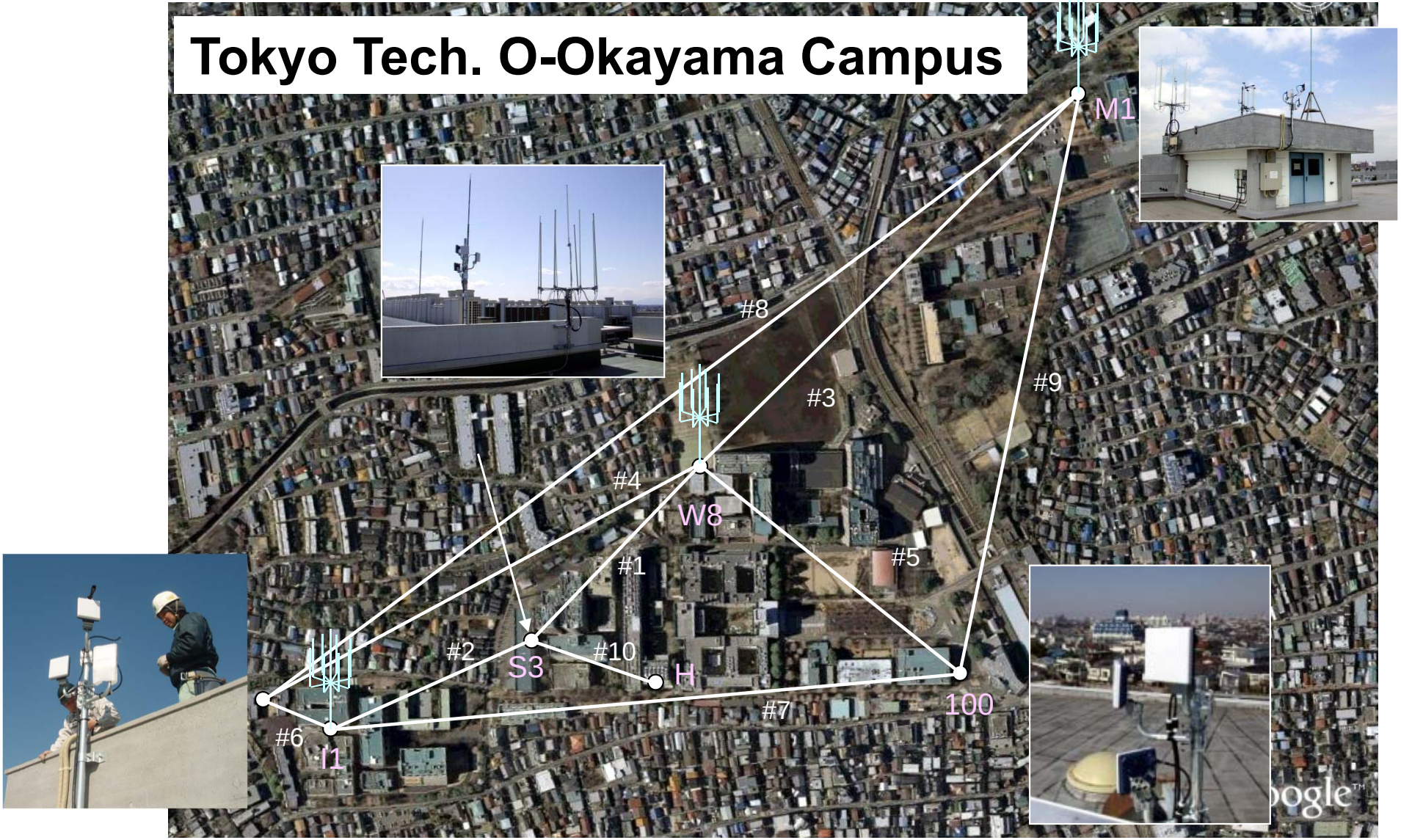
BER vs. SNR

BER for 64QAM has been reduced to the ideal



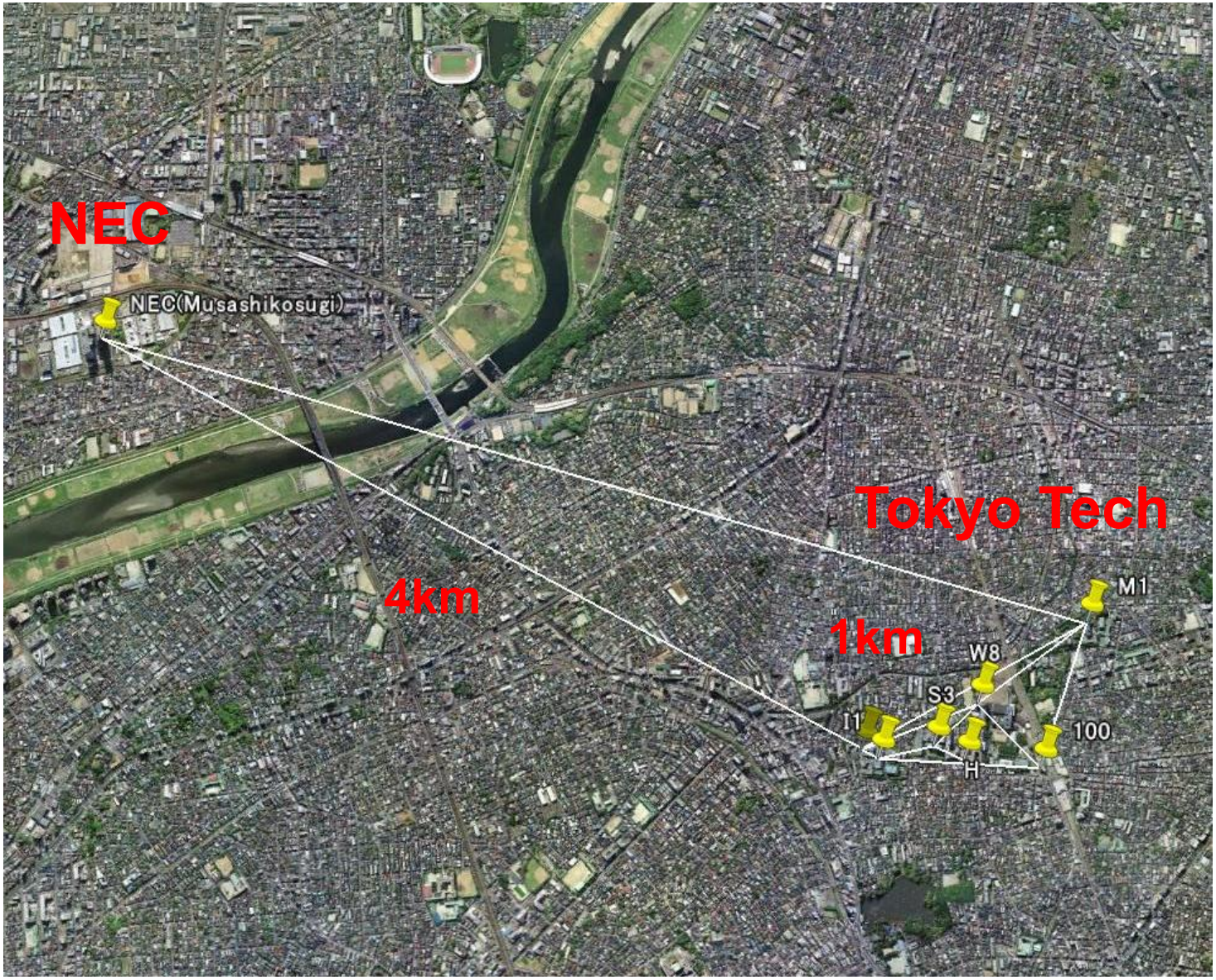
Tokyo Tech. Model Network

Ten mm-wave base stations in our campus



Expand the area to NEC (4km)

Challenge for 4km mm-wave communication

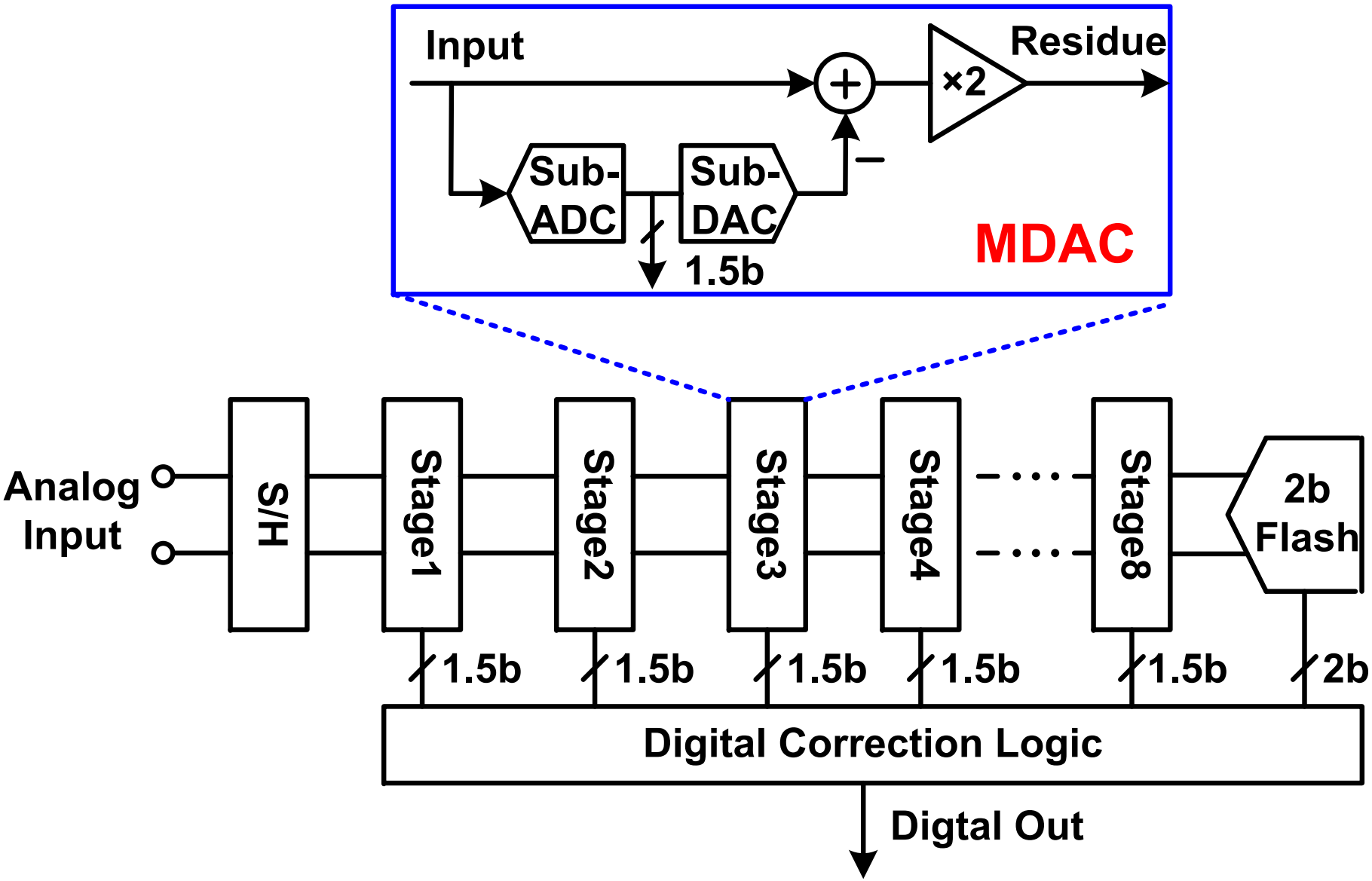


Outline

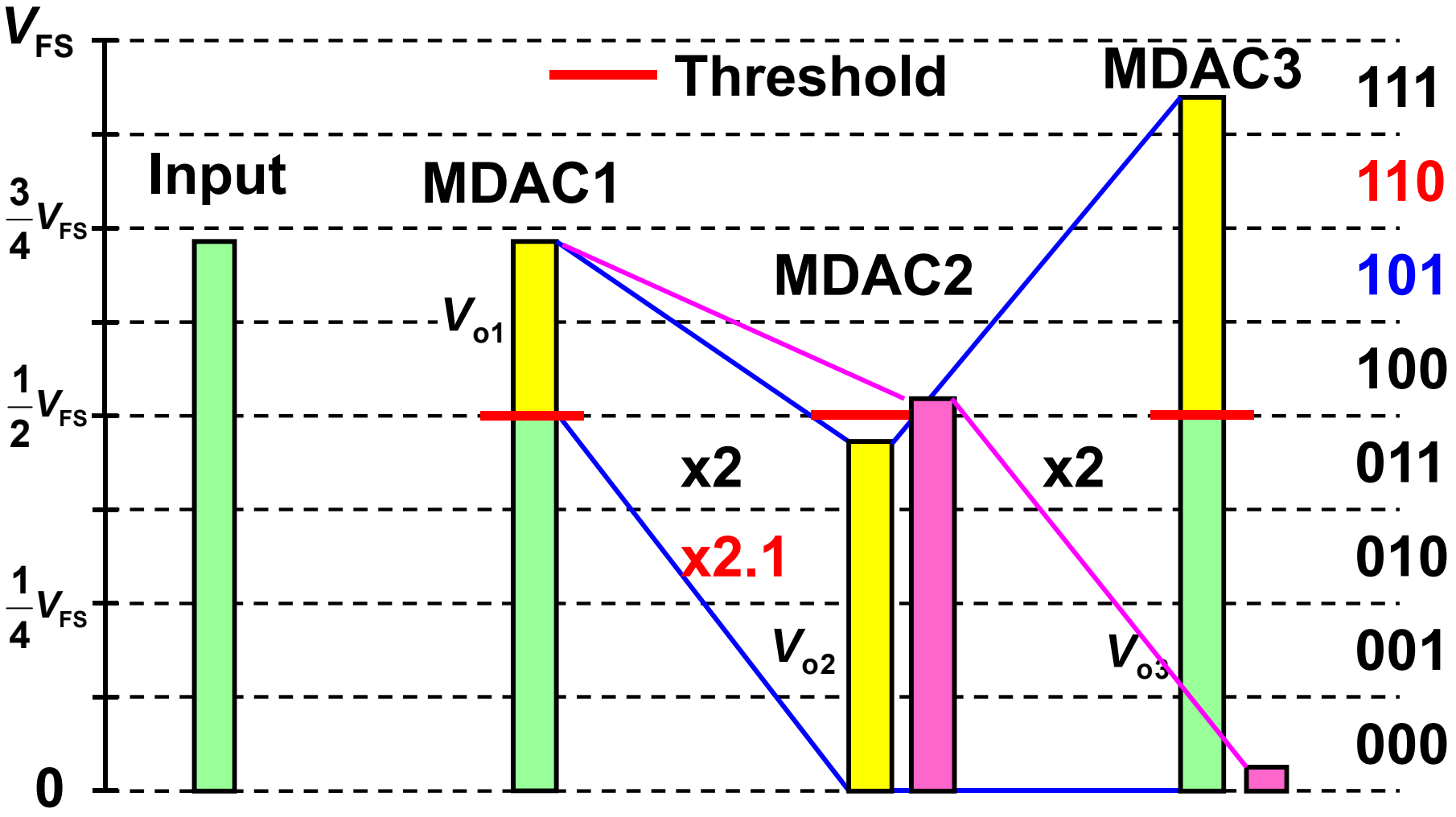
- Introduction
- Interpolation Techniques
- Circuit Implementation
- Measurement Results
- Conclusions

Conventional Pipelined ADC

Conventional pipelined ADC requires accurate MDAC



Pipelined ADC Conversion

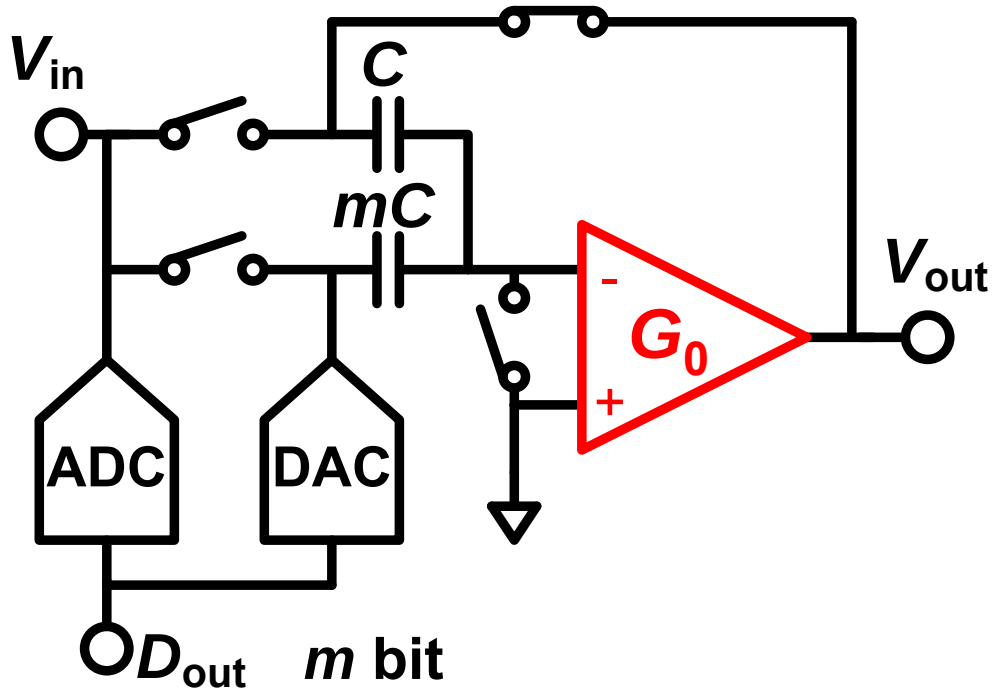


Residue V_{in} $V_{o1} = 2\left(V_{in} - \frac{1}{2}V_{FS}\right)$ $V_{o2} = 2V_{o1}$ $V_{o3} = 2\left(V_{o2} - \frac{1}{2}V_{FS}\right)$

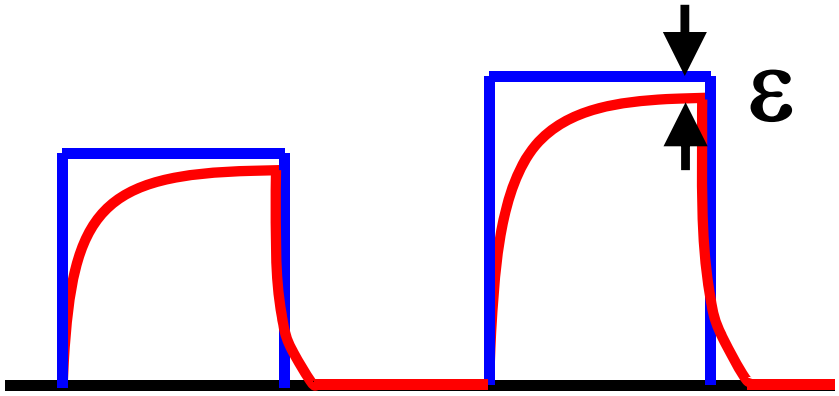
Output CODE 1 0→1 1→0

Conventional MDAC

- High DC gain OpAmp
  - Difficult to realize in scaled technology
- Closed-loop MDAC leads to lower speed



MDAC Implementation



$$G_0(\text{dB}) > 6N + 10$$

$$GBW > NF_s$$

N: Number of bits

F_s: Sampling freq.

OpAmp gain and conversion error

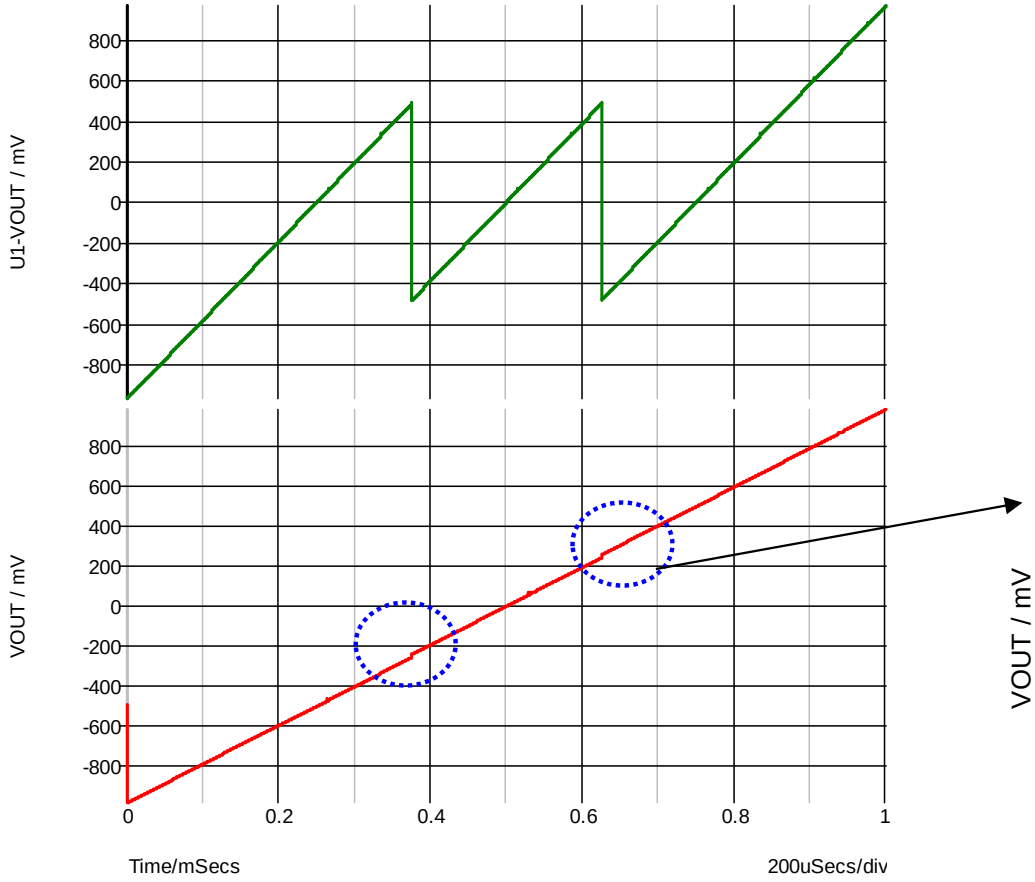
$$\varepsilon_{(LSB)} = \frac{3 \times 2^N}{G} \qquad G > \frac{3 \times 2^N}{\varepsilon_{(LSB)}}$$

$$G > 6N + 10\,(dB)$$

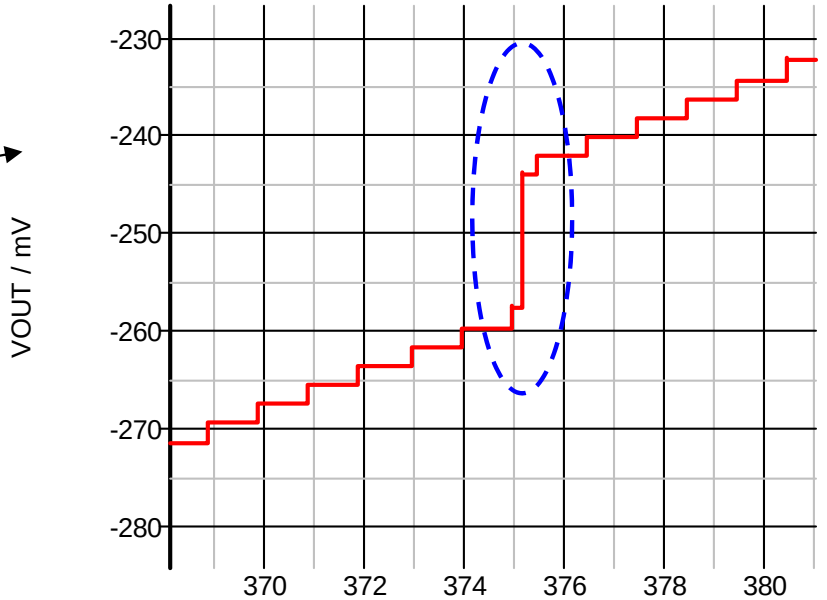
Gain>70dB

10bit ADC

Large error occurs



40dB gain



Recent Works

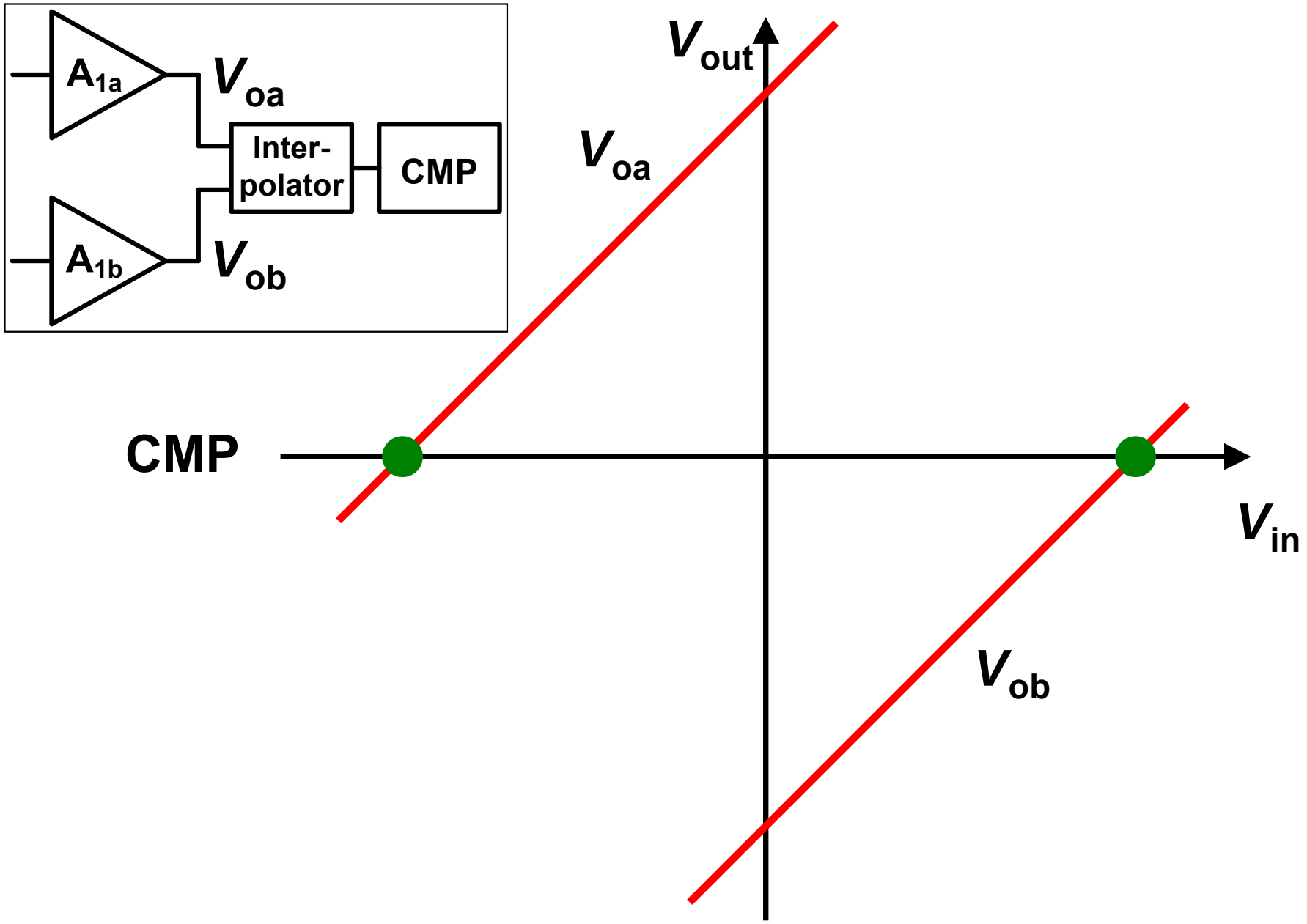
- **Digital compensation technique [1, 2]**
  - **Capacitor mismatch, gain error and opamp nonlinearity can be corrected**
    - **Simple analog circuit design**
  - **Foreground compensation**
    - **PVT variation degrade the performance**
  - **Long compensation time**
    - **Increase of test cost**

[1] B. Murmann and B. E. Boser, Dec., 2003.
[2] A. Verma and B. Razavi, Nov., 2009.

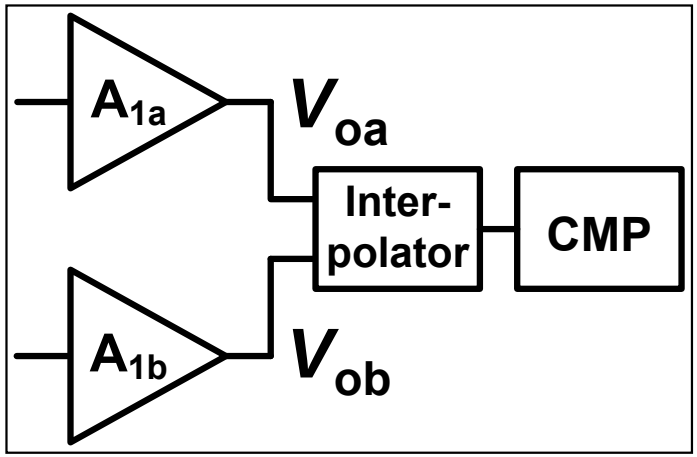
Proposed ADC

- Target : 10bit, F_s> 300 MS/s
- Interpolation and pipelined operation
  - Moderate relative gain
    - $\Delta G/G < 5\%$ for 10bit
    - Open-loop amplifiers can be used
    - No need of linearity compensation
  - Insensitive to settling time
    - High speed
    - Low power

Interpolation Architecture



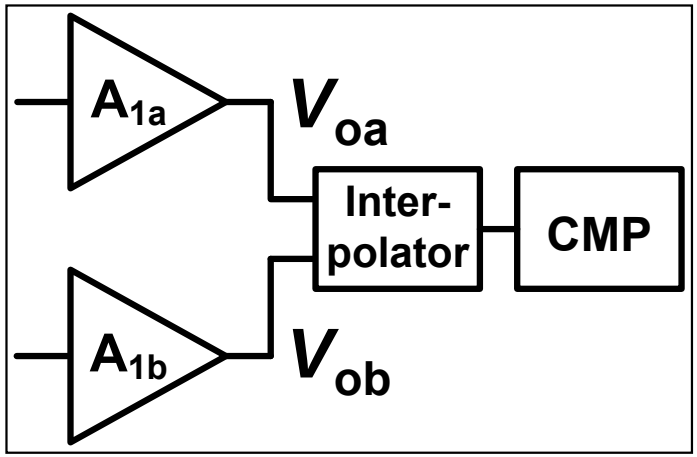
Interpolation Architecture

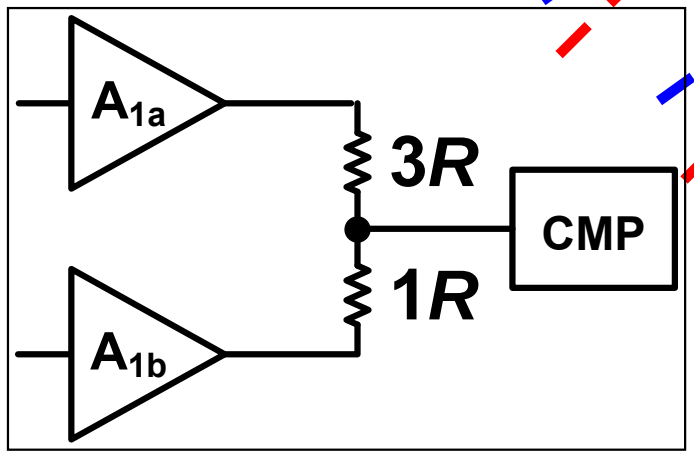


Interpolator example [3,4]

[3]A. Matsuzawa, et al. Feb. 1990.
[4]C. Mangelthdolf, et al. , Feb. 1993.

Interpolation Architecture



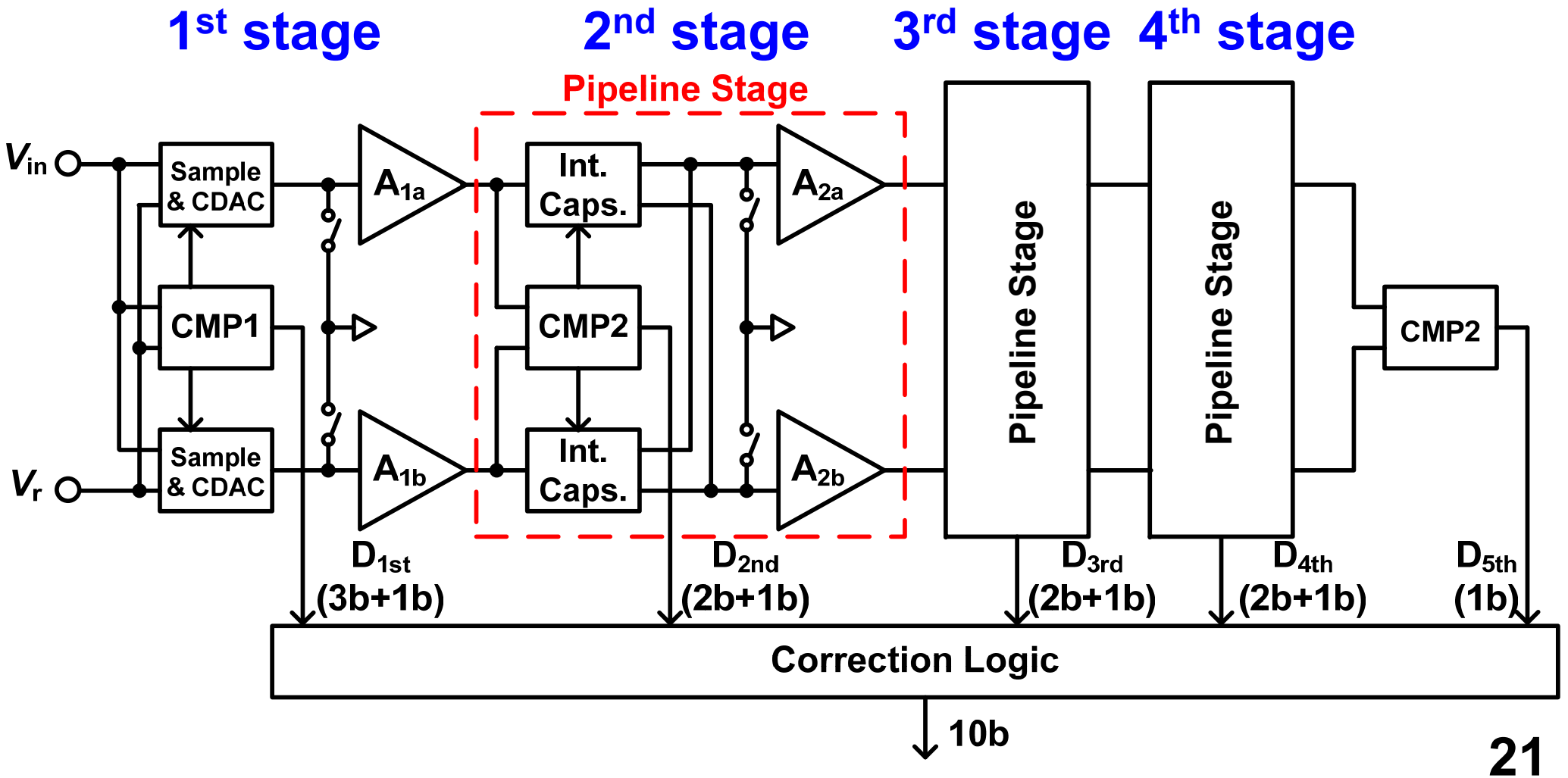


Interpolator example

Conversion error is not occurred by changing gain

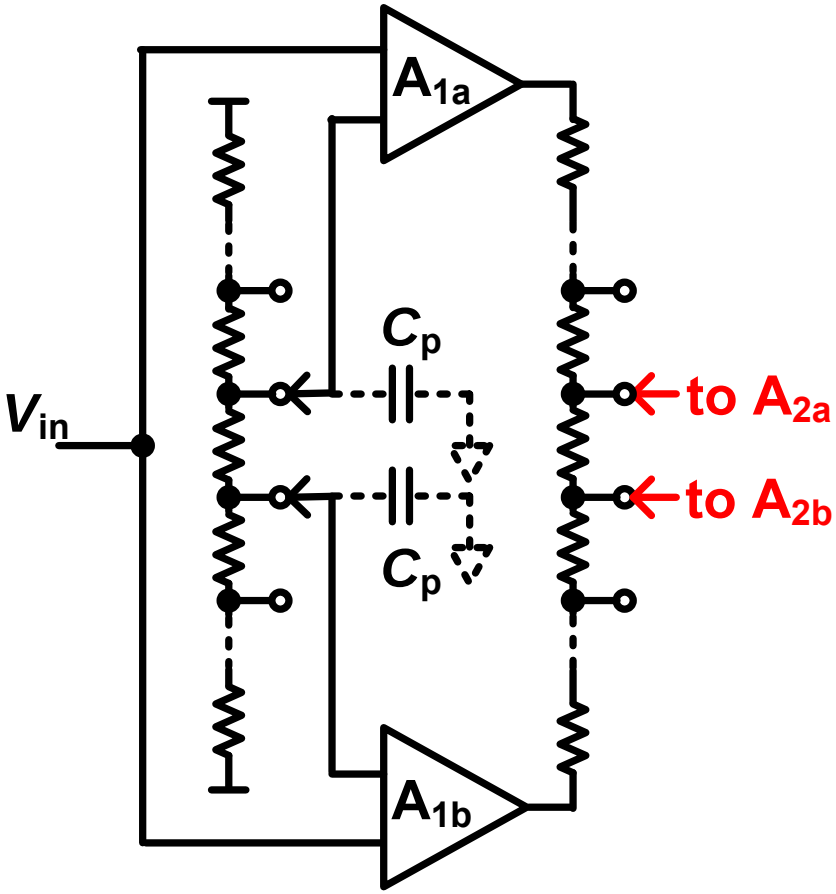
Interpolated Pipeline ADC Structure

Interpolation technique is used for 2-4th stage.
Each stage has an 1-bit redundancy.



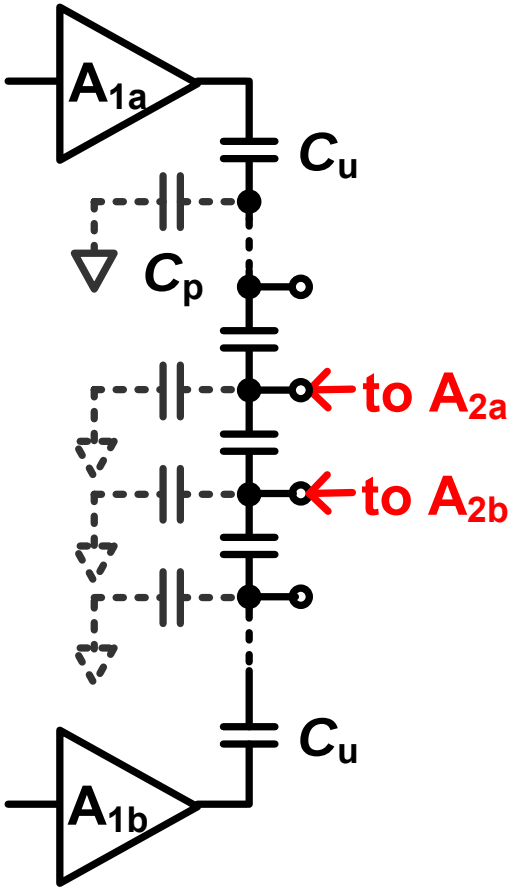
Interpolation methods

- Static current
- Good linearity
- Imbalance settling



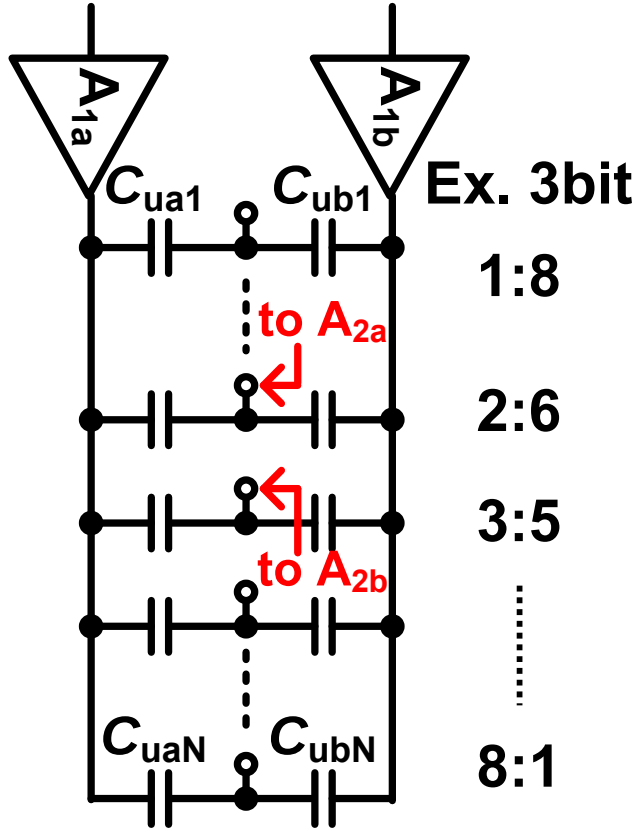
Resistive (Series) [3,4]

- No static current
- C_p causes nonlinearity



Capacitive (Series)

- No static current
- Good linearity
- Heavy load

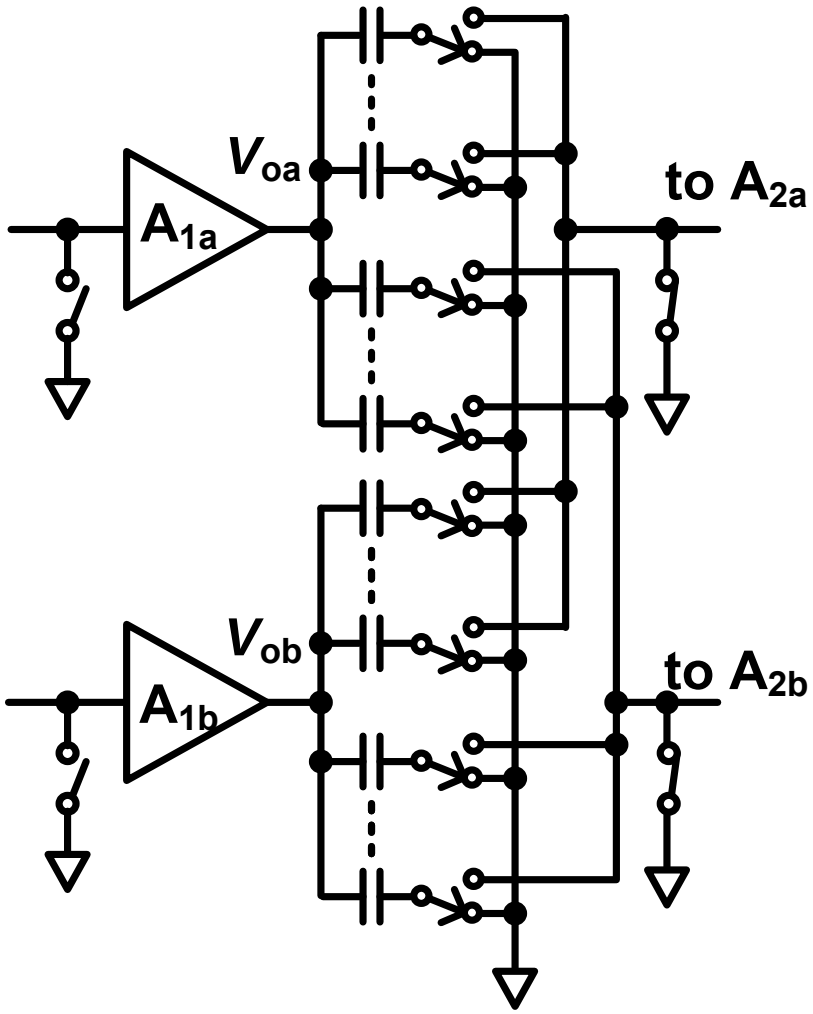


Total:36Cu

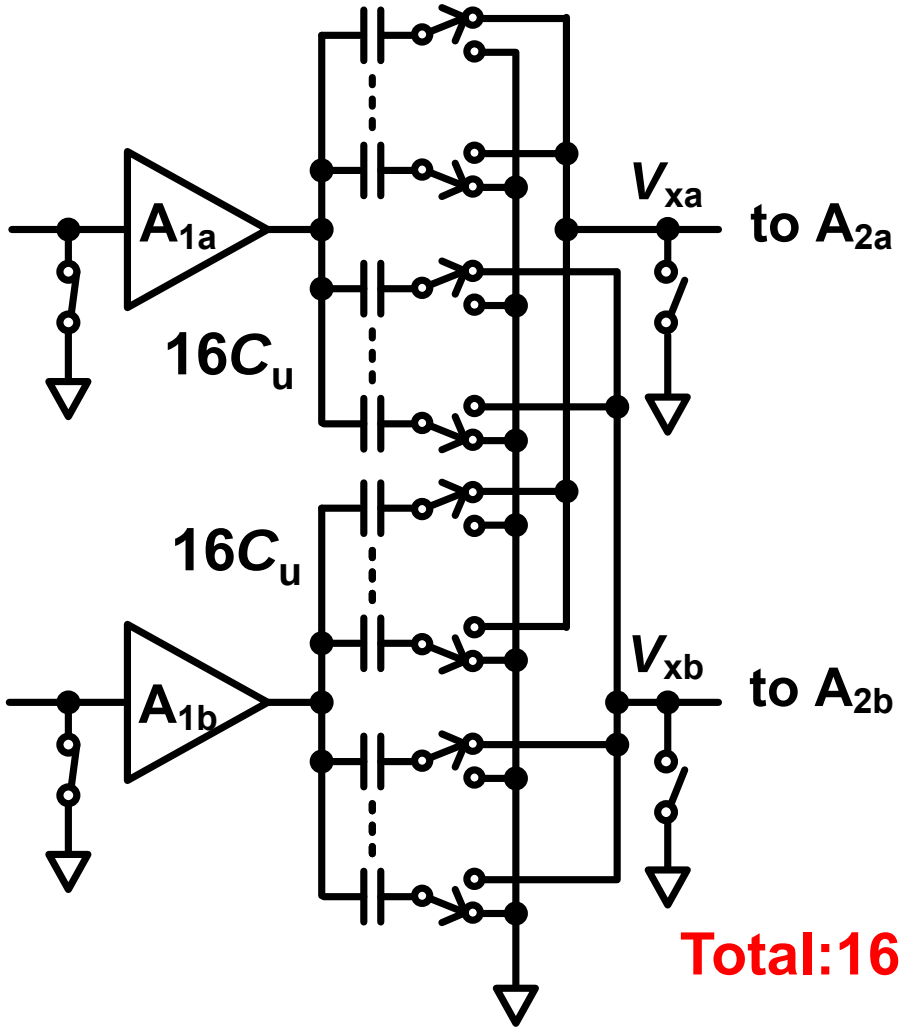
Capacitive (Weighted)

Proposed Weight Controlled Capacitor Array

Sub-ADC controls the capacitor weight.
Load capacitance is reduced from $36C_u$ to $16C_u$ (3bit).



Sampling Phase



Interpolation Phase

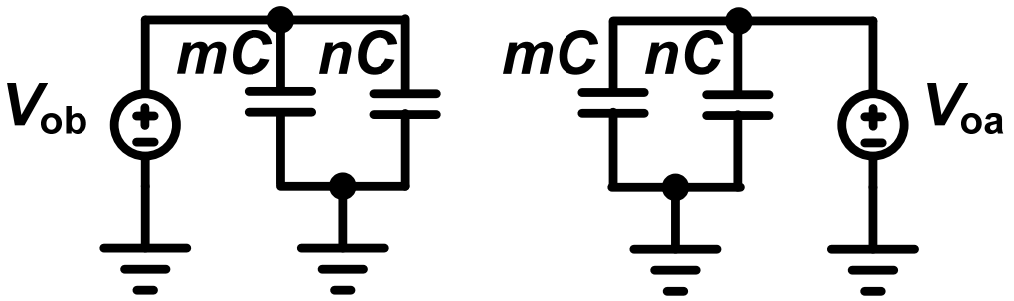
Total:16Cu

Weight Controlled Capacitor Array

Offset voltage can be cancelled in interpolation phase

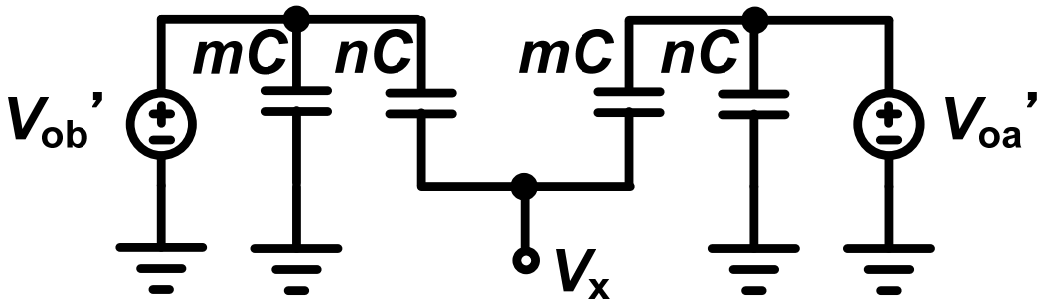
$$V_x = -\left[\frac{m}{m+n}G_a\left(V_{in}-V_{ra}\right)+\frac{n}{m+n}G_b\left(V_{in}-V_{rb}\right)\right]$$

$2^M = m+n$



Sampling phase

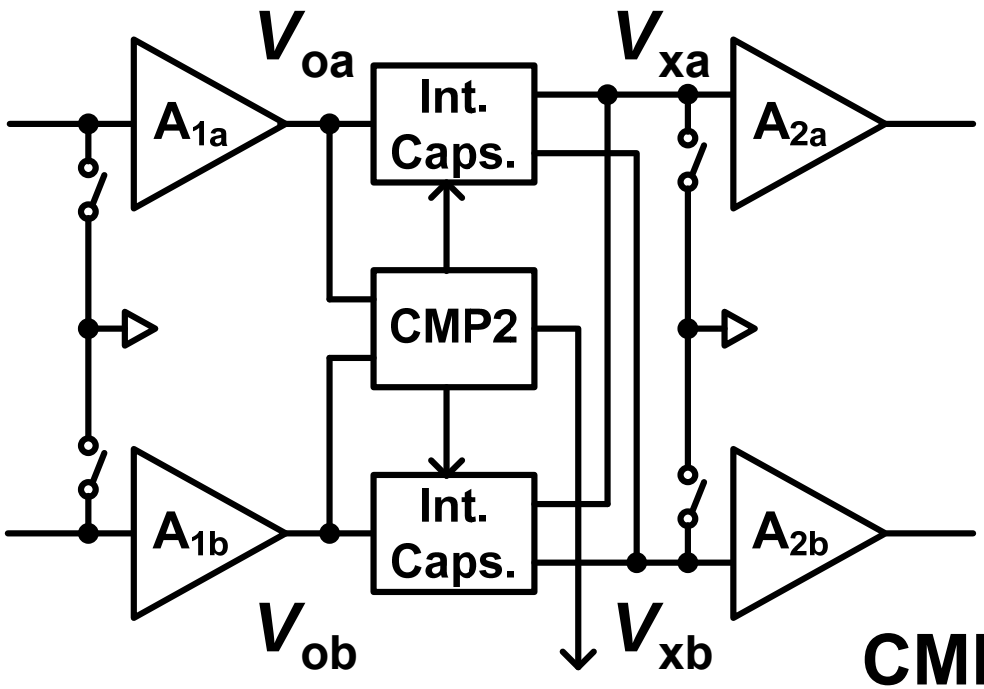
$$V_{oa} = G_a\left(V_{in}-V_{ra}-V_{off\_a}\right)$$
$$V_{ob} = G_b\left(V_{in}-V_{rb}-V_{off\_b}\right)$$
$$V'_{oa} = G_a\left(-V_{off\_a}\right)$$
$$V'_{ob} = G_b\left(-V_{off\_b}\right)$$

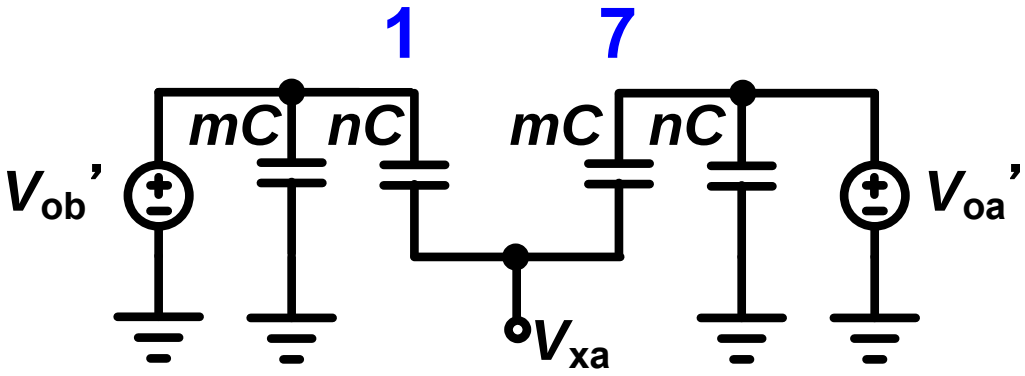


Interpolation phase

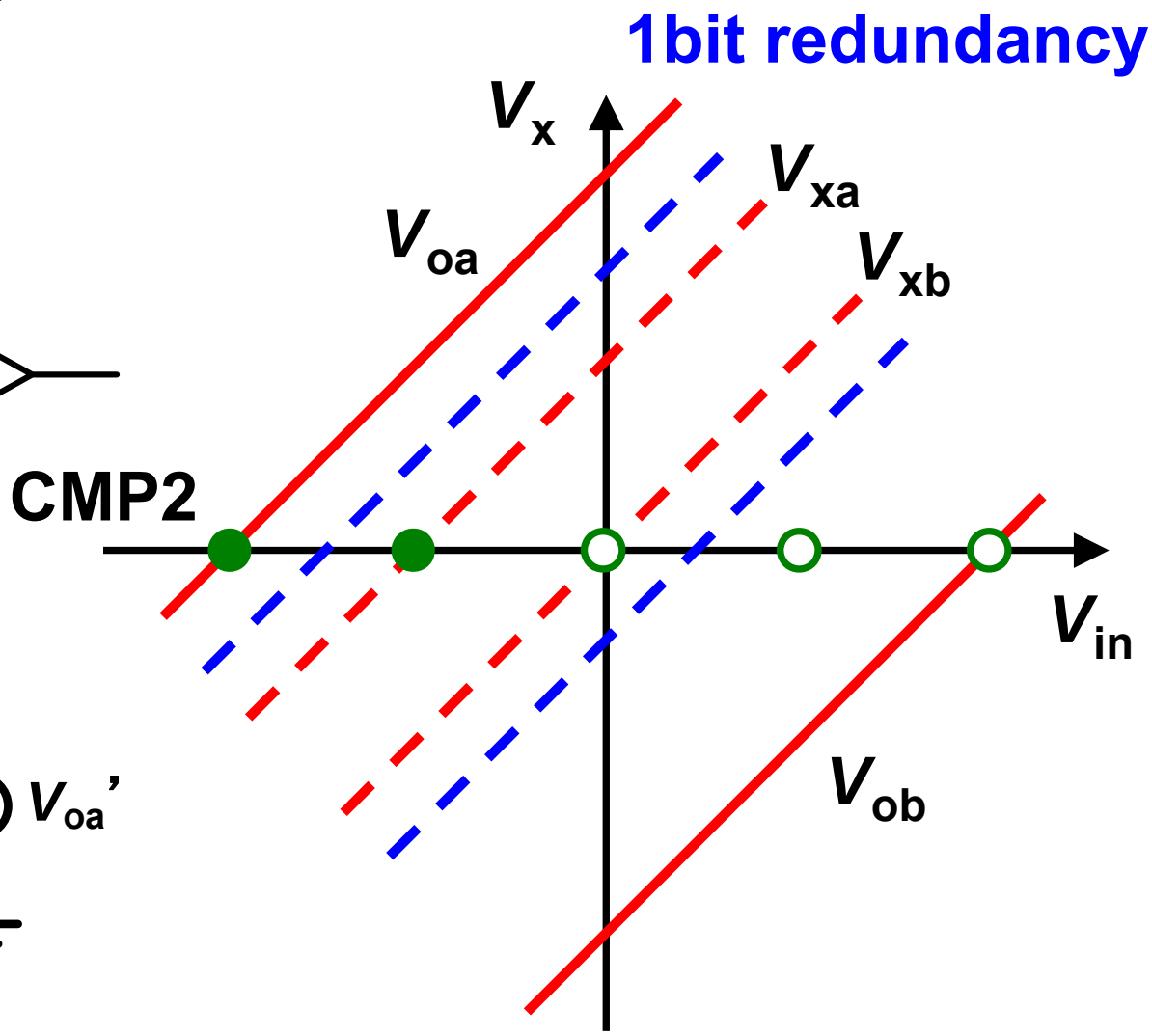
G_a, G_b: Gain of A_{1a} and A_{1b}
V_{oa}, V_{ob} : Output voltage
V_{off_a}, V_{off_b}: Offset voltage
V_{ra}, V_{rb}: Reference voltage
m, n : Capacitor weight

Interpolated Output





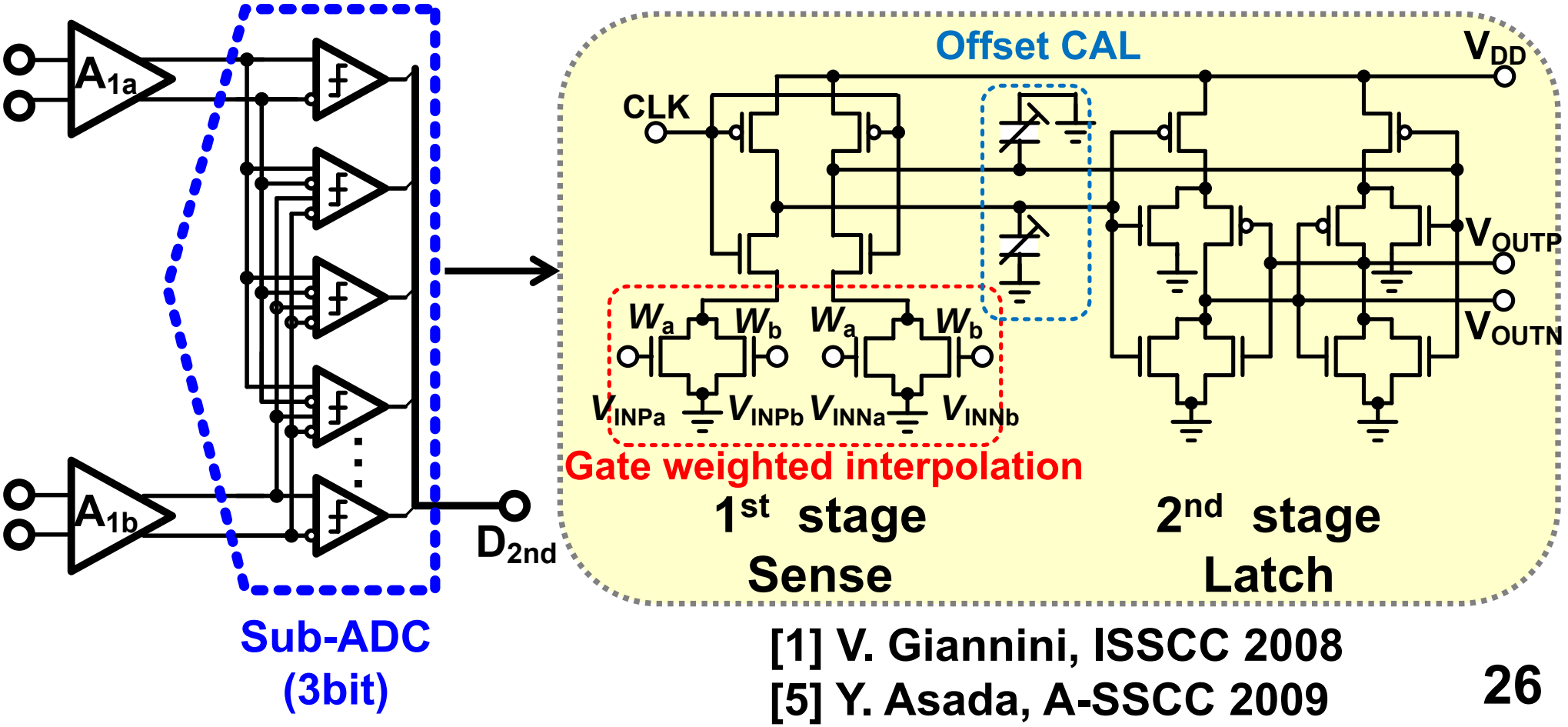
Interpolation phase



Sub-ADC Structure

Gate-width-weighted interpolation comparators with capacitive offset calibration is used.

- **Offset voltage < 2 mV (σ)**



[1] V. Giannini, ISSCC 2008
[5] Y. Asada, A-SSCC 2009

Requirements for An Amplifier

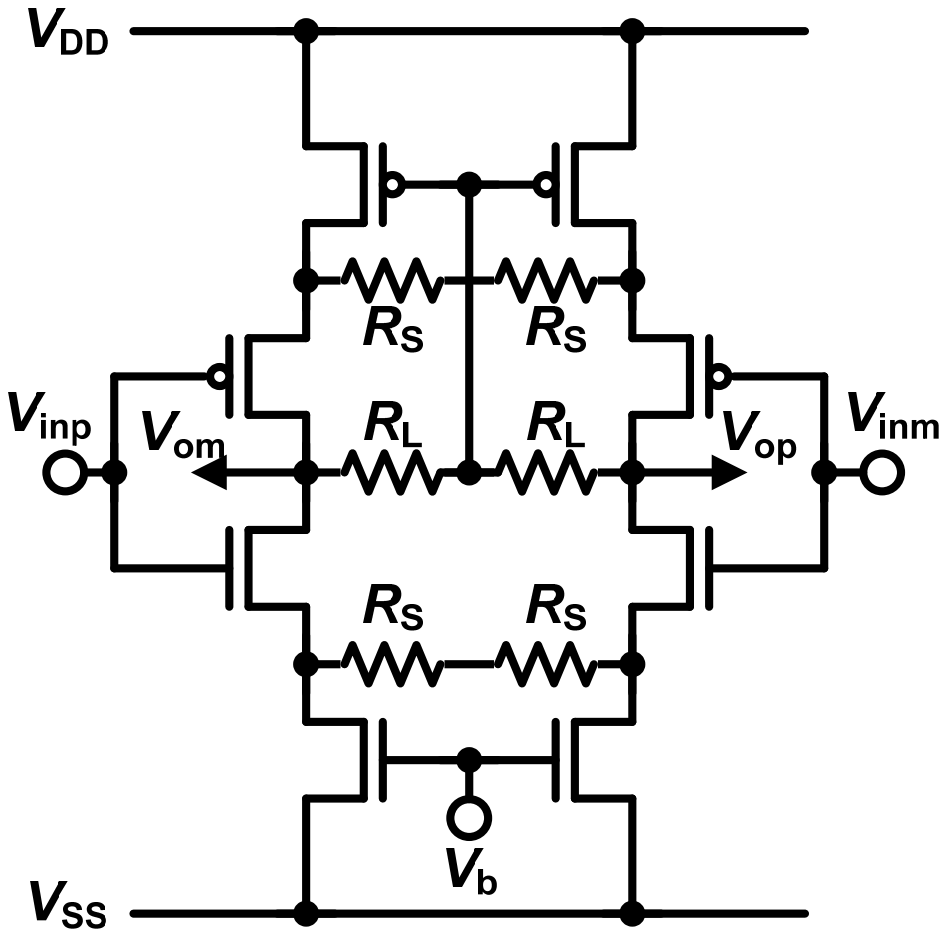
- Absolute Gain error ⇒ No error
- Offset voltage ⇒ DNL error
  - Offset voltage < 1LSB
    - Offset voltage can be negrected by output offset cancel technique.
- Gain mismatch ⇒ DNL error
- Linearity ⇒ DNL and INL error

Amplifier : Schematic

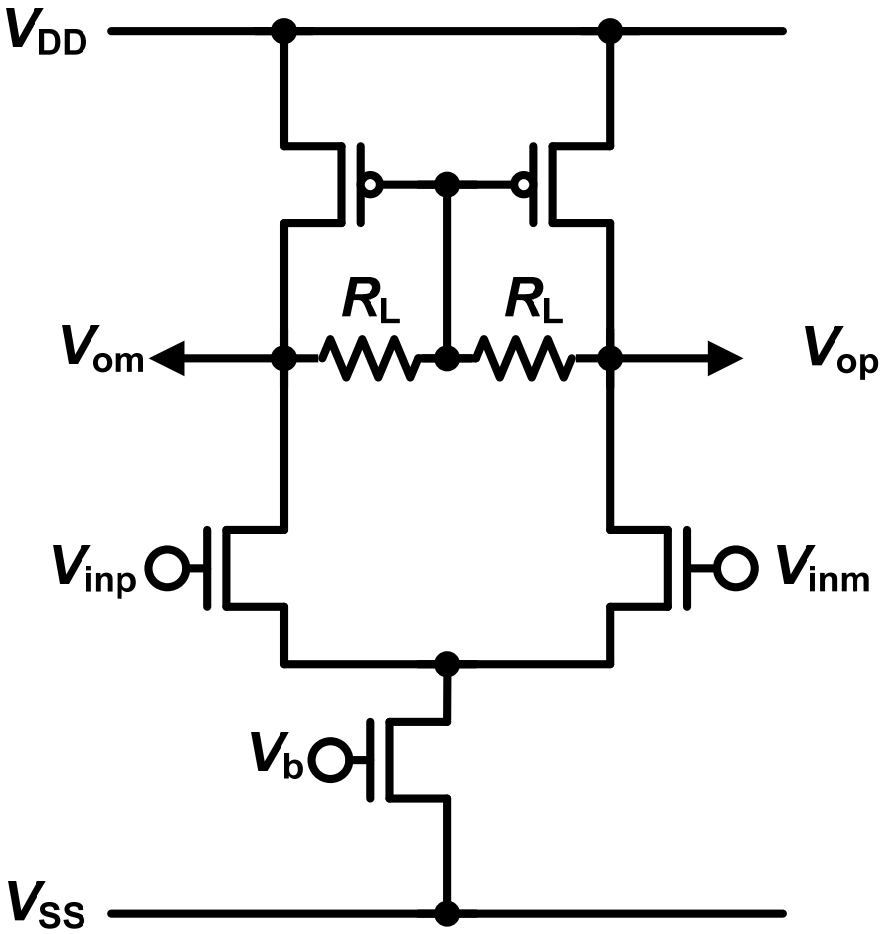
1st stage amplifier require good linearity

=>CMOS input with source degenerations

Gain mismatch < 2.1%(3σ)



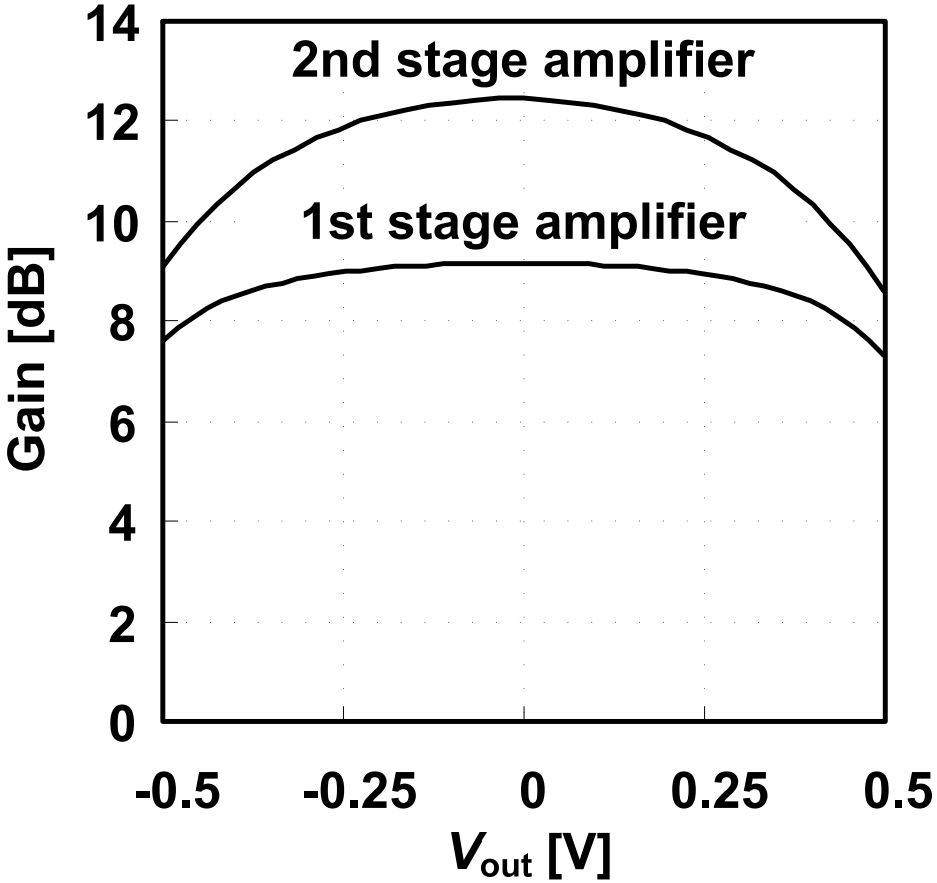
1st stage amplifier



2nd stage amplifier

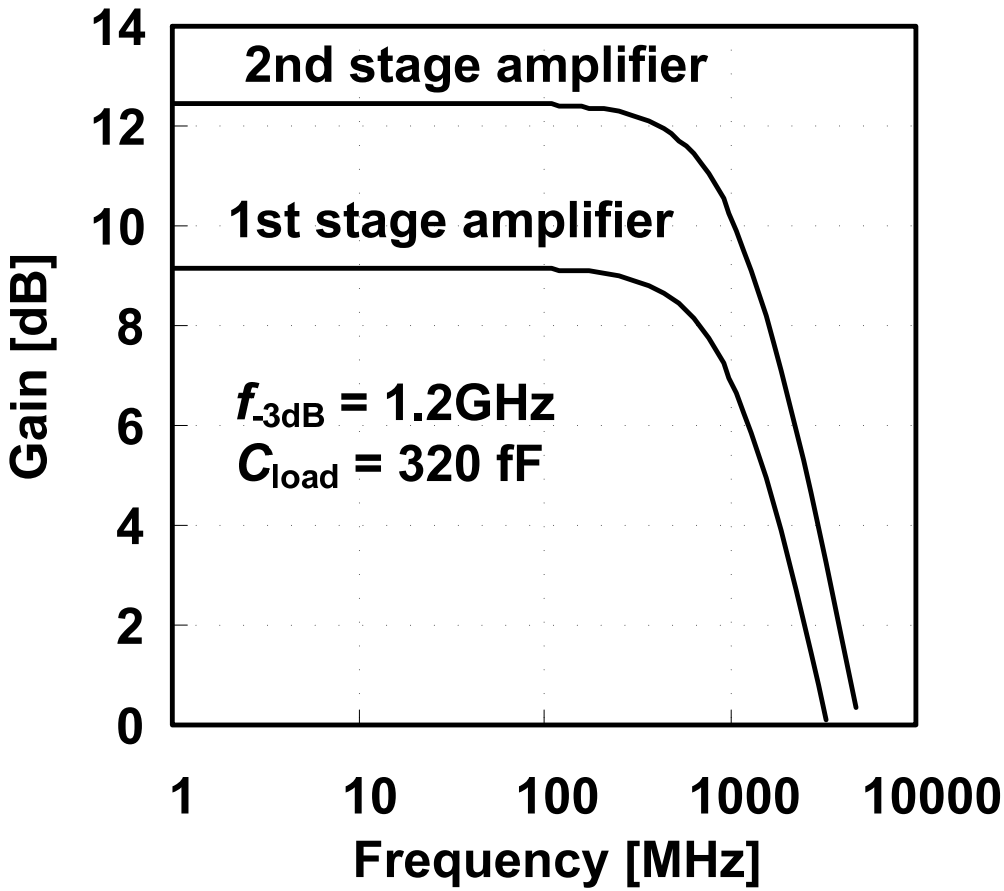
Amplifiers : Simulation results

$$V_{out} \approx a_1 V_{in} - a_3 V_{in}^{\ 3}$$



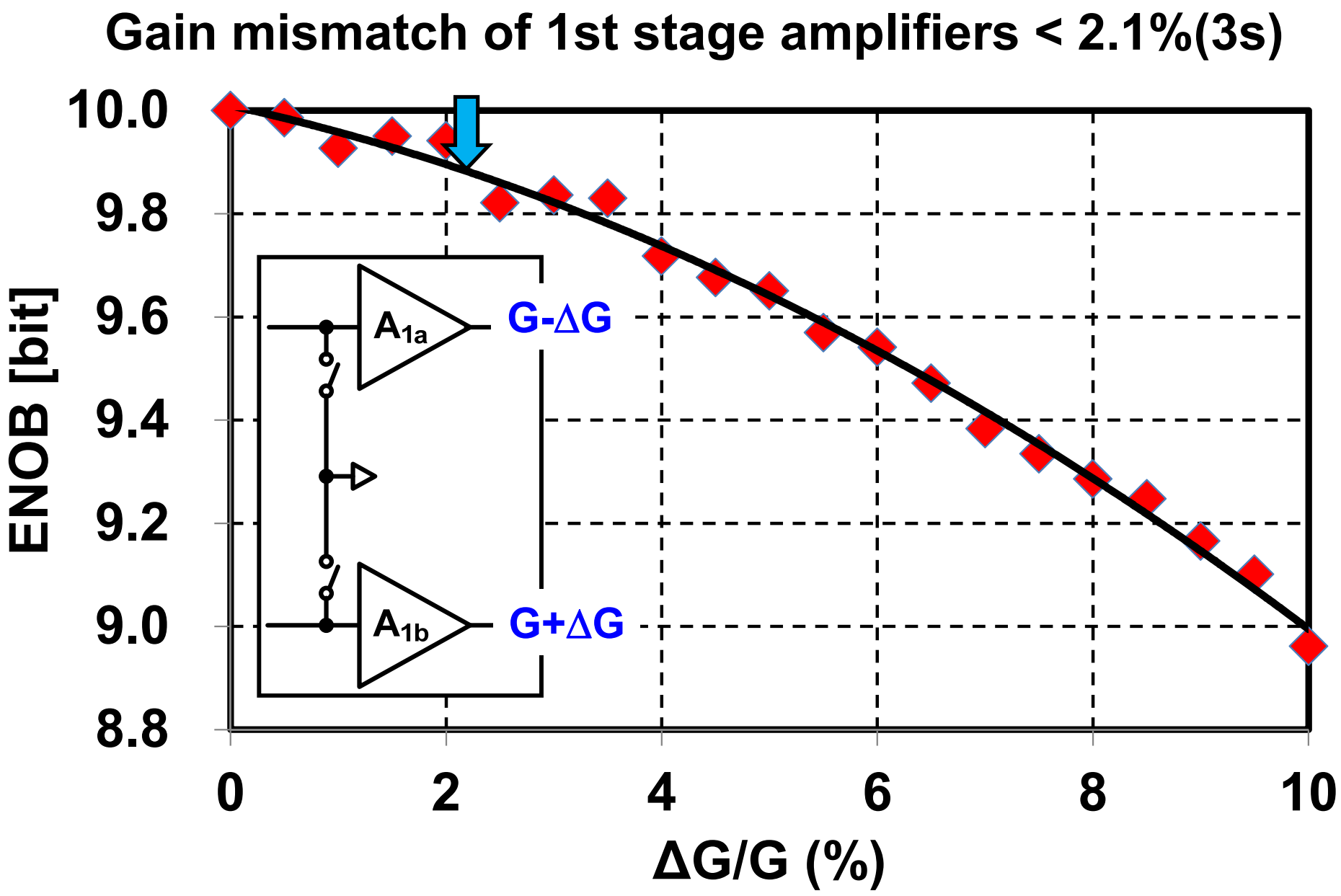
Output voltage vs. DC gain.

1st stage $a_3/a_1 < 1.3$
2nd stage $a_3/a_1 < 6.2$

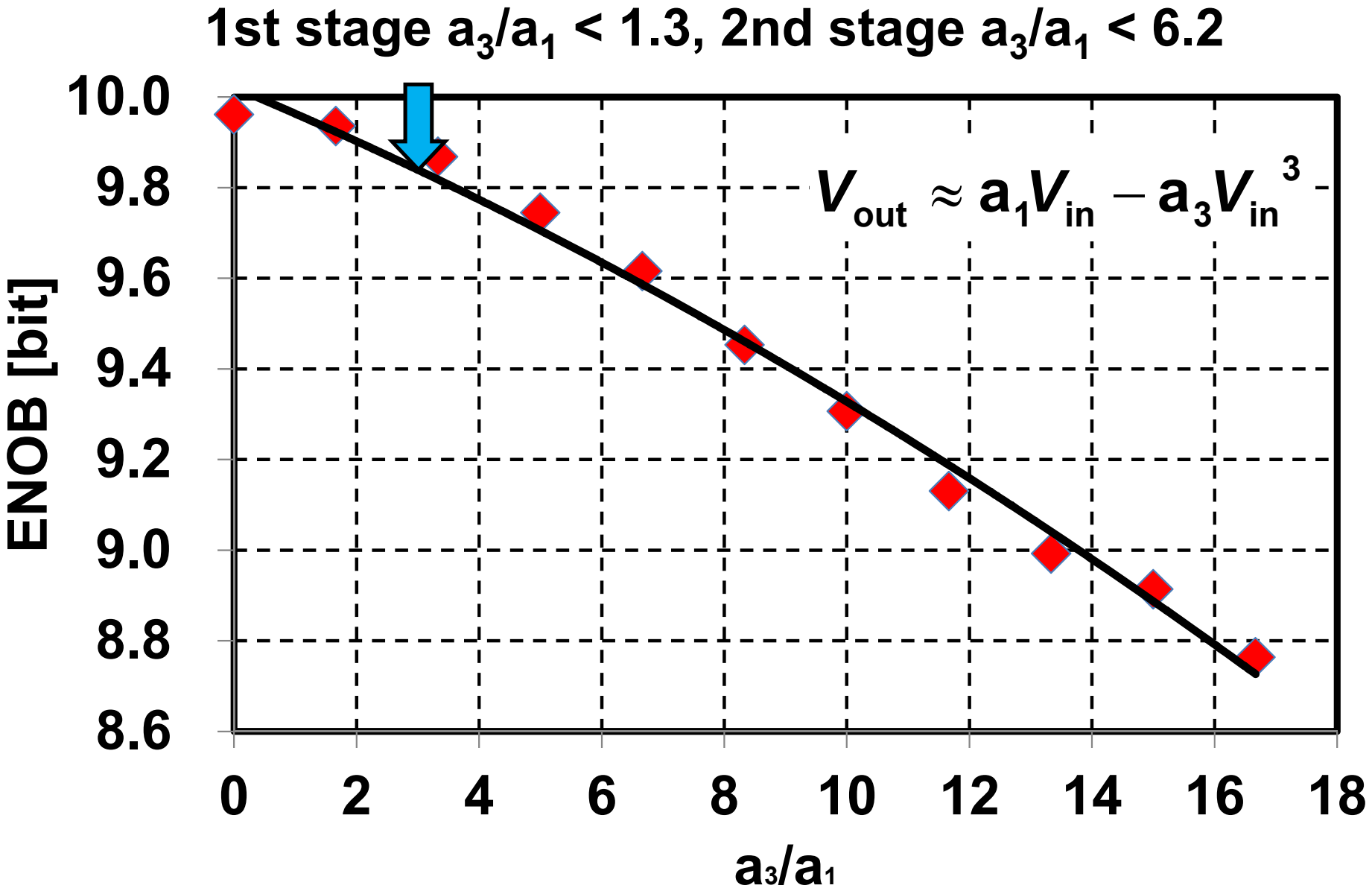


Frequency vs. gain.

Gain matching requirement

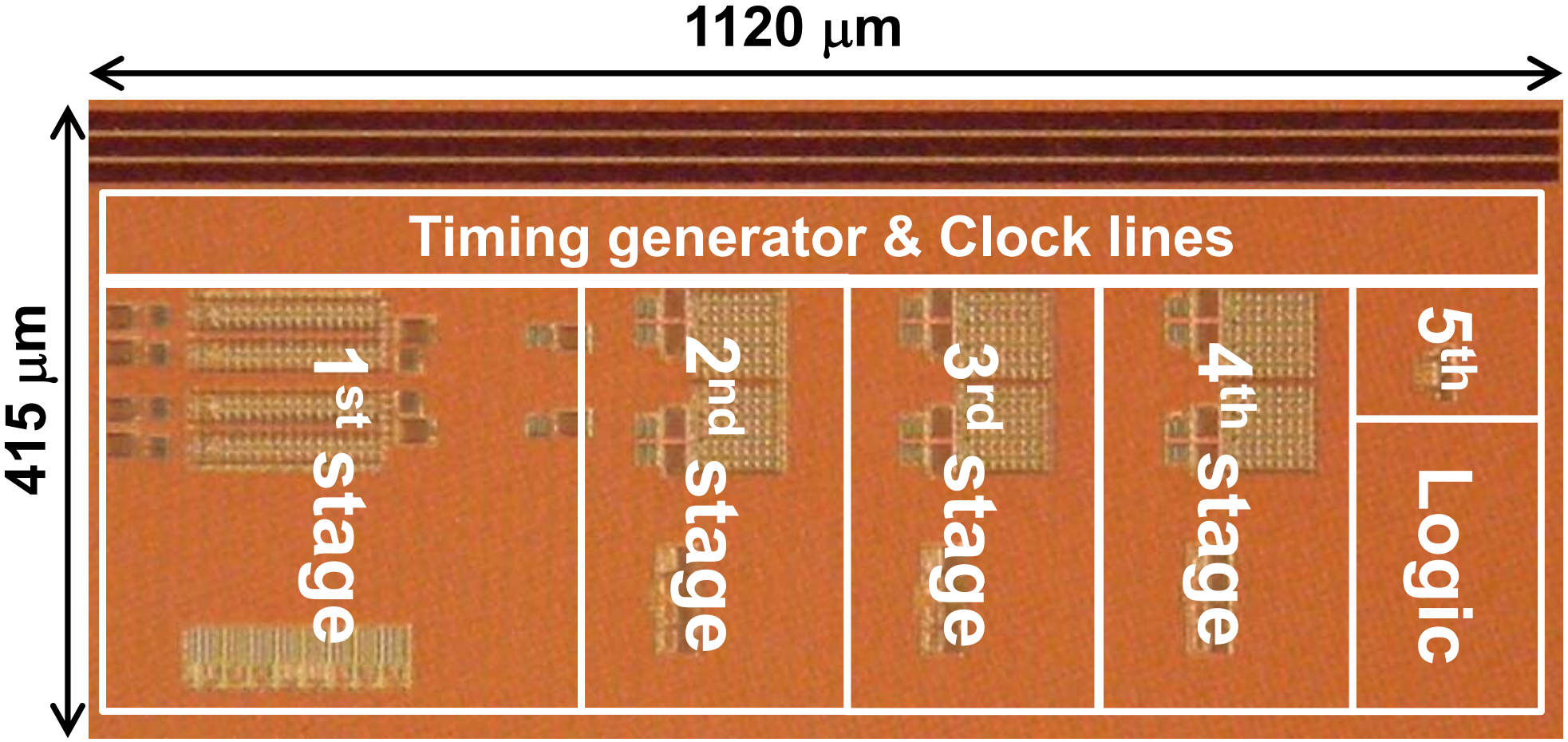


Linearity Requirement



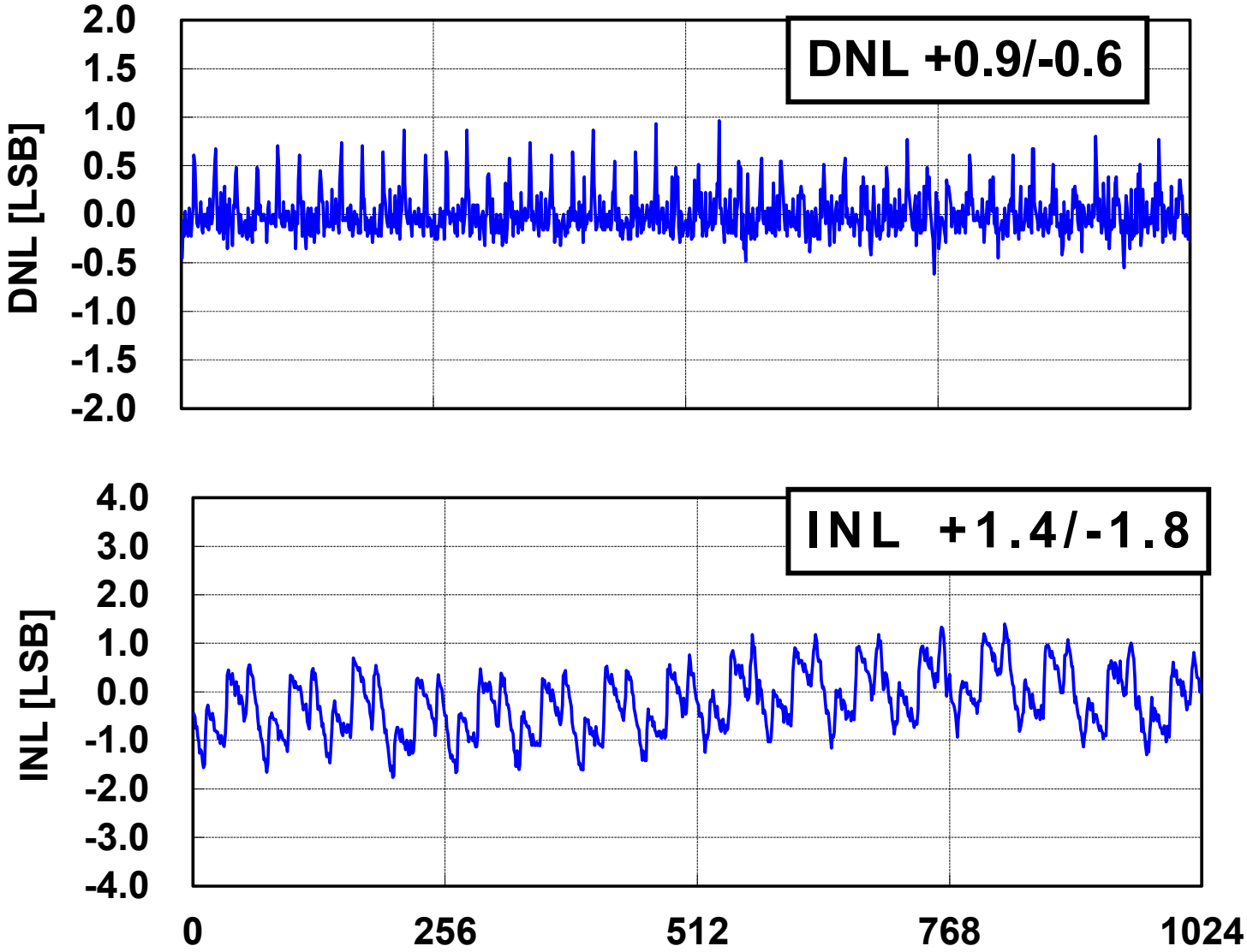
Chip photo

- 90 nm 10M1P CMOS technology
- Chip area of 0.46mm^2

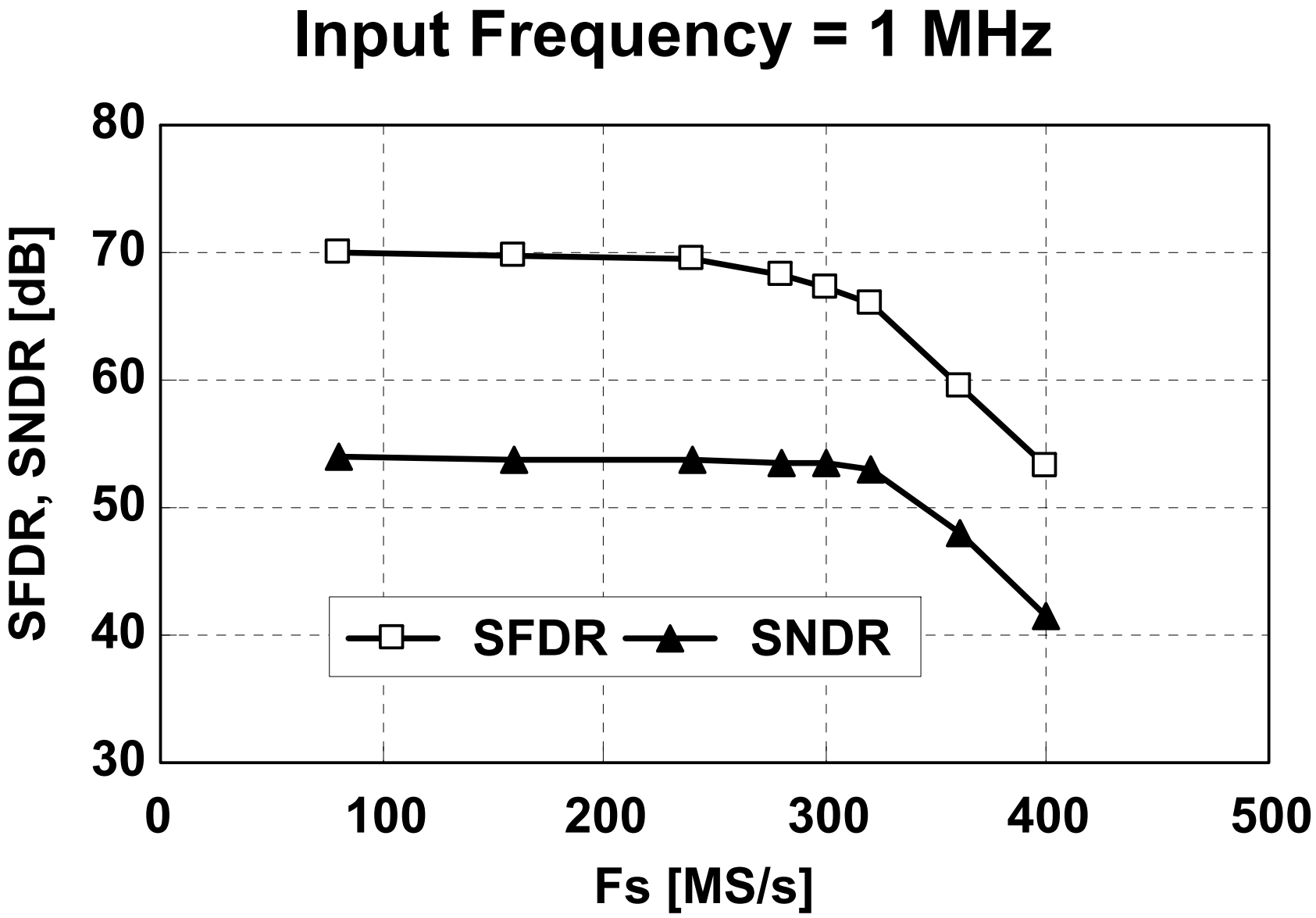


DNL, INL

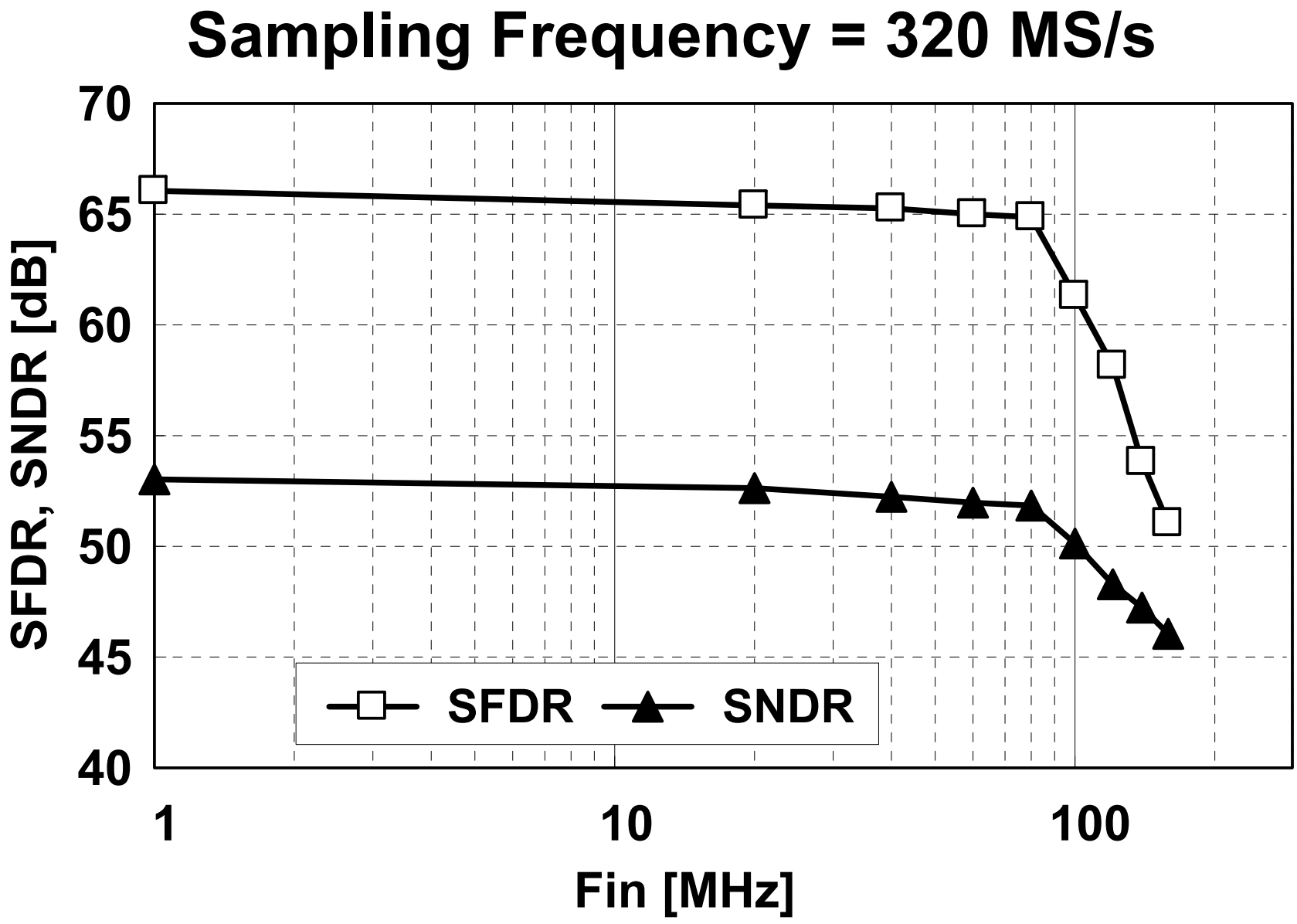
This periodical error is due to bad layout, not essential issue.



Sampling Frequency vs. SNDR



Input Frequency vs. SNDR



Performance summary

	This Work	[2]	[6]	[7]
Resolution (bit)	10	10	10	10
F_{sample} (MS/s)	320	500	205	320
V_{DD} (V)	1.2	1.2	1.0	-
Power (mW)	40	55	61	42
$ENOB_{peak}$ (bit)	8.5	8.5	8.7	8.7
FoM_{Fs}/ FoM_{ERBW} (pJ/c.-s)	0.35 / 0.77	0.31	0.65	0.36/0.44
Technology (nm)	90	90	90	90
Active Area (mm^2)	0.46	0.5	1	0.21
Amplifier type	Open	Closed	Closed	Closed
Linearity Compensation	No	Yes	No	Yes

[2] A. Verma and B. Razavi, IEEE J. Solid-State Circuits, vol. 44, Nov., 2009.
[6] S. Lee, Y. Jeon, K. Kim, J. Kwon, J. Kim, J. Moon, and W. Lee," ISSCC, 2007.
[7] H. Chen, W. Shen, W. Cheng, and H. Chen, A-SSCC, 2010.

Conclusions

- **An interpolated pipelined ADC using open-loop amplifier has been proposed.**
  - **Interpolation architecture**
    - **$\Delta G/G < 5\%$ for 10bit**
    - **Using simple open-loop amplifiers enables high speed operation**
    - **No need of a linearity compensation**
  - **Weight Controlled Capacitor Array**
    - **Load capacitance is reduced from $36C_u$ to $16C_u$**
    - **Offset voltage of the amplifier can be cancelled**
  - **10bit, 320MS/s, 40 mW ADC has been realized**

Future Prospect

- **Issue: Need twice larger circuits**
  - **Same capacitance as for the conventional pipeline ADC can be used by modifying circuits.**
  - **Area and power can be reduced, since lower bandwidth is acceptable.**

- **Still need the pipelined ADC?**
  - **SAR ADC: lowest FoM, but low f_s and low resolution.**
  - **SAR-Pipeline: higher resolution, but lower f_s due to multi step conversions.**
  - **Interleaving: effective for low resolution ADC, but need totally large capacitance.**