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n-Channel Metal–Oxide–Semiconductor Field-Effect Transistor Modeling in Forward Body Bias Condition for Low Voltage Complementary Metal–Oxide–Semiconductor Circuits Design

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This paper proposes a modified transistor model to improve the accuracy under the forward body bias operation that is vital for low voltage circuits, such as 0.5 V, to reduce the power consumption of complementary metal–oxide–semiconductor (CMOS) LSI. The proposed model and equations were implemented in BSIM4 version 4.6 with SPICE3f5 and verified by measurements of 60 nm n-channel metal–oxide–semiconductor field-effect transistors (n-MOSFETs). Approximately 50% inaccuracy of the drain current can be corrected. Furthermore, the importance of the proposed model will become higher with further lower threshold voltage operation requirements. © 2012 The Japan Society of Applied Physics

1. Introduction

In order to reduce power dissipation while maintaining speed of any circuits in battery supplied portable systems, the importance of low voltage sub-100 nm complementary metal–oxide–semiconductor (CMOS) technology is increasing.[1] An effective approach to operate metal–oxide–semiconductor field-effect transistors (MOSFETs) at low bias voltages is a forward body-biasing scheme for extending bulk-Si CMOS technology scaling. A forward body bias improves threshold voltage roll-off behavior and enables the use of shorter gates, as explained by a quasi-two-dimensional (2D) model.[2]

To simulate circuits with the forward body-biasing scheme, the MOSFET model is the key to reproduce the effect[3–5] accurately. However, there are two major problems to characterize n-MOSFETs. One is the threshold voltages of n-MOSFETs that cannot be monotonically scaled whereas p-MOSFETs can. The other is the bulk charge which is mainly affected in the velocity saturation region.

During our circuit design process, we found that the existing MOSFET compact models, including BSIM3,[6] 4,[7] and HiSIM2,[8] do not make sufficient attention to the forward body bias operations. In particular the simulated drain current of n-MOSFET by the circuit simulator is much lower than the measured value under the forward body bias condition. So far, existing sub-micron MOSFET models including HiSIM2, BSIM4, PSP,[9] and EKV3[10] describe the drain current formulation only under null and reverse body biases. An empirical equation of threshold voltage for forward body biases is written only in BSIM4 model source code.[7] It is needed to develop a physical based model to simulate drain current in forward body biases in addition to null and forward body bias operations with sufficient accuracies.

We first formulate depletion thickness (X_d) which is dominant to determine the threshold voltage (V_TH) using vertical and horizontal doping profiles. Next the bulk charge effect dependencies on reverse to forward body biases are analyzed and modeled. Then, these results are implemented into BSIM4 as an instance for simulating drain current from reverse to forward body bias ranges. Finally, the model is compared with measurement of 60 nm n-MOS transistors.

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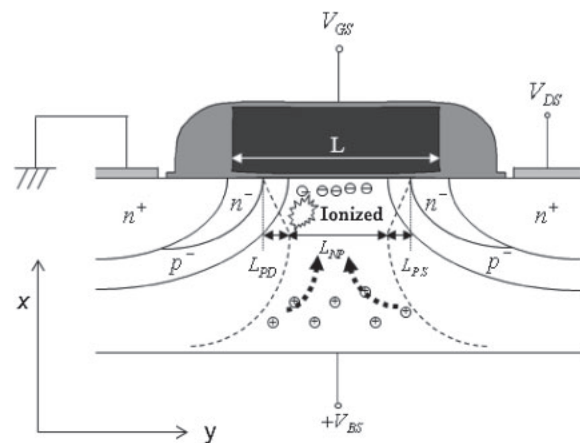

Fig. 1. Cross-sectional diagram of a pocket n-MOSFET structure in the state of forward body biases. Inset illustration shows the ionization mechanism when the forward body bias was supplied.

2. Modeling

2.1 Threshold voltage

As shown in Fig. 1, non-uniform doping profiles can be categorized into vertical non-uniformity and lateral non-uniformity.[11] The vertical non-uniformity can be due to additional implantation for threshold voltage adjustment or for punch through prevention.[12–14] On the other hand, lateral non-uniformity due to the intended pocket implantation for deep sub-micron technology or the unavoidable transient enhanced diffusion of boron impurity at the edge of the source and drain regions in n-MOSFET. Doping profiles of these two regions are modeled as Gaussian distribution.[11]

We focus on the device operation in triode mode whose energy band diagrams are shown in Fig. 2. In the reverse body biasing condition, the conduction energy band has been bended to the amount of body bias. Accordingly, X_d becomes thicker than that of null body bias condition. When positive bias is supplied to the bulk, the energy band is slightly bended because the gate-to-source voltage (V_GS) is higher than bulk-to-source voltage (V_BS). Therefore, X_d is thinner than that of reverse and null body bias conditions. The forward body bias operation can also be explained by ionization mechanism which is illustrated in Fig. 1. It means

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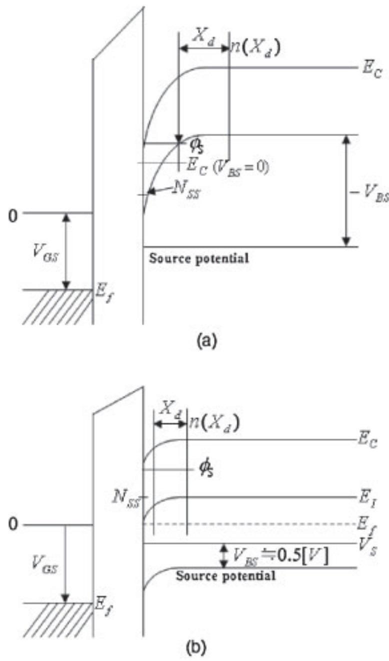

Fig. 2. Energy band diagrams of (a) reverse and (b) forward body biases.

that some percentage of channel electrons are ionized by the holes which are supplied by the bulk terminal. As a result, depletion thickness becomes smaller than that of null and reverse body biases. It is clear that X_d is dominated by concentration of channel (N_{ch}) and pocket implant (N_{pocket}).

Since the forward bias reduces X_d, V_{TH} has a strong dependency on V_{BS}, which is dominated by pocket implant.[12] The forward V_{BS} dependency of X_d can be written as a non-uniform vertical doping model in

$$X_d = \sqrt{\frac{2\varepsilon_{si}}{qN_{eff}} \cdot (\phi_S - V_{BS})}. \tag{1}$$

Here, ε_{si} is a dielectric constant of silicon, ϕ_S is the surface potential, q is an electric charge. Effective channel carrier concentration (N_{eff}) is solved by

$$N_{eff} = 2\int_0^{L_{PD}} N_{PD}\,dy + \int_{L_{PD}}^{L_{ND}} N_{NP}\,dy. \tag{2}$$

Here, N_{PD} and N_{PS} are drain and source carrier density, respectively, and N_{NP} is the bulk density. As also shown in Fig. 3, l_p is the standard deviation length of source (drain) carrier, L_{PS} and L_{PD} are the variance length of source and drain carrier, respectively. L_{NP} is the unaffected bulk area length, and L_{eff} is the effective channel length.

The drain channel density which is affected by surface state density (N_{SS}) and N_{pocket} is solved by

$$N_{PD} = \frac{\int_0^{L_{PD}} \{N_{SS} + N_{pocket} \cdot \exp[-(y/l_p)^2]\}\,dy}{L_{PD}}. \tag{3}$$

Since the vertical doping profile of drain and source regions show Gaussian distribution, statistical functions can be used as shown in Fig. 3. σ represents the standard deviation, σ^2 means the variance. Using Gaussian distribution calculation referred to Fig. 3, eq. (3) can be solved by

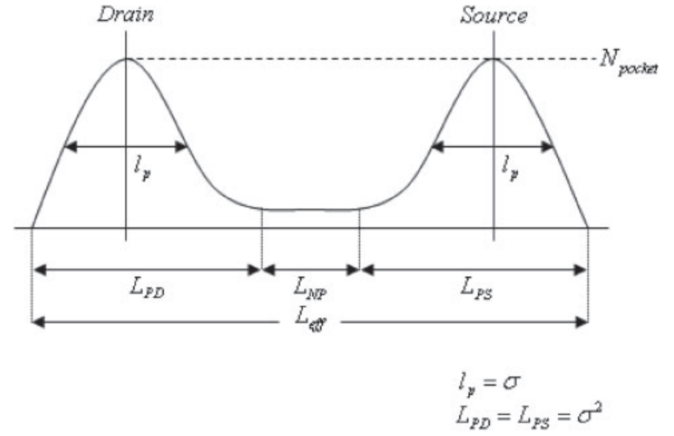

Fig. 3. Illustration of vertical non-uniform doping profile in three regions.

$$N_{PD} = \frac{\left[\frac{\sqrt{\pi}}{2} \cdot l_p \cdot N_{pocket} \cdot \mathrm{erf}\left(\frac{L_{PD}}{l_p}\right) + N_{SS} \cdot L_{PD}\right]}{L_{PD}} = \frac{\sqrt{\pi}}{2} \cdot l_p \cdot N_{pocket} \cdot \frac{l_p}{L_{PD}} \cdot \mathrm{erf}\left(\frac{L_{PD}}{l_p}\right) + N_{SS}. \tag{4}$$

Here, erf is the error function encountered in integrating the normal distribution (which is a normalized form of the Gaussian function). In the same manner, N_{PS} is represented by

$$N_{PS} = \frac{\sqrt{\pi}}{2} \cdot l_p \cdot N_{pocket} \cdot \frac{l_p}{L_{PS}} \cdot \mathrm{erf}\left(\frac{L_{PS}}{l_p}\right) + N_{SS}. \tag{5}$$

Assuming of drain and source channel as symmetrical, $L_{NP} = L_{eff} - L_{PD} - L_{PS}$, $L_{PD} = L_{PS} = l_p^2$, $N_{PD} = N_{PS}$, and $N_{NP} = N_{SS}$.

By plugging eqs. (4) and (5) into eq. (2), N_{eff} is formulated as

$$N_{eff} = \frac{2 \cdot L_{PD} \cdot N_{PD} + L_{ND} - N_{NP} \cdot L_{PD}}{L_{eff}}. \tag{6}$$

Surface potential is written as

$$\phi_S = \phi_{S0} - \Delta\phi_S. \tag{7}$$

Here, ϕ_{S0} is the surface potential at $V_{BS} = 0$ and expressed as

$$\phi_{S0} = \frac{2kT}{q} \cdot \log e\left(\frac{N_{eff}}{n_i}\right). \tag{8}$$

$\Delta\phi_S$ is written as

$$\Delta\phi_S = \phi_{DIBL} + \phi_{BF}. \tag{9}$$

ϕ_{DIBL} means the potential of drain induced barrier lowering (DIBL) and written as

$$\phi_{DIBL} = \lambda \cdot V_{DS}. \tag{10}$$

λ is the DIBL coefficient. ϕ_{BF} is the potential drop which is mentioned earlier in Figs. 1 and 2. Since ϕ_{BF} is in proportional to forward V_{BS} (V_{BF}), it is written as

$$\phi_{BF} = \lambda_B \cdot V_{BF}. \tag{11}$$

Here, λ_B is the coefficient of forward body bias.

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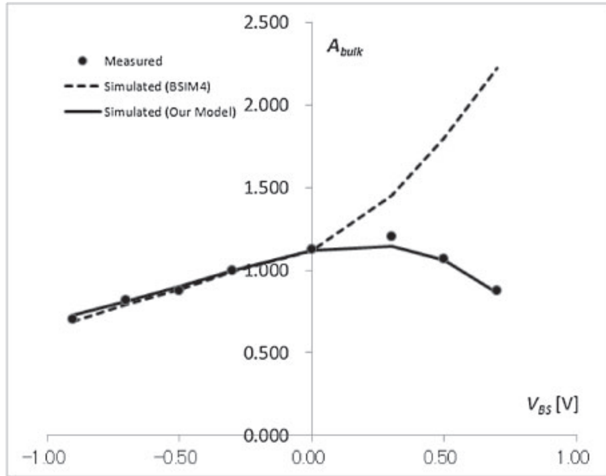

Fig. 4. Bulk charge coefficient characteristic calculations. Measured A_{bulk} was calculated with eq. (12) from I_{DS} and numerically derived v_{sat} value. Also, simulated one was calculated with model equations and extracted model parameters. Gate channel length (L) and width (W) are 60.0 nm and 10.0 µm.

Since X_{d}, N_{eff}, and ϕ_{S} are solved, threshold voltage equations can be modified with any existing nano-meter MOSFET compact models such as HiSIM2, PSP, and BSIM4.

2.2 Saturation drain current

Unlike threshold voltage equations, most MOSFET compact models use variety types of empirical formulations to represent second order effects in drain current equations. In this research BSIM4 has been adopted for implementing forward body biasing effects.

A coefficient of bulk charge effect (A_{bulk}) which is a part of the saturation drain current (I_{DS}) in eq. (12) of BSIM4[7] represents body biasing effects as shown in eq. (13):

$$I_{\mathrm{DS}} = WC_{\mathrm{ox}}(V_{\mathrm{gst}} - A_{\mathrm{bulk}}V_{\mathrm{dsat}})v_{\mathrm{sat}}. \tag{12}$$

$$A_{\mathrm{bulk}} = [1 + F_{\mathrm{dope}}(F_{\mathrm{length}} + F_{\mathrm{width}})] \cdot \frac{1}{1 + K_{\mathrm{eta}} \cdot V_{\mathrm{BS}}}. \tag{13}$$

Here v_{sat} is the velocity saturation.

A_{bulk} was calculated and plotted from measured and simulated data using model equations in Fig. 4. The target n-MOSFET device, whose drawn channel length and width are 60 nm and 10 µm, respectively, for the measurement was selected from MOSFET TEGs using 60 nm CMOS technology. The V_{BS} dependencies of A_{bulk} in eq. (13) can only express proportionality relation in BSIM4 that needs to be modified to represent forward V_{BS} case. We empirically developed eq. (14) to express the reduction of A_{bulk} at the forward body biases.

$$A_{\mathrm{bulk}} = [1 + F_{\mathrm{dope}}(F_{\mathrm{length}} + F_{\mathrm{width}})] \times \frac{1}{1 + (K_{\mathrm{eta}} + K_{\mathrm{etavb}} \cdot e^{V_{\mathrm{BS}}}) \cdot V_{\mathrm{BS}}}. \tag{14}$$

Here, W, C_{ox}, V_{gst}, and V_{dsat}, are the channel width, oxide capacitance, V_{GS} minus V_{TH}, and saturation voltage, respectively. F_{dope}, F_{length}, and F_{width} are the functions of non-uniform doping, channel length, and channel width dependencies, respectively.[7] K_{etavb} is the newly added parameter to represent reverse-to-forward V_{BS} dependencies to work with K_{eta}, which is a fitting parameter in BSIM4 model.

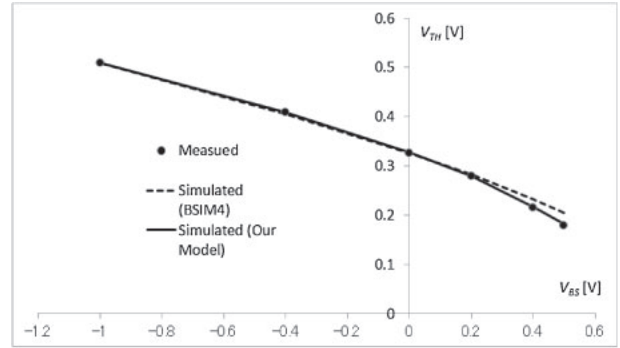

Fig. 5. V_{TH}, dependencies on reverse-to-forward body biases. Here, V_{TH} was adopted by the V_{GS} at the I_{DS} of 100 nA × W/L. Also, $L = 1.0$ µm and $W = 10.0$ µm.

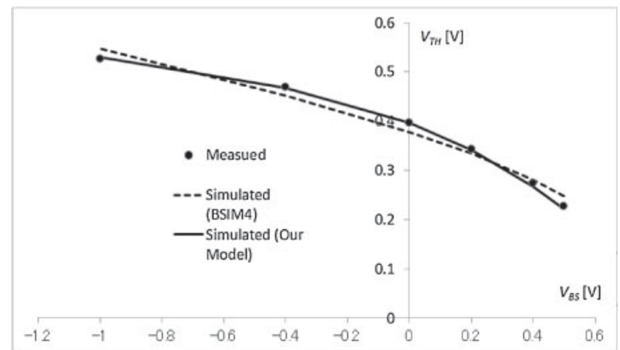

Fig. 6. V_{TH}, dependencies on reverse-to-forward body biases. Here, V_{TH} was adopted by the V_{GS} at the I_{DS} of 100 nA × W/L. Also, $L = 60$ nm and $W = 10.0$ µm.

3. Experiment

The proposed model was implemented into SPICE3f5 and all the parameters were extracted from measured data. After the process instance parameters (physical dimensions and doping profiles) are defined, the model parameter extraction procedure consists of three simple steps. First, we extracted and optimized original BSIM4 DC parameters using a standard procedure which is written in BSIM4 manual[7] or using any advanced commercial software such as MoDeCH Extractor.[15] Secondly, L_{PD} and λ_{B} were optimized by using V_{TH} vs V_{BS} measurement shown in Fig. 5. Finally, K_{etavb} and K_{eta} were optimized by using I_{DS} vs V_{DS} measurement shown in Fig. 8.

Figures 5 and 6 show V_{TH} vs V_{BS} characteristic of measurement and simulations used by current BSIM4 and our modified BSIM4 models. It shows that the simulated V_{TH} by current BSIM4 has some differences under the forward bias condition, in contrast, our model agreed with the measured V_{TH} in sufficient accuracy. Since our threshold voltage equations include short channel effects, larger improvements of the forward V_{BS} dependencies are presented in Fig. 6.

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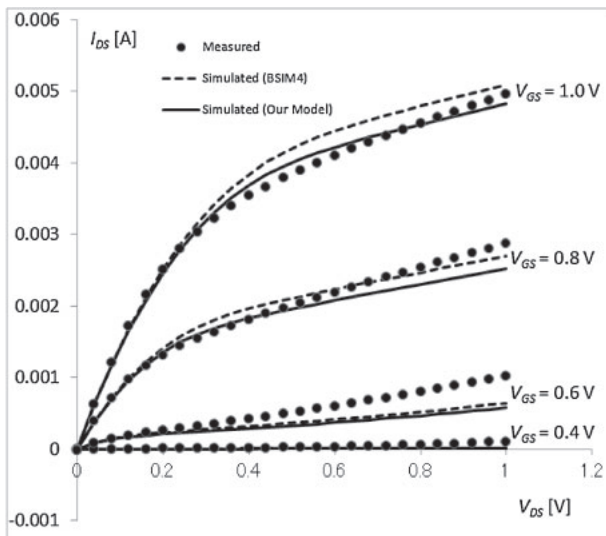

Fig. 7. Characteristic of measured and simulated I_{DS} vs V_{DS} at $V_{BS} = -1.0$ V (reverse biased). L and W are 60.0 nm and 10.0 μm.

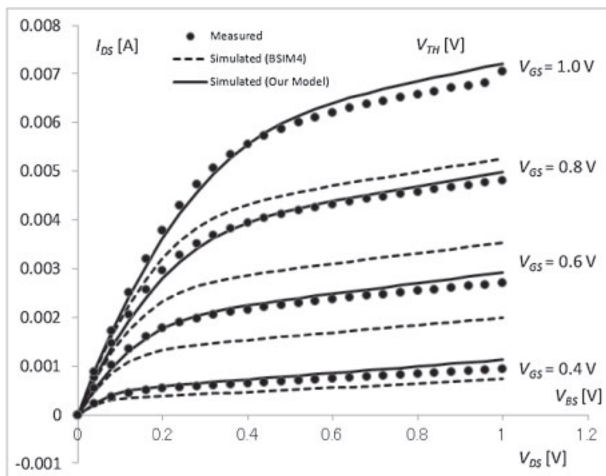

Fig. 8. Characteristic of measured and simulated I_{DS} vs V_{DS} at $V_{BS} = 0.5$ V (forward biased). L and W are 60.0 nm and 10.0 μm.

Figure 7 shows I_{DS} vs drain-to-source voltage (V_{DS}) with some V_{GS} voltages under the reverse bias condition for measured and simulated current by BSIM4 and our proposed models. Both of simulated currents show equivalent accuracies. Figure 8 shows I_{DS} vs V_{DS} with some V_{GS} voltages under the forward bias condition. The simulated current by BSIM4 is approximately 35% lower than that of measured value, particularly in a high V_{GS} region. The total rms error current was about 50%. However, the simulated current by proposed model agrees with measured data in sufficient accuracy which was about 3% rms error.

The forward bias technique needs to be used for low voltage operations such as 0.75 or 0.5 V, to reduce the threshold voltage in more scaled devices whose electrical fields become higher.

4. Conclusions

The forward body bias technique will be important for low voltage operation such as 0.5 V, however current MOSFET compact models, such as BSIM4, do not have sufficient accuracy in this body bias operation. We first formulate X_d which is dominant to determine the V_{TH} using vertical and horizontal doping profiles. Next the velocity saturation dependencies on reverse to forward body biases that was dominated by body charge coefficient in BSIM4 approach were analyzed and modeled. The total rms error of the simulated current by proposed model agrees with measured data in sufficient accuracy which was about 3%, whereas the error with BSIM4 was about 50%. Thus we proposed the model and equations to implement in BSIM4 version 4.6 as an instance.

The proposed model improved the forward body biased drain current simulation accuracies without sucrificing simulation accuracies of the null and reverse biased drain current in 60 nm n-MOSFET process devices.

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