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Pursuing Excellence

Essence and Technology Direction of ADC Design

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Outline

- **Overview of ADCs**
- **OpAmp based ADC design: Pipeline ADC**
- **Comparator based ADC design : SAR ADCs**
- **Flash ADCs**
- **Summary**

ADC performance and data rate

Data rate is proportional to the product of f_s and N

Conversion frequency is determined by signal bandwidth.

$$BW < \frac{f_s}{2}$$

$$D_{rate} \approx N f_s$$

Shannon's theory to determine the communication capacity

$$C = BW \log_2\left(1 + \frac{P_S}{P_N}\right)$$

SNR of ADC is

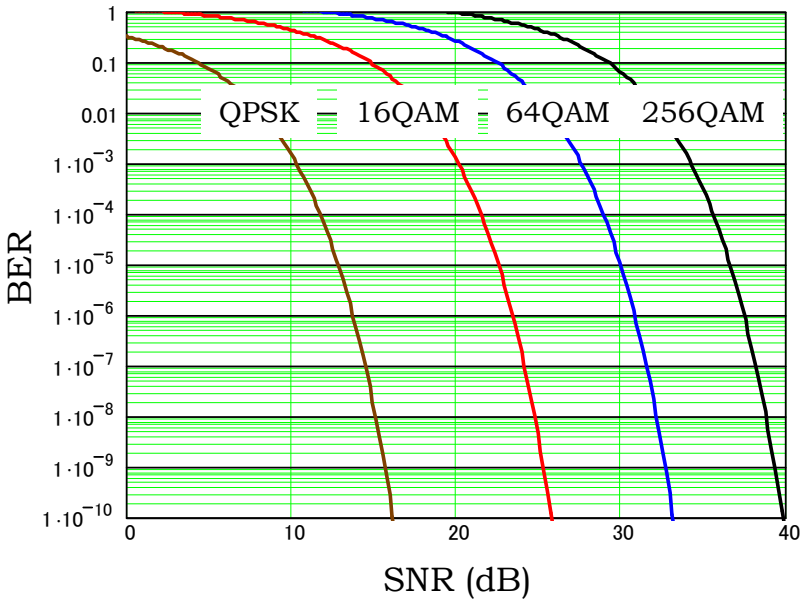
$$\left.\frac{P_S}{P_N}\right|_{ADC} = 1.5 \cdot 2^{2N}$$

Therefore

$$C \approx N f_s$$

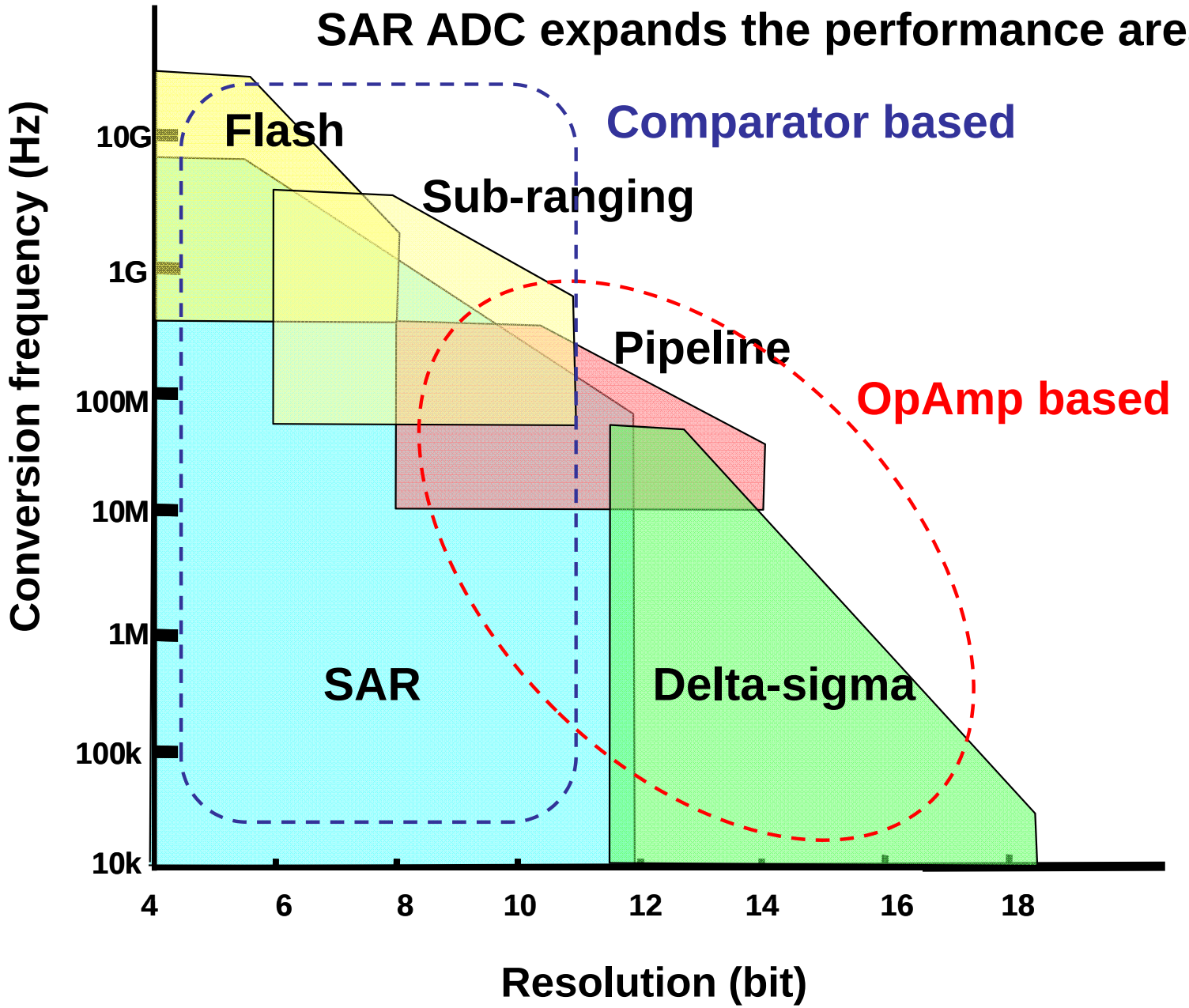
f_s: Sampling frequency
N: Resolution

Higher data-rate can be realized by higher multi-level modulation. It result in increase of ADC resolution.



Performance and architectures of ADCs

ADC has a suitable performance domain.



Strategy of energy efficient ADC design

Reducing static power

Resistor DAC → Capacitor DAC

OpAmp based → Dynamic comparator based

Reducing capacitance

$$E_d \approx CV_{DD}^2$$

# of CMP Flash → SAR

$$\Delta V_T \propto \frac{1}{\sqrt{C_G}}$$

TR size Large TR → Small TR with compensation

$$\overline{V_n} \propto \frac{1}{\sqrt{C}}$$

Noise Use complementally ckt.

Clock Use self clocking

Reducing voltage

Effective to digital gates

Use forward or adaptive body biasing

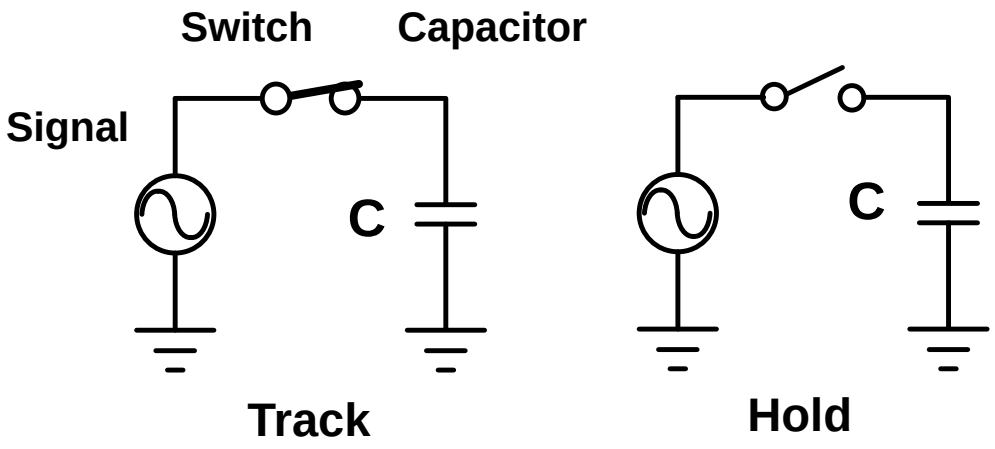
Fundamental Energy of sampling circuit

Fundamental energy of sampling is often used.

$$E_s = 24kT2^{2N}$$

However this neglects the power for comparison.

Sampling circuit



Electrical energy=Thermal energy

$$\frac{1}{2}CV_n^2 = \frac{1}{2}kT \quad \therefore \quad V_n^2 = \frac{kT}{C}$$

Quantization voltage

$$V_{qn} = \frac{V_{FS}}{2^N}$$

Quantization noise power

$$P_{qn} = \frac{V_{qn}^2}{12} = \frac{V_{FS}^2}{12 \cdot 2^{2N}}$$

Noise balance $V_n^2 = P_{qn}$

Capacitance $C = 12kT\frac{2^{2N}}{V_{FS}^2}$

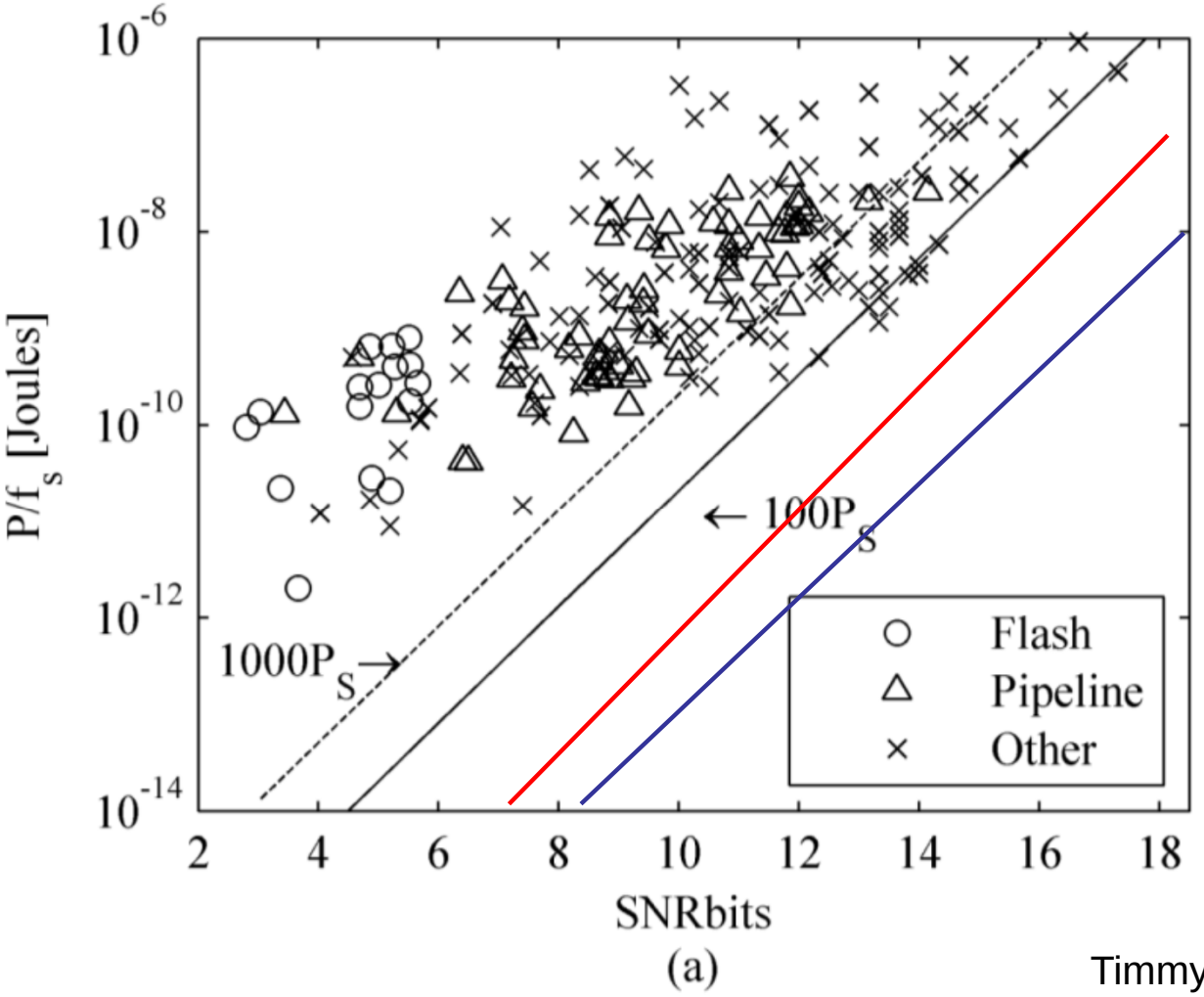
P_d of sampling circuit

$$E_d = 2CV_{FS}^2 = 24kT2^{2N}$$

Energy consumption of ADC

Consumed energy of ADC is mainly determined by the resolution.

Energy of ADC is reaching 100x of the fundamental sampling energy, and 10x of the fundamental ADC energy consumption.



Conventional fundamental sampling energy

$$E_s = 24kT_s 2^{2N}$$

$$E_s = 2^{2N} \times 10^{-19}$$

Fundamental ADC conversion energy involving energy consumption of comparator

$$E_{ADC} \approx N \cdot E_s$$

$$E_{ADC} = N \times 2^{2N} \times 10^{-19}$$

Timmy Sundstrom, PhD thesis, Linkoping 2011.

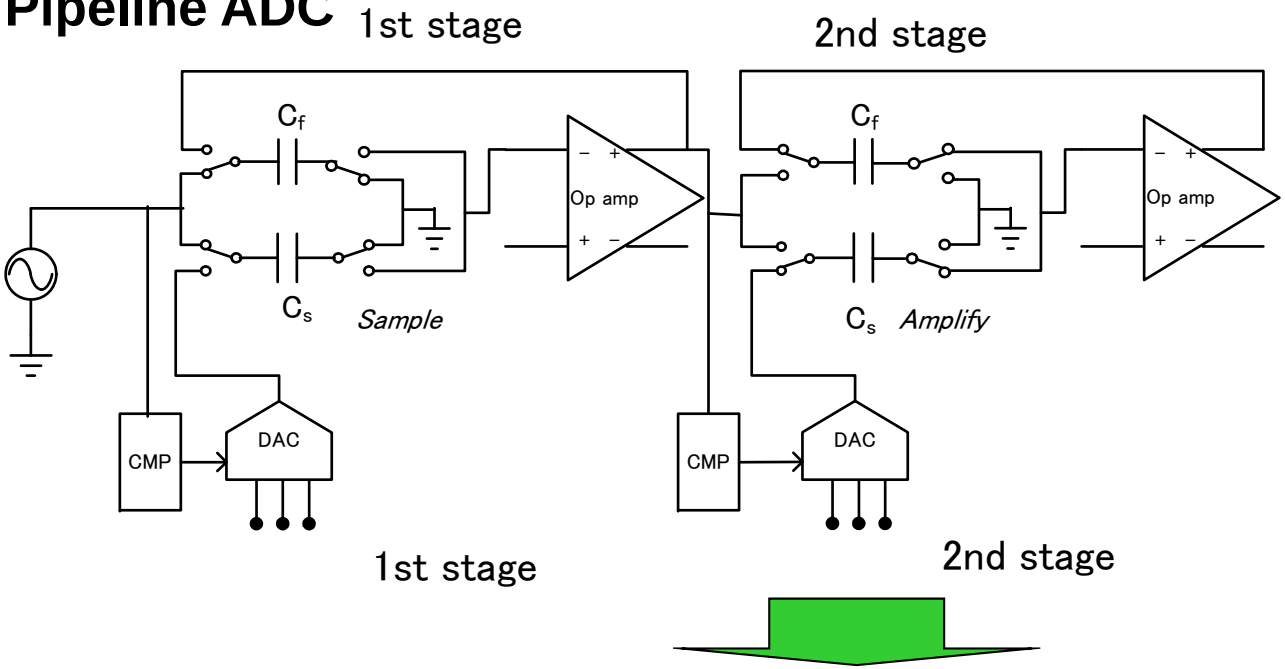
OpAmp based ADC design

Pipeline ADC

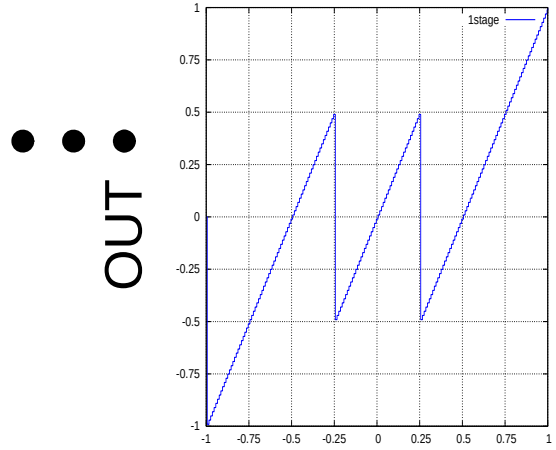
Mega-technology trend of ADCs

Major conversion scheme is now changing from pipeline to SAR.

Pipeline ADC

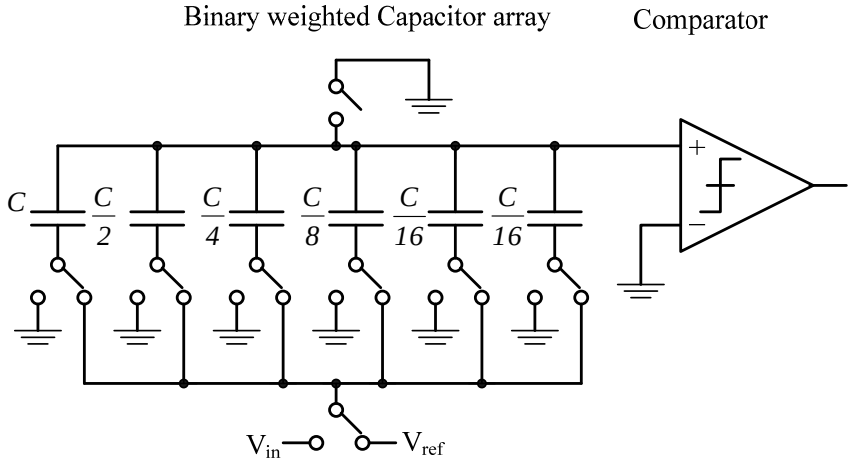


I/O transfer curve of the stage



1st stage 2nd stage

SAR ADC



OpAmp based design

Consumes static power

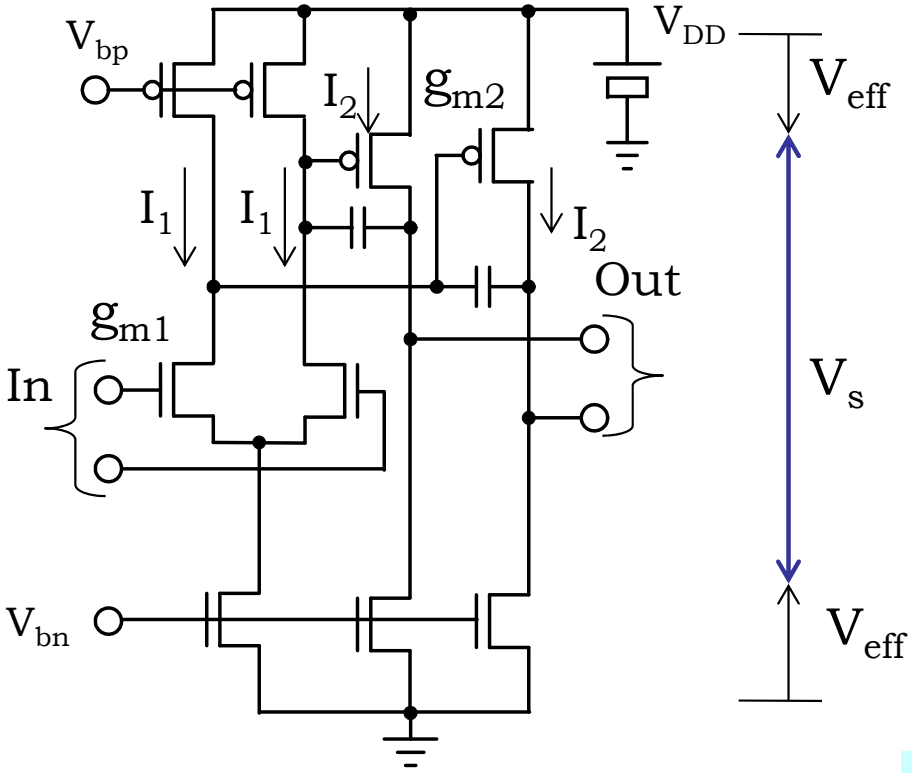
Comparator based design

No static power

Low voltage OpAmp: Headroom and Pd

Two stage cascade OpAmp can realize low voltage operation.
However, the output voltage swing becomes lower at low voltage operation.

$$V_{s\_pp} = 2\left(V_{DD} - 2V_{eff}\right)$$



Two stage OpAmp

$$V_{eff} \equiv V_{GS} - V_T$$
$$V_{eff} \approx 0.15V$$

$$GBW \approx \frac{g_{m2}}{4\pi C_0} = Nf_c$$

$$\therefore g_{m2} = \frac{2I_2}{V_{eff}} = 4\pi C_0 N f_c \quad C_0 \geq \left(2 + \frac{\gamma n}{\beta}\right)\frac{kT}{V_{n\_th}^2}$$

$$\therefore I_2 = 2\pi C_0 N f_c V_{eff} = \frac{2\pi N f_c V_{eff} kT}{V_{n\_th}^2}\left(2 + \frac{\gamma n}{\beta}\right)$$

$$g_{m2} = 4g_{m1} \quad \therefore I_2 = 4I_1$$

n=4

$$I_{tot} = \frac{5}{2} I_2$$

$$P_{da} = V_{DD} \cdot I_{tot} = 5\pi V_{DD} \frac{N f_c V_{eff} kT}{V_{n\_th}^2}\left(2 + \frac{\gamma n}{\beta}\right)$$

Total Pd of ADC

$$P_{dpipe} = 2P_{damp} = 10\pi V_{DD} \frac{N f_c V_{eff} kT}{V_{n\_th}^2}\left(2 + \frac{\gamma n}{\beta}\right)$$

FoM vs. V_{DD}

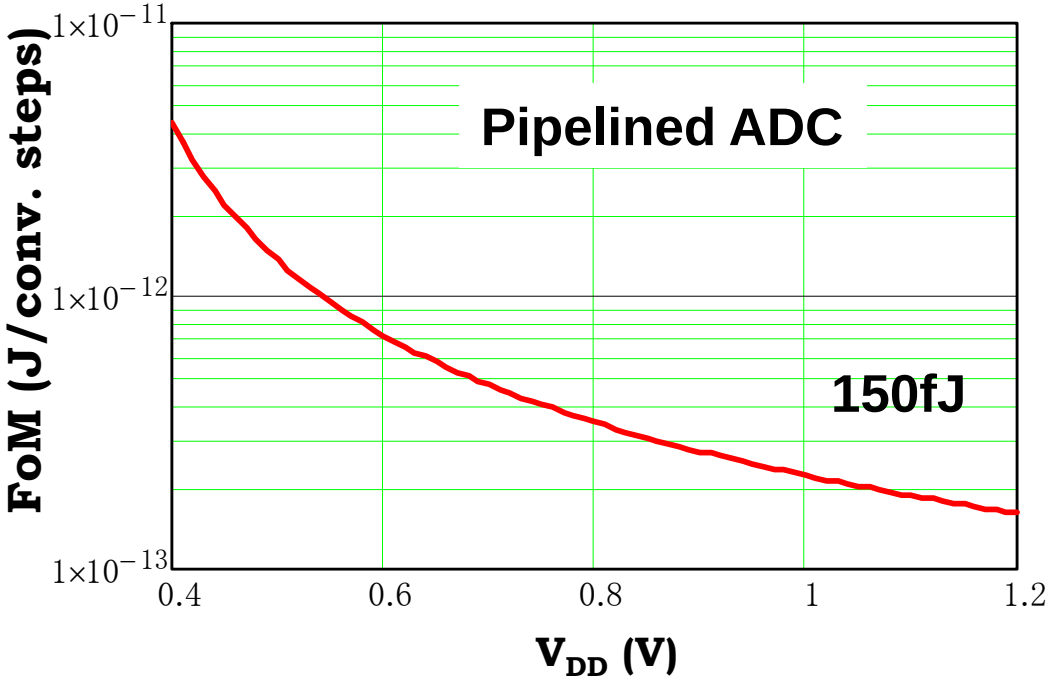
An OpAmp based ADC consumes large conversion energy

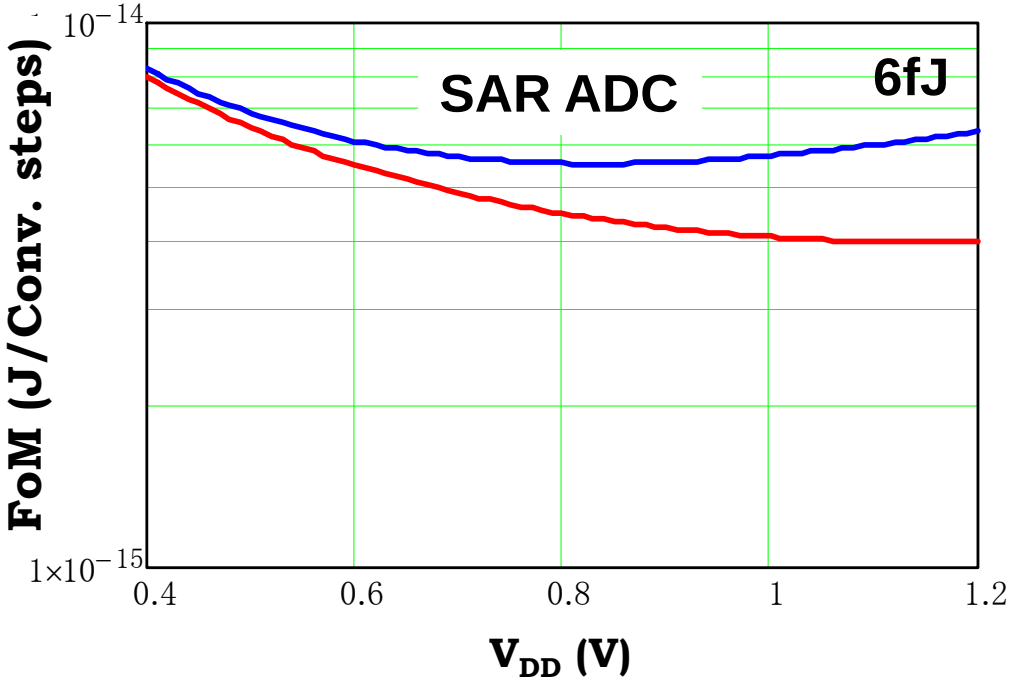
$$P_d = I_D V_{DD} \propto C_0 f_c V_{eff} V_{DD} \propto \frac{f_c \cdot T \cdot SNRV_{eff} V_{DD}}{\left(V_{DD} - 2V_{eff}\right)^2}$$

$$FoM(J) = \frac{P_d}{f_c \times 2^{ENOB}} = \frac{P_d \times 2^{\Delta ENOB}}{f_c \times 2^N}$$

$$f_c \propto GBW \propto \frac{g_m}{C_0} \approx \frac{2I_D}{C_0 V_{eff}}$$

12bit ADC





Comparator based ADC design

: SAR ADC

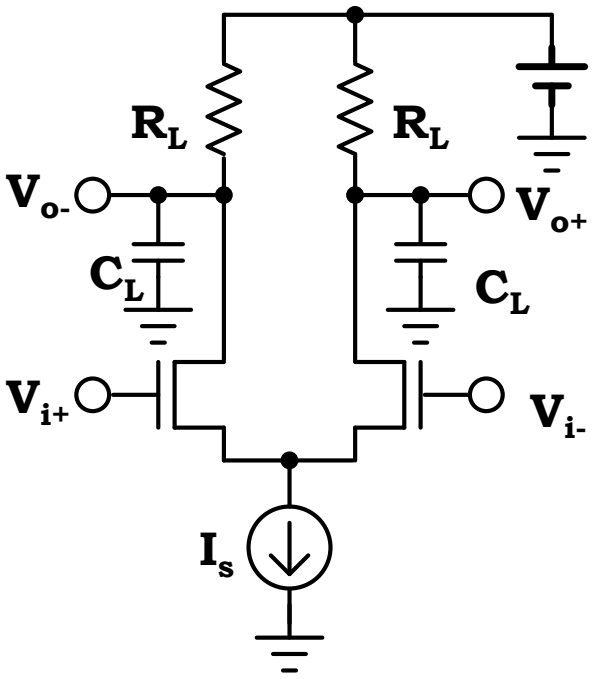
Basic idea for low energy analog design

Conventional analog circuit consumes larger energy.

Dynamic circuits doesn't consume larger energy.

CMOS: Consumed energy is independent of the delay time.

CML, OpAmp

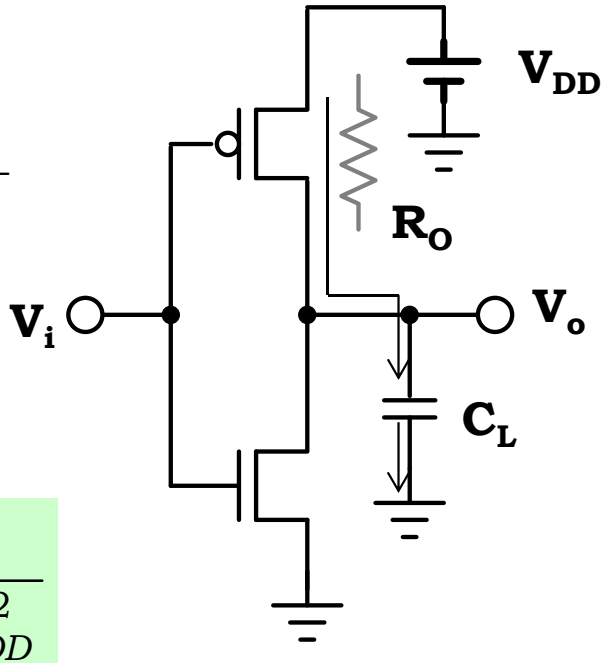


$$f_{togle} \propto \frac{I_s}{V_{DD} C_L}$$

$$P_d = V_{DD} I_s$$

$$f_{togle} \propto \frac{P_d}{C_L V_{DD}^2}$$

CMOS



$$f_{togle} \propto \frac{1}{T_r} \propto \frac{1}{R_o C_L}$$

$$P_d = f E_d = \frac{1}{2} f C_L V_{DD}^2$$

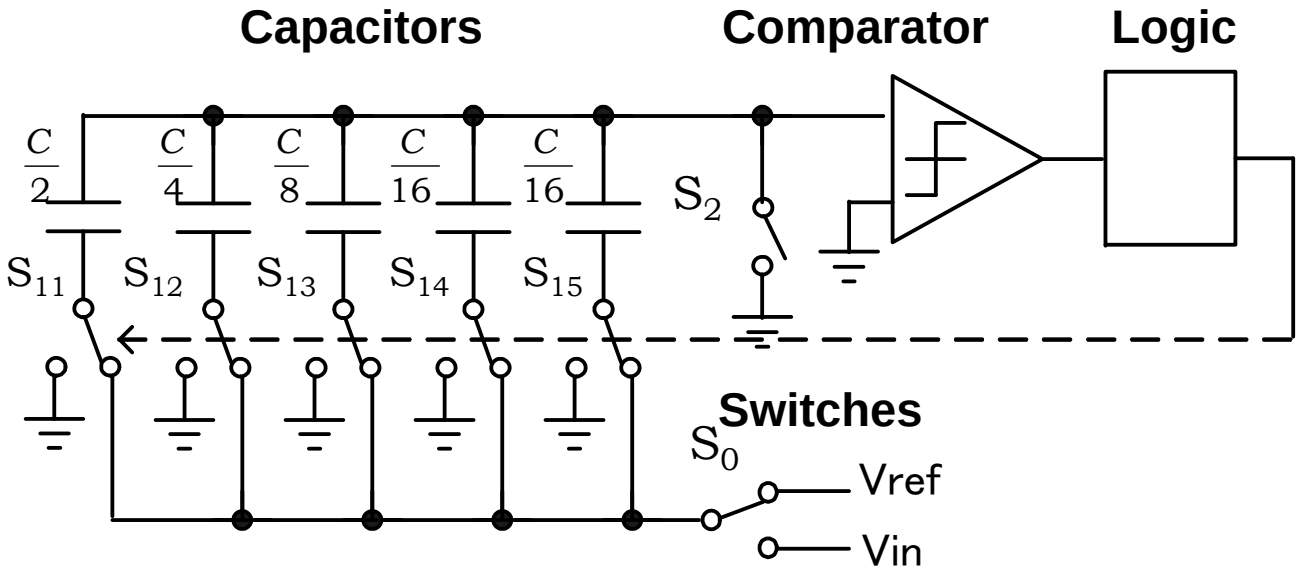
$$E_d = \frac{1}{2} C_L V_{DD}^2$$

$$f_{togle} \propto \frac{1}{R_o C_L}$$

SAR ADC

SAR can be designed to consume no static power.

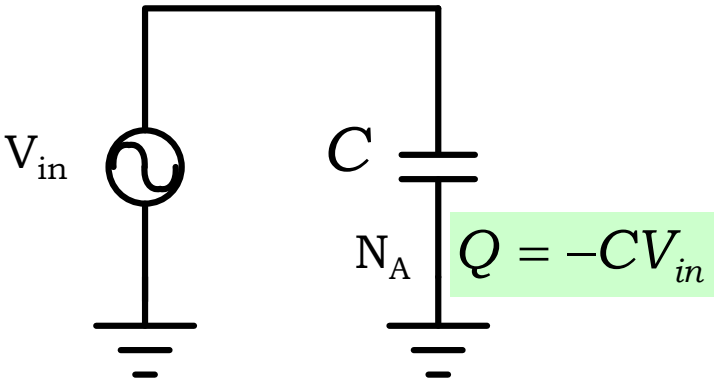
SAR can realize larger signal swing compared with pipeline ADC.



Not OpAmp based, but comparator based

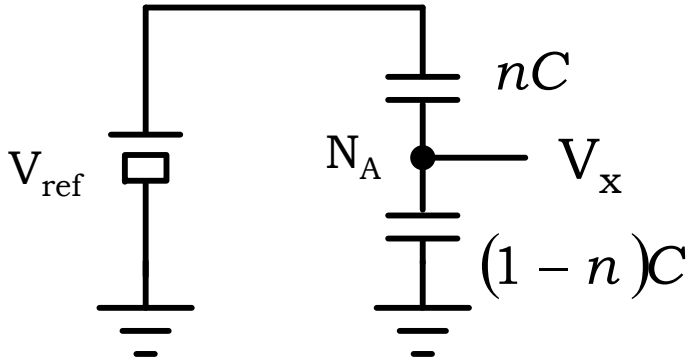
No resistors
No static current !
Potentially full swing

Sample



$Q = -CV_{in}$

Generating subtracted signal



$0 < n < 1$

$$E \approx \frac{1}{2} C V_{ref}^2$$

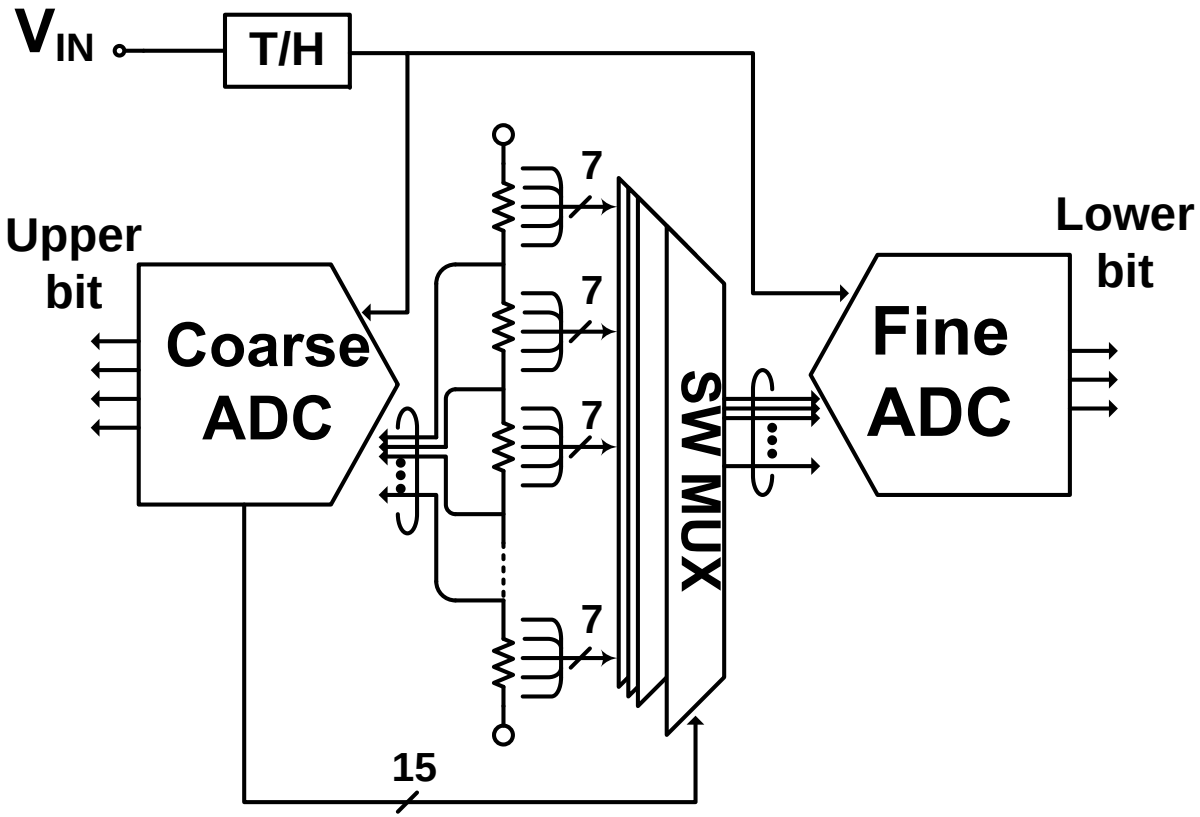
$$V_x = -\left(V_{sig} - n \cdot V_{ref}\right)$$

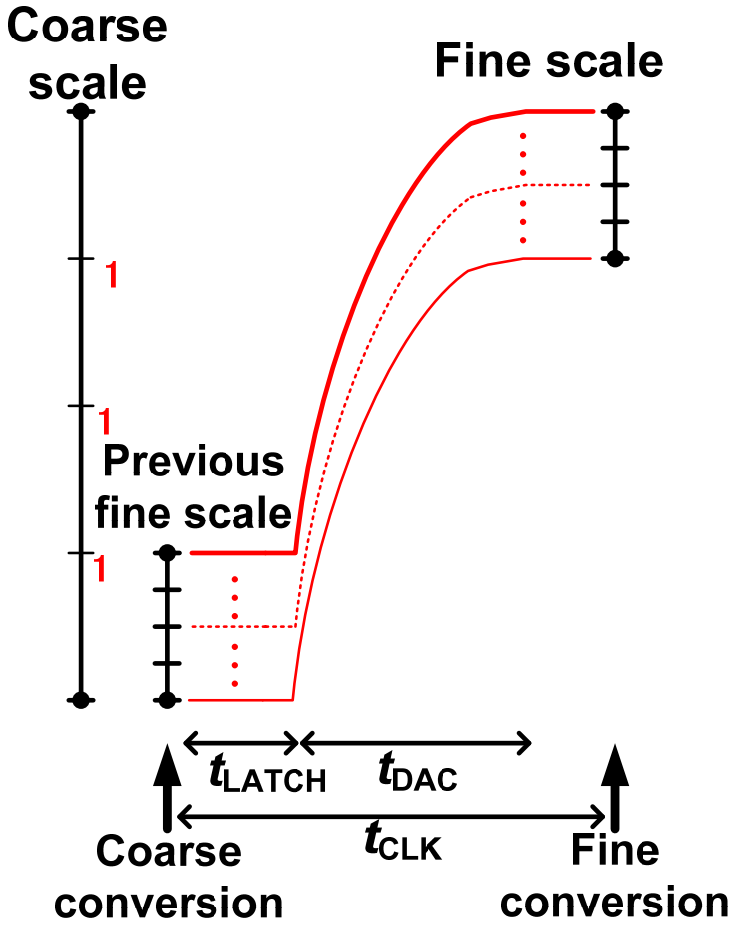
Issue of resistive DAC to generate V_{REF}

Resistive DAC consumes static power and has a serious tradeoff between Pd and speed.

$$\tau_{ref\,\max} \approx \left\{\frac{R}{4} + R_{on}\right\} C_{pr} = \left\{\frac{V_{ref}}{4I_{ref}} + R_{on}\right\} C_{pr}$$

$$\tau \propto \frac{1}{I}$$





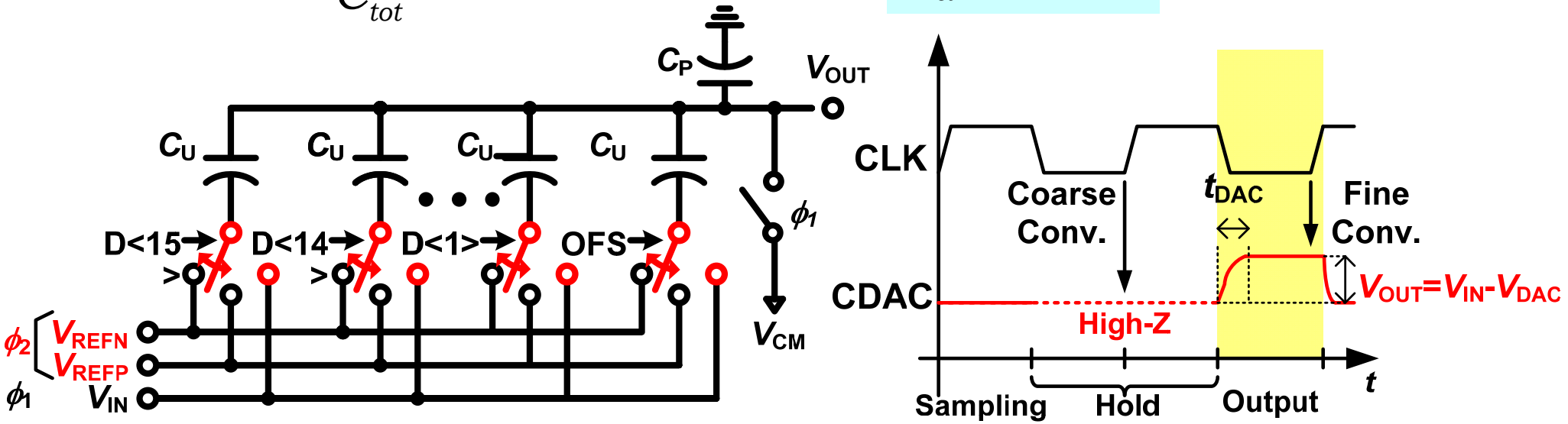
Advantage of capacitive DAC to generate V_{REF}

Capacitor DAC doesn't consume static power and has no trade off between Pd and speed.

$$V_{out} = \frac{-1}{1+\frac{C_p}{C_{tot}}}\left(V_{IN} - n \cdot V_{REF}\right)$$

$$\tau \approx R_{on}C$$

$$E_d \approx CV_{DD}^2$$



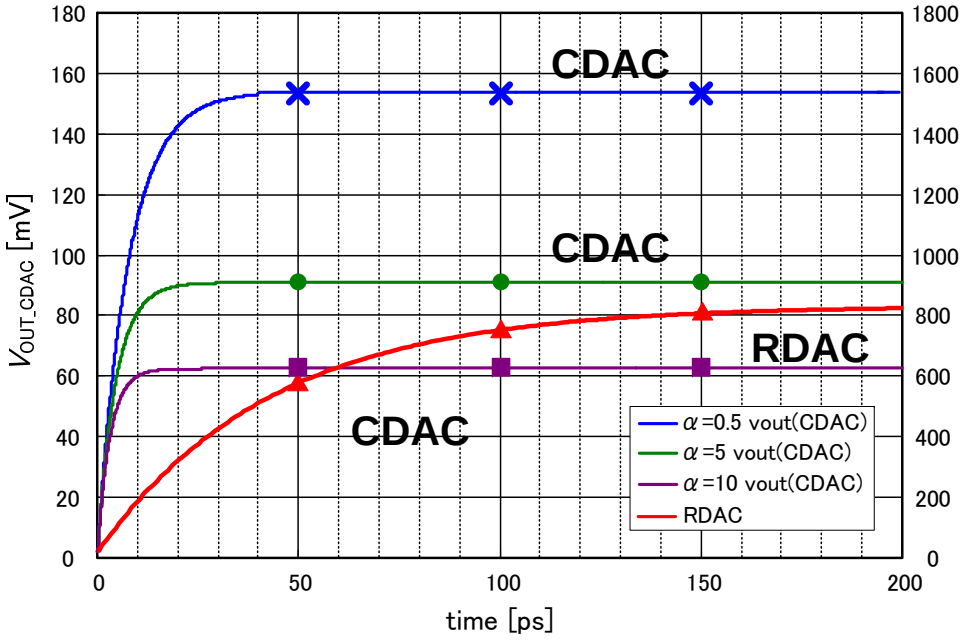
Operating as S/H circuit

- **No static power consumption (360μW@1GHz)**
- **Smaller C_u realize faster settling time**

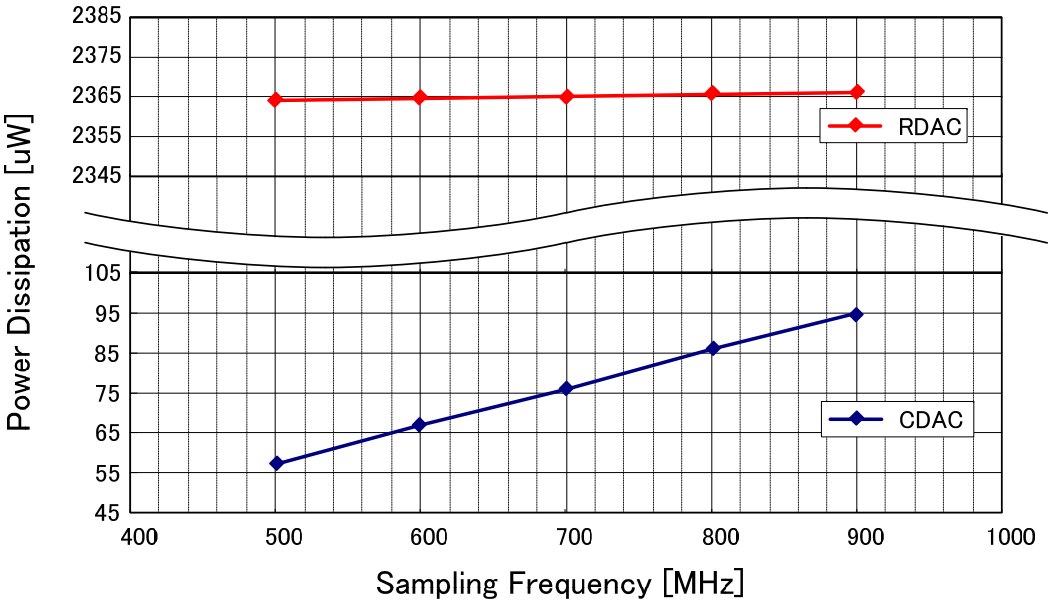
  (t_{DAC}= 3.4 $r_{on}C_U$ < 80ps @ r_{ON} = 1kΩ, C_U= 15fF)

Settling time and power

CDAC realizes faster settling time to RDAC with low power consumption.



Time response

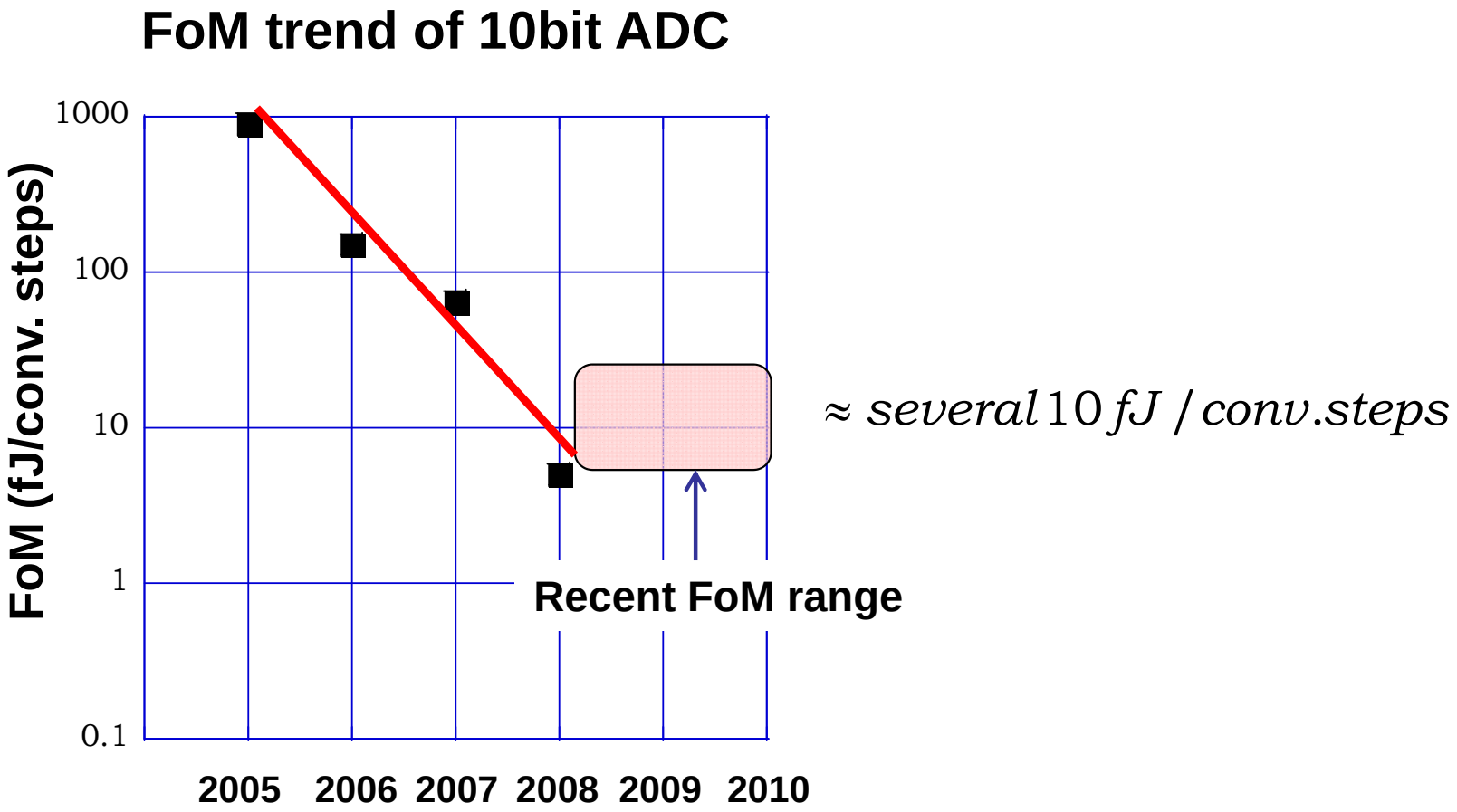


Power dissipation

Performance overview of SAR ADCs

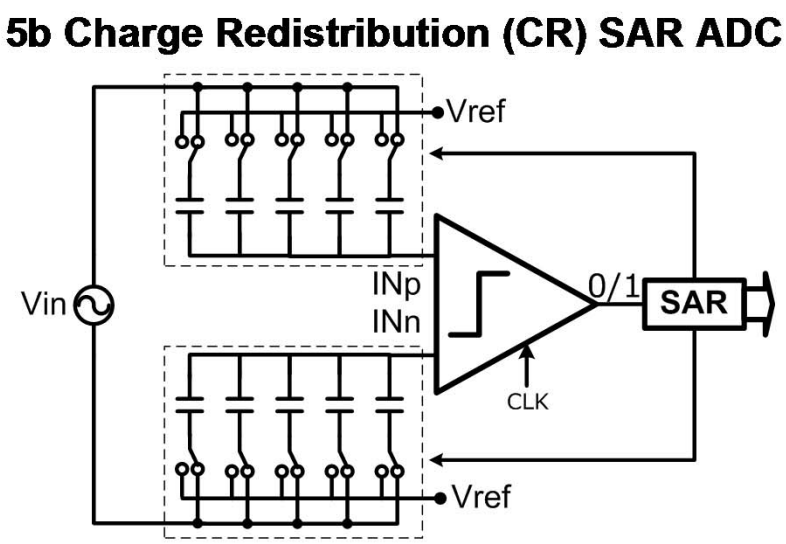
FoM has lowered rapidly due to the progress of SAR ADC.

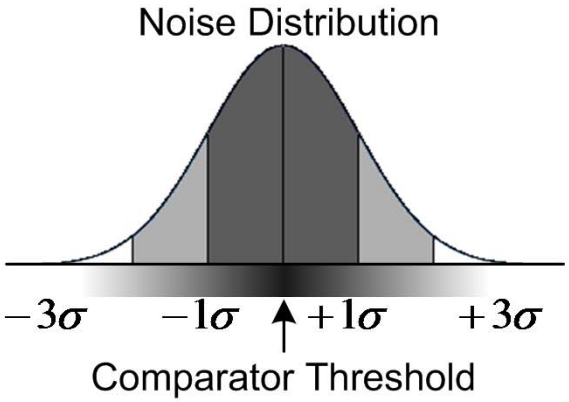
1/200 during three years.

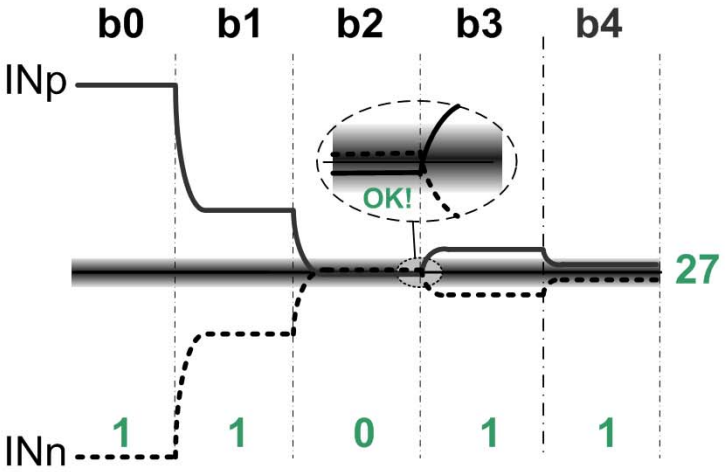


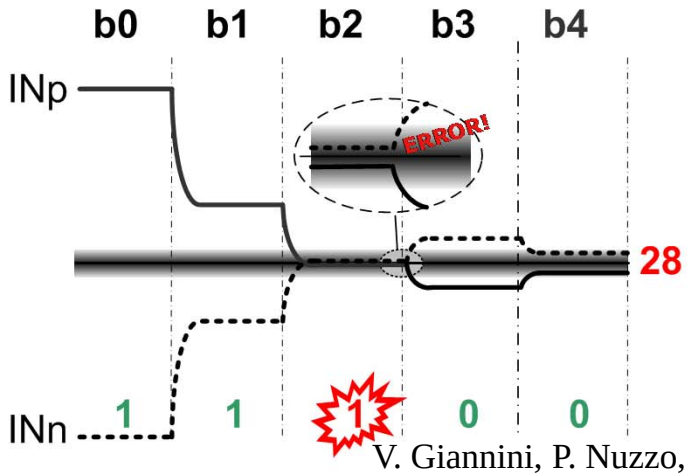
Issue of comparator for SAR ADCs

A comparator has noise and this results in conversion error.







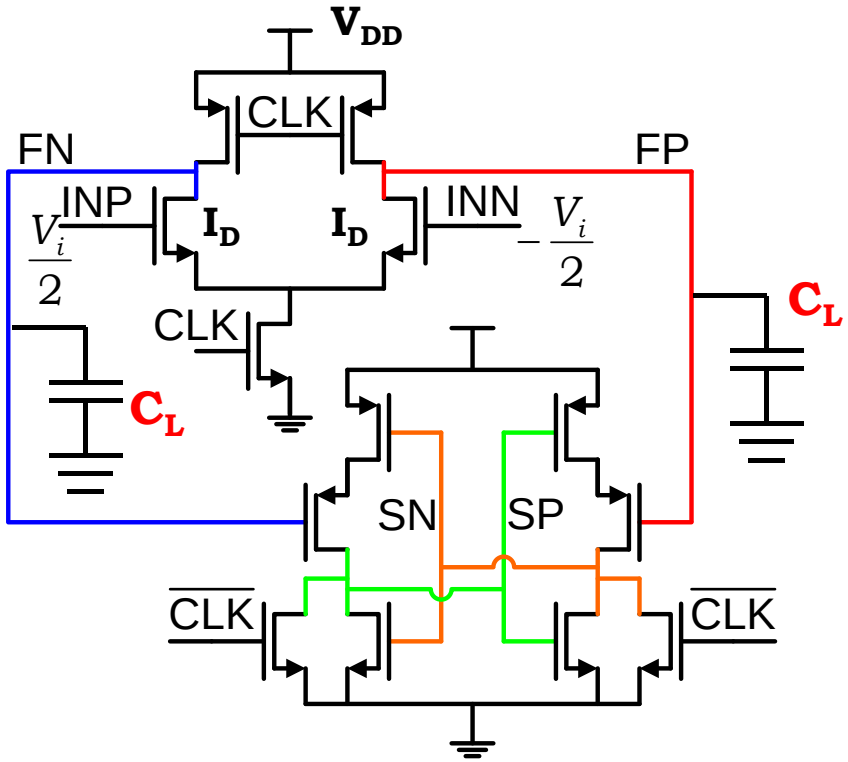


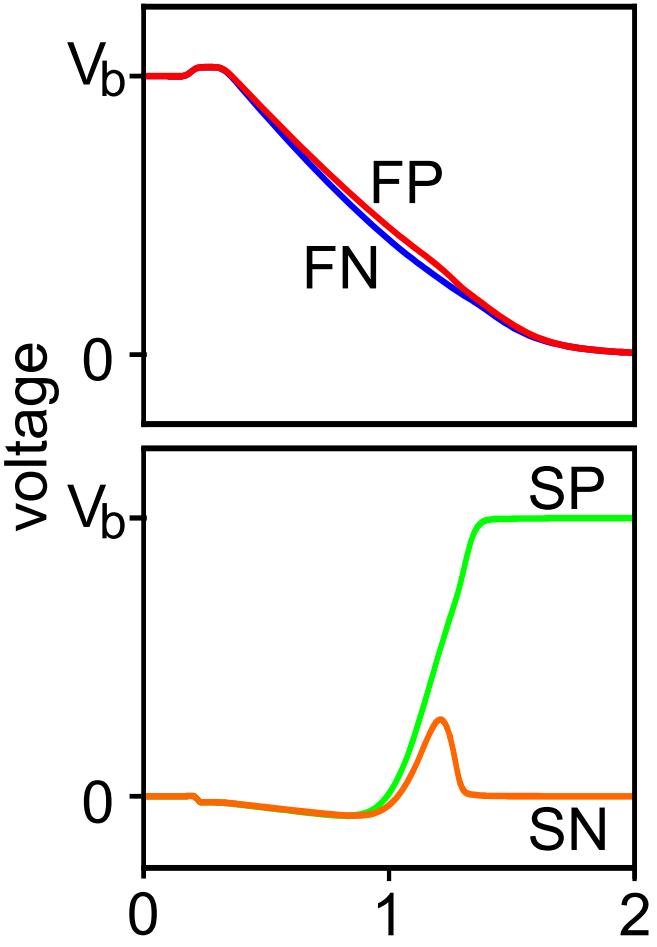
V. Giannini, P. Nuzzo, V. Chironi, A. Baschirotto, G. van der Plas, and J. Craninckx, “An 820uW 9b 40MS/s Noise Tolerant Dynamic-SAR ADC in 90nm Digital CMOS,” IEEE ISSCC 2008, Dig. of Tech. Papers, pp.238-239, Feb. 2008.

Dynamic comparator

A dynamic comparator is widely used to reduce static power.

The difference in input voltages causes a difference in discharging speed.

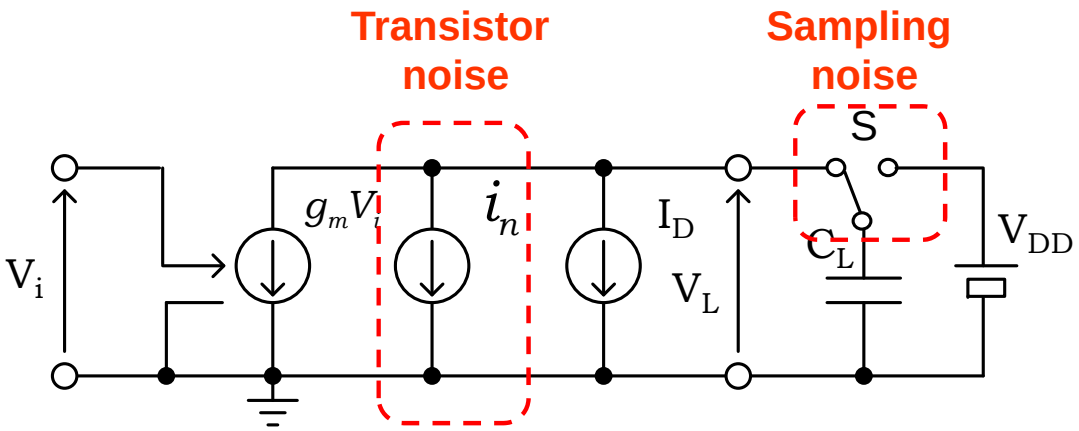




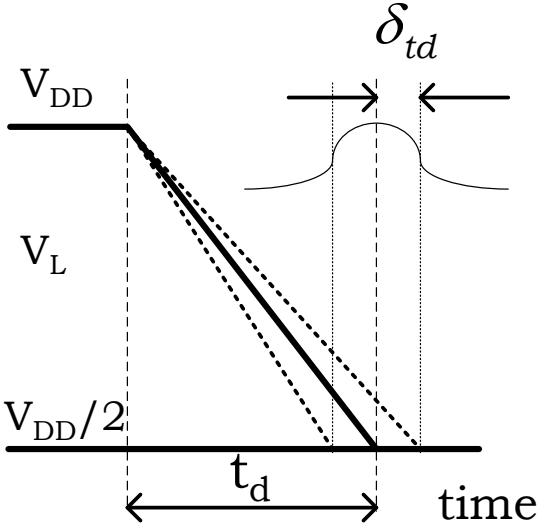
D. Schinkel, E. Mensink, E. Klumperink, Ed Van Tuijl, B. Nauta,

"A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup-Hold Time," ISSCC Dig. of Tech. Papers, pp.314-315, Feb., 2007.

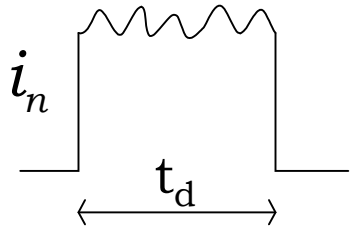
Deriving noise equation



Equivalent circuit



Voltage and timing



TR noise

1) Sampling noise of Switch

$$\left\langle v_n^2 \right\rangle = \frac{kT}{C_L}, \quad \delta_{t_d}^2 = \frac{\left\langle v_n^2 \right\rangle}{\left(\frac{I_D}{C_L}\right)^2} = \frac{kTC_L}{I_D^2}$$

2) Transistor noise

$$\delta t = \frac{C_L}{I_D}\delta v$$

Noise voltage of output by current noise

$$v_n = \frac{1}{C_L}\int_0^{t_d} i_n dt \qquad \delta_{t_d}^2 = \frac{C_L^2}{I_D^2}\delta_{vn}^2 = \frac{1}{I_D^2}\left\langle \left(\int_0^{t_d} i_n dt\right)^2 \right\rangle$$

$$\delta_{t_d}^2 = \frac{kTC_L}{I_{ds}^2}\left(\alpha\gamma\frac{V_{dd}}{V_{eff}} + 1\right)$$

$$\delta V_{in}^2 = \left(\frac{V_{eff}}{a}\frac{\delta_{td}}{t_d}\right)^2 = \frac{4kTV_{eff}^2}{a^2 C_L V_{dd}^2}\left(a\gamma\frac{V_{dd}}{V_{eff}} + 1\right)$$

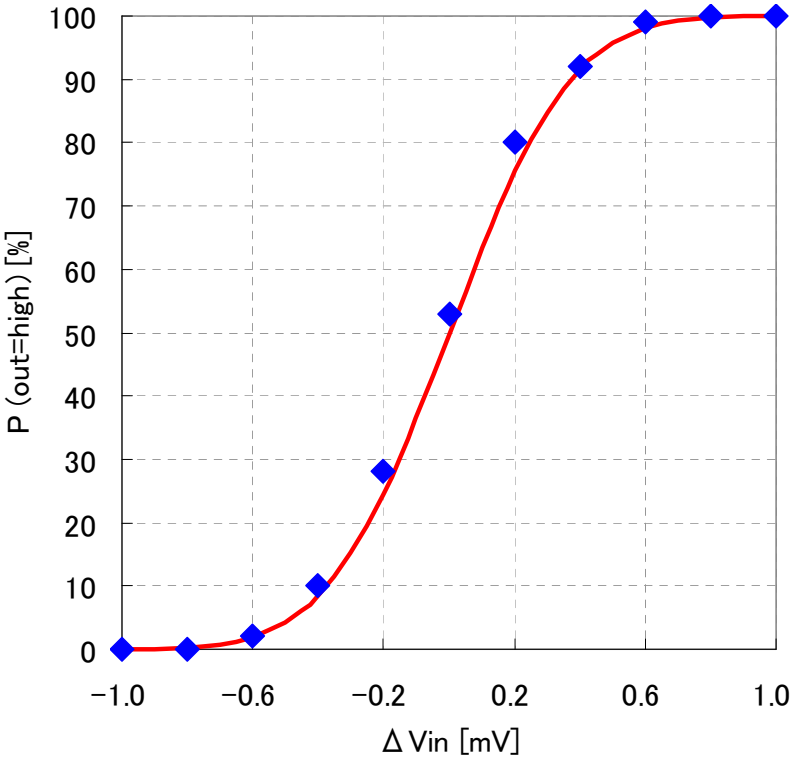
A. Matsuzawa," IEEE 8th International Conference on ASIC(ASICON), pp. 218-221, Oct. 2009.

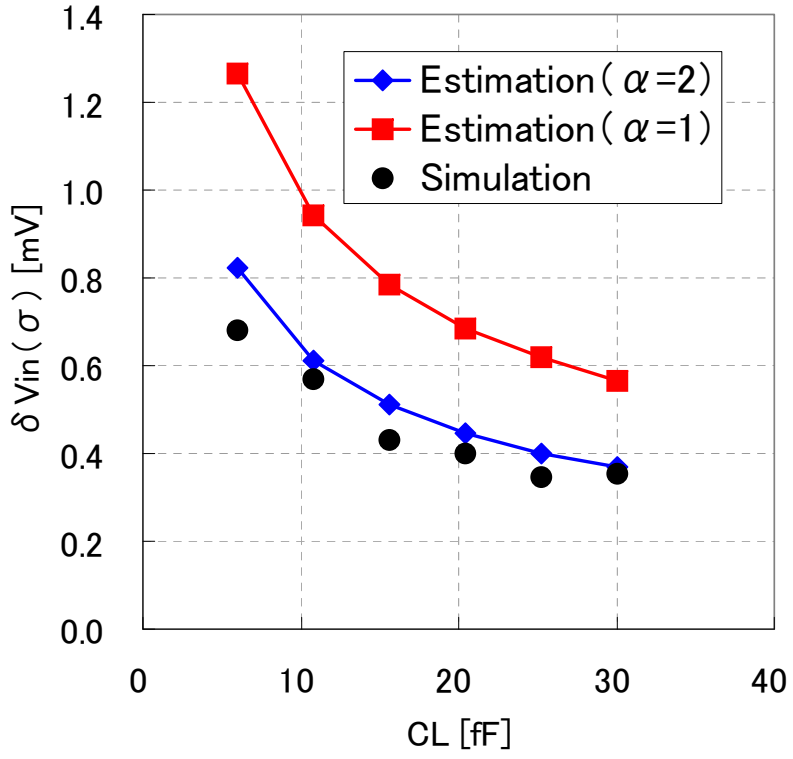
Match with noise simulation

The derived equation has a good match with simulation.

$$\delta V_{in}^2 = \frac{4kTV_{eff}^2}{a^2 C_L V_{dd}^2}\left(a\gamma\frac{V_{dd}}{V_{eff}}+1\right)$$

Noise in comparator

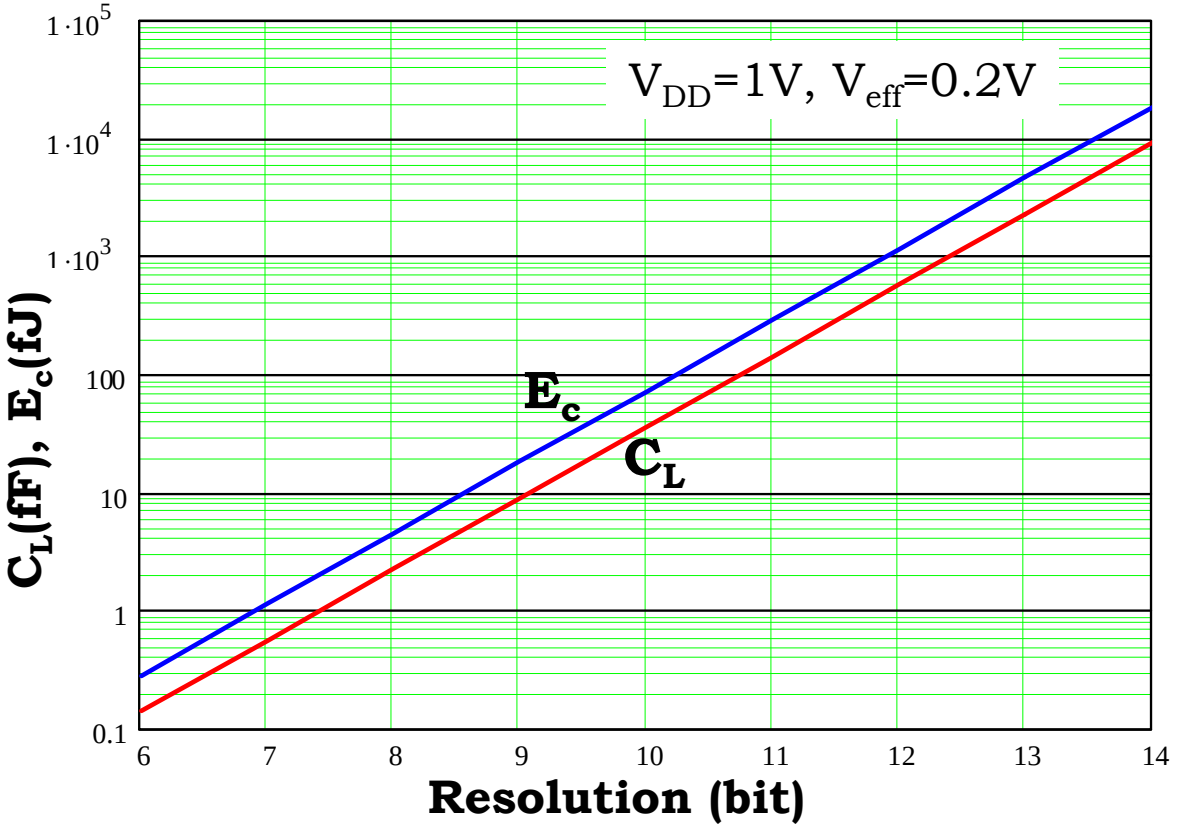




Required capacitance and consumed Energy

Node capacitances should be increased to realize higher ADC resolution. This results in increase of consumed energy of the dynamic comparator.

Flash ADC: E_c **determines the minimum FoM**
SAR ADC: E_c **cannot be neglected for higher resolution ADC**



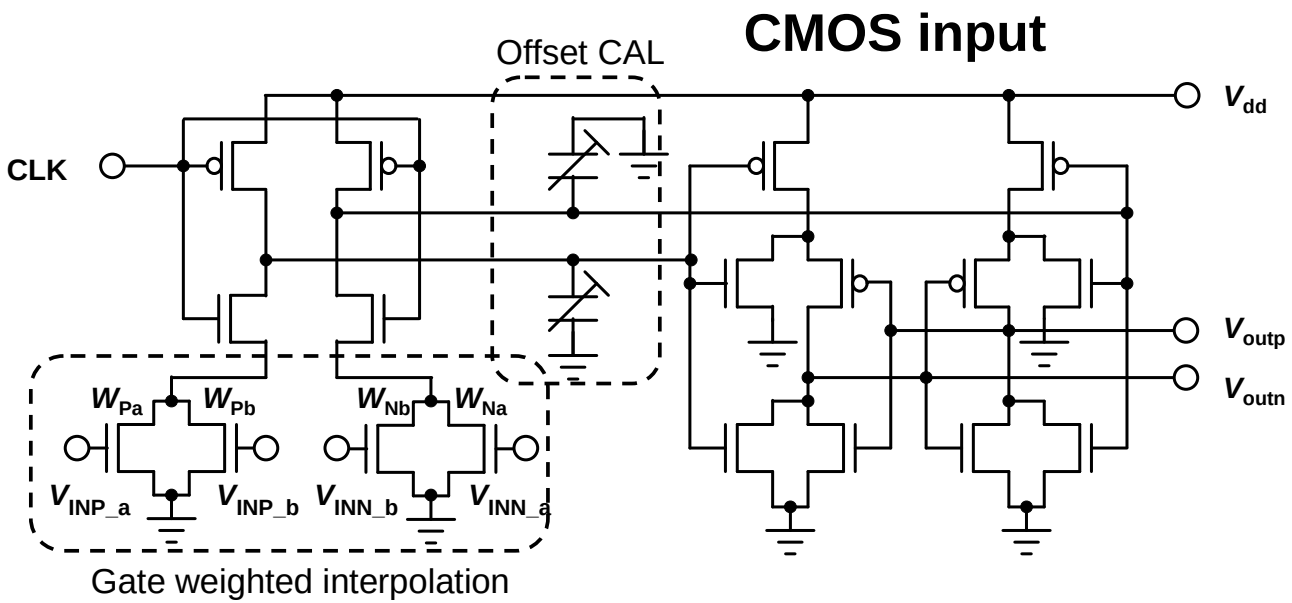
E_c: conversion energy

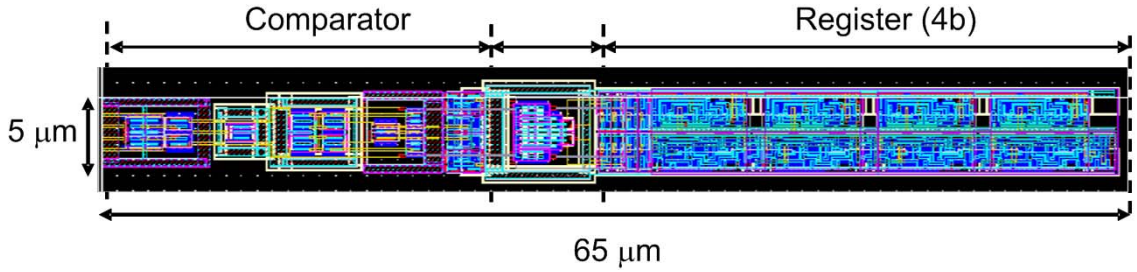
2fF & 4fJ	@8bit
40fF & 80fJ	@10bit
0.6pF & 1pJ	@12bit
10pF & 20pJ	@14bit

Noise improvement of dynamic comp.

Noise of comparator can be reduced by complementary ckt. and an optimization of the node capacitance.

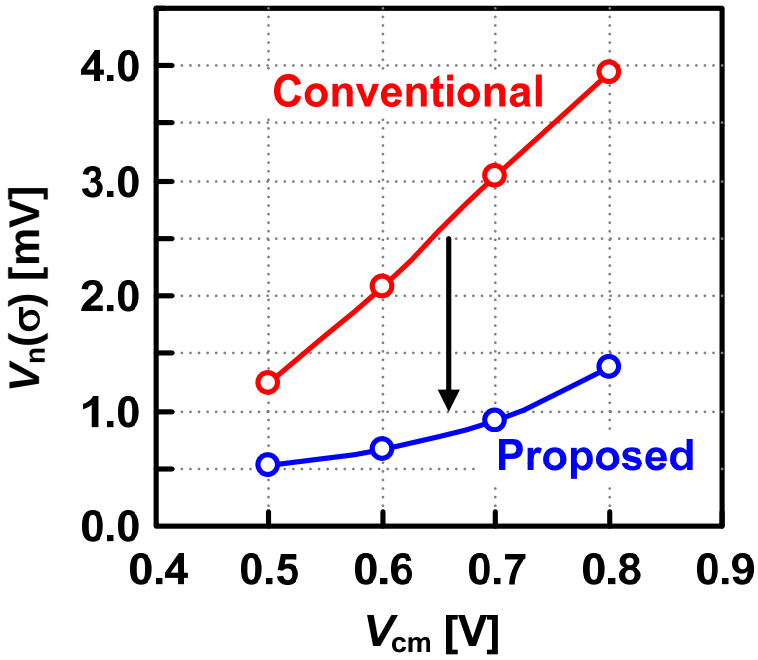
Dynamic comparator





90nm CMOS

Noise of comparator



M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," A-SSCC, Nov. 2008.

Yusuke Asada, Kei Yoshihara, Tatsuya Urano, Masaya Miyahara, and Akira Matsuzawa, "A 6bit, 7mW, 250fJ, 700MS/s Subranging ADC," A-SSCC, 5-3, pp. 141-144, Taiwan, Taipei, Nov. 2009.

P_d estimation of SAR ADC

Divide SAR ADC into three different circuits.

1) S/H&CDAC

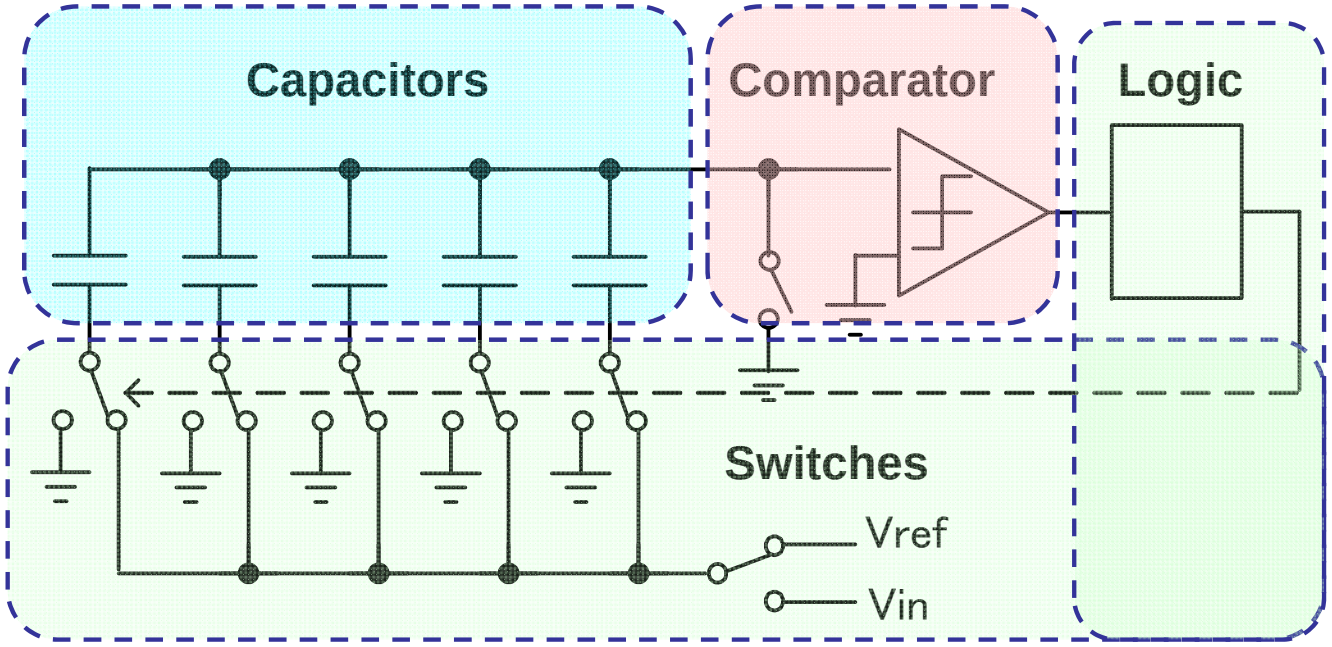
$$p_{ds} = 2 f_c C_s V_{DD}^2$$

$$C_s \propto \frac{2^{2N}}{V_{DD}^2}$$

2) Comparator

$$p_{dc} = 2(N+2) f_c C_L V_{DD}^2$$

$$C_L \propto \frac{2^{2N}}{V_{DD}^3}$$



2) Logic gates and switch drivers $p_{dc} = 2N f_c C_g V_{DD}^2$ **C_g: const**

C_s: Total sampling capacitance
C_L: Load capacitance of comparator
C_g: Effective capacitance of gates and switches

Akira Matsuzawa, ISSCC Forum, San Francisco, CA, Feb. 2011.

Equations to estimate the ADC performance

Quantization voltage

$$\overline{V_q^2} = \frac{1}{3}\left(\frac{V_{DD}}{2^N}\right)^2$$

Permitted thermal noise

$$V_{n\_th}^2 = \left(2^{2\Delta ENOB} - 1\right)\overline{V_q^2}$$

Thermal Noise of COMP.

$$V_{n\_th}^2 = \frac{4kT}{C_L}\left(\gamma\frac{V_{DD}}{V_{eff}} + 1\right)\left(\frac{V_{eff}}{V_{DD}}\right)^2$$

Sampling capacitor

$$C_s = \frac{4kT}{V_{n\_th}^2}$$

Load Capacitor Of COMP.

$$C_L = \frac{4kT}{V_{n\_th}^2}\left(\gamma\frac{V_{DD}}{V_{eff}} + 1\right)\left(\frac{V_{eff}}{V_{DD}}\right)^2$$

P_d of S/H

$$p_{ds} = 2f_c C_s V_{DD}^2$$

P_d of COMP.

$$p_{dc} = 2(N+2)f_c C_L V_{DD}^2$$

$$FoM = \frac{\left(P_{ds} + P_{dc} + P_{dg}\right)\cdot 2^{\Delta ENOB}}{f_c \times 2^N}$$

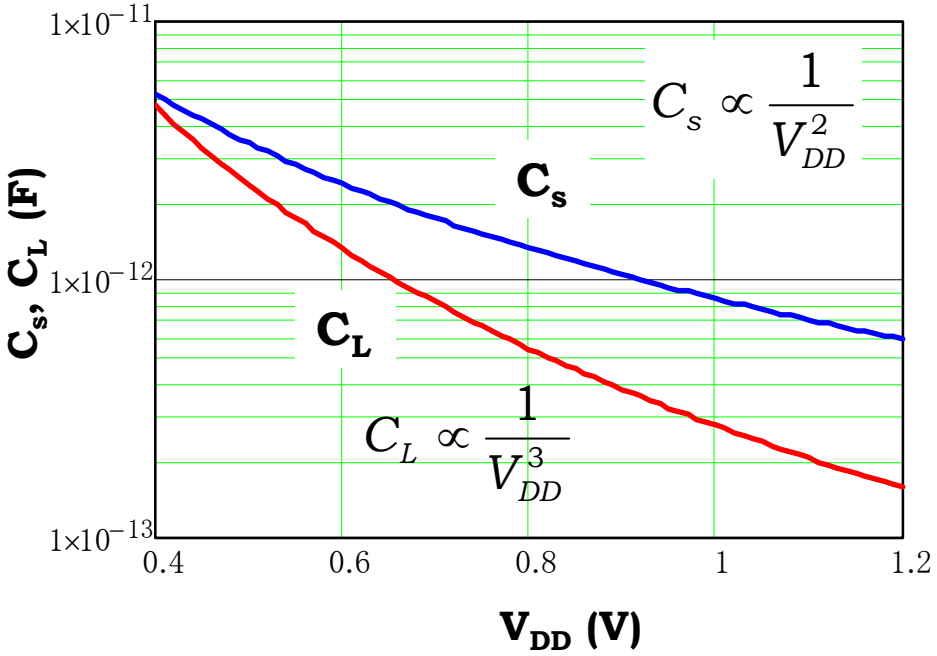
P_d of Gate

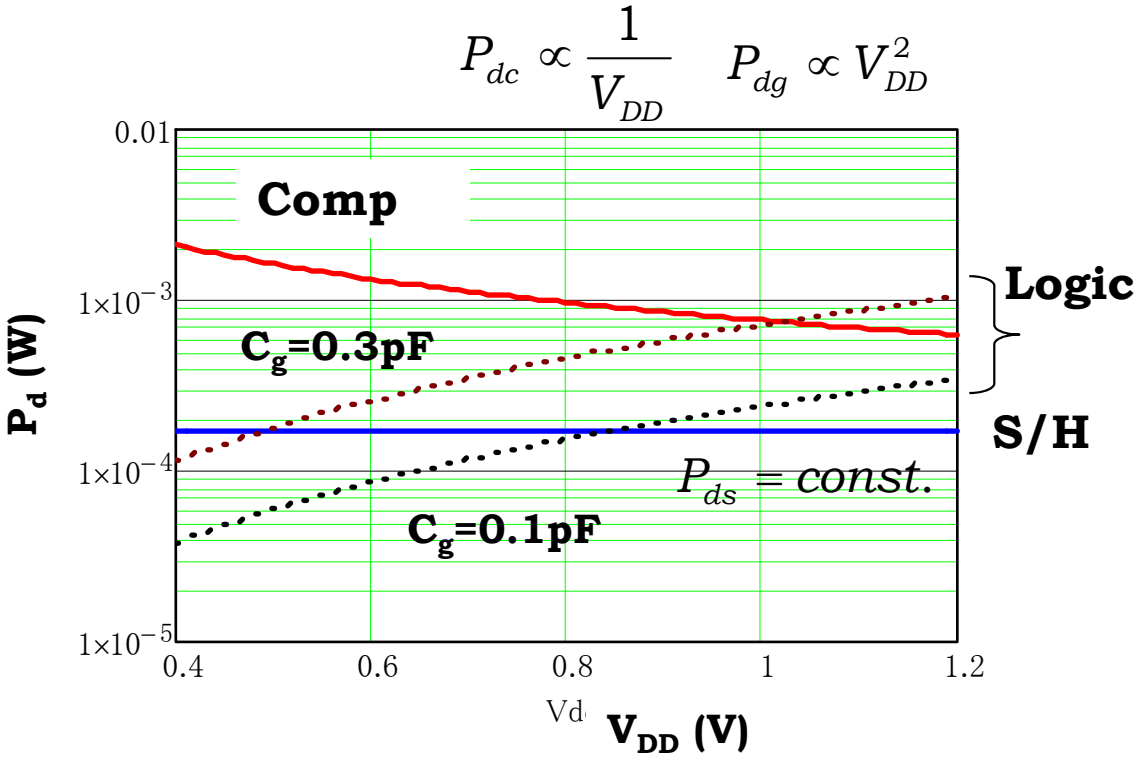
$$p_{dg} = 2Nf_c C_g V_{DD}^2$$

C, P_d, and FoM vs. V_{DD}

C_s and C_L increase with reducing V_{DD},
since the quantization voltage decreases with reducing V_{DD}.

P_d of S/H is constant for V_{DD},
however P_d of comparator increases with reducing V_{DD}.
P_d of logic gate decreases rapidly with reducing V_{DD}.

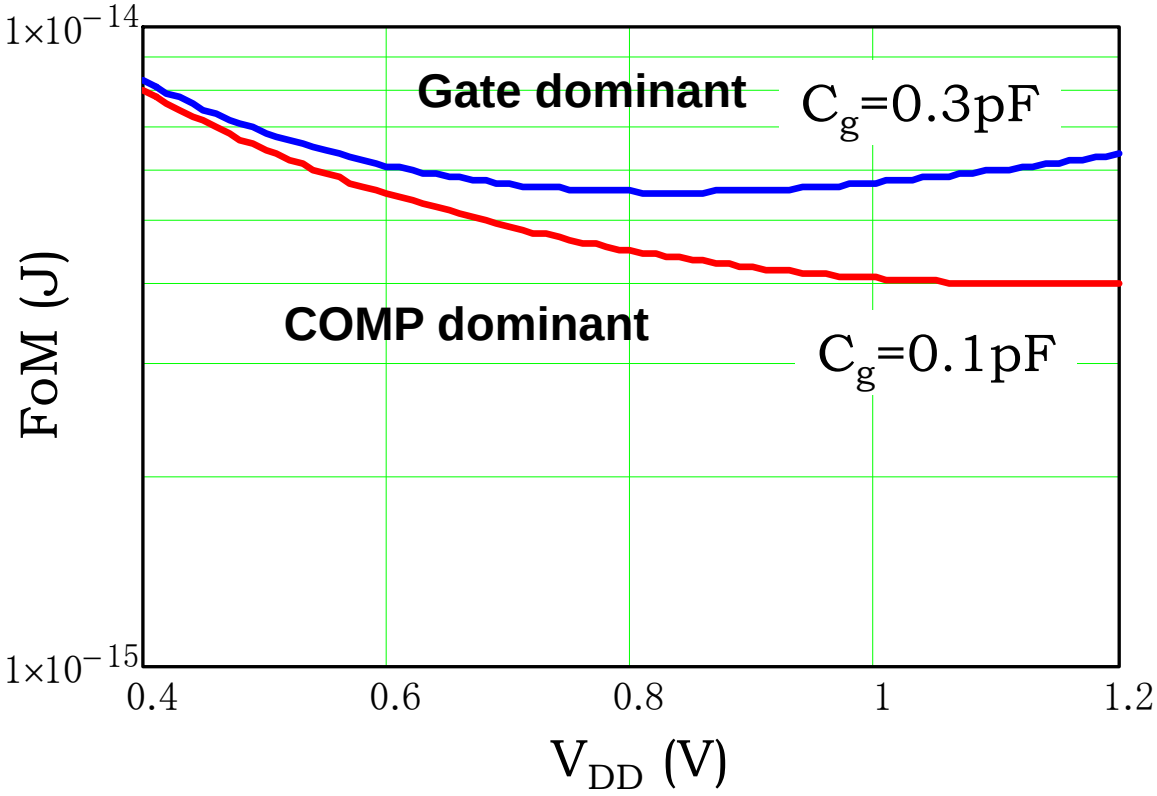




FoM vs. V_{DD}

FoM can be lowered by reducing V_{DD}, if P_d of logic gate is dominant.

Thus the voltage lowering is effective to reduce P_d for low resolution ADC, However, it is still difficult to reduce P_d by reducing V_{DD} for high resolution ADC, even if SAR ADC architecture is used.



$$N = 12bit$$

$$F_c = 100MHz$$

$$\Delta ENOB = 0.5bit$$

$$\gamma = 2$$

$$T = 300°K$$

$$V_{eff} = 0.15V$$

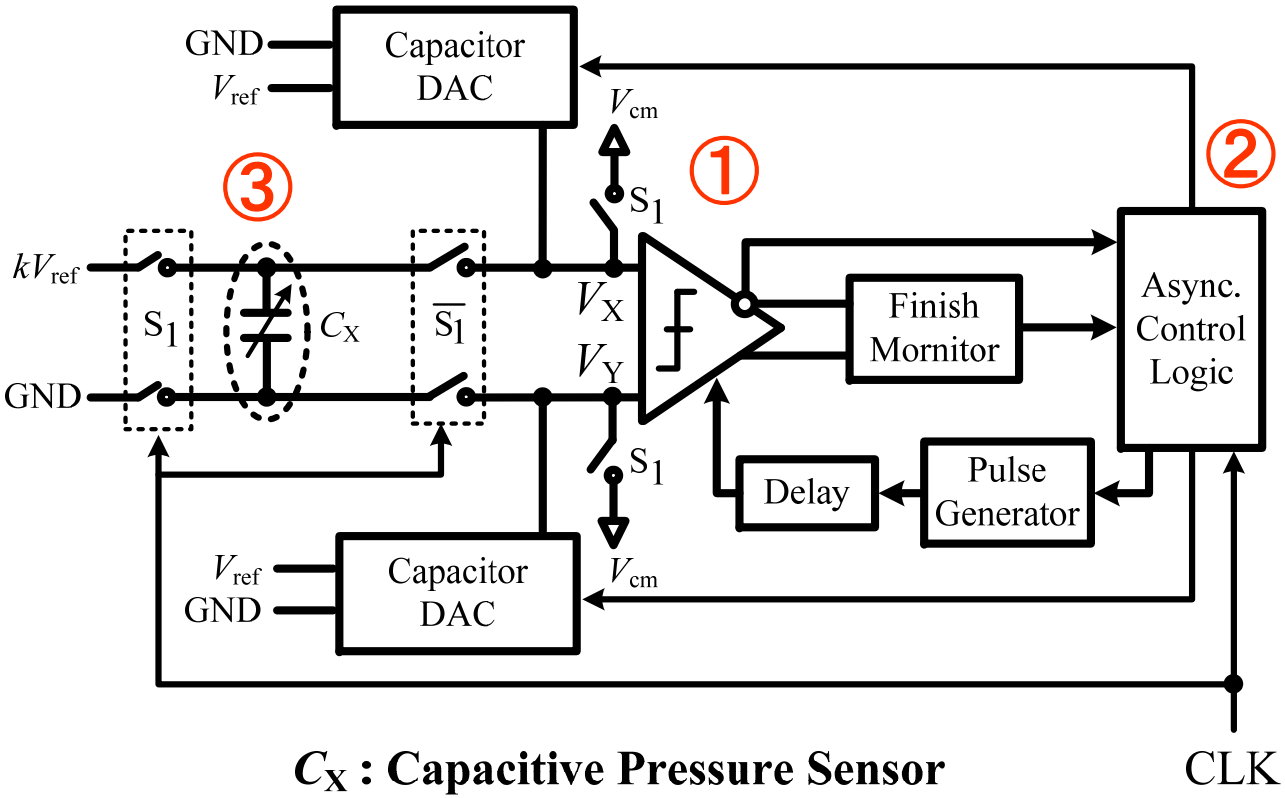
Example: An ultra-low power CDC

We have developed an ultra-low power Capacitance to Digital Converter.

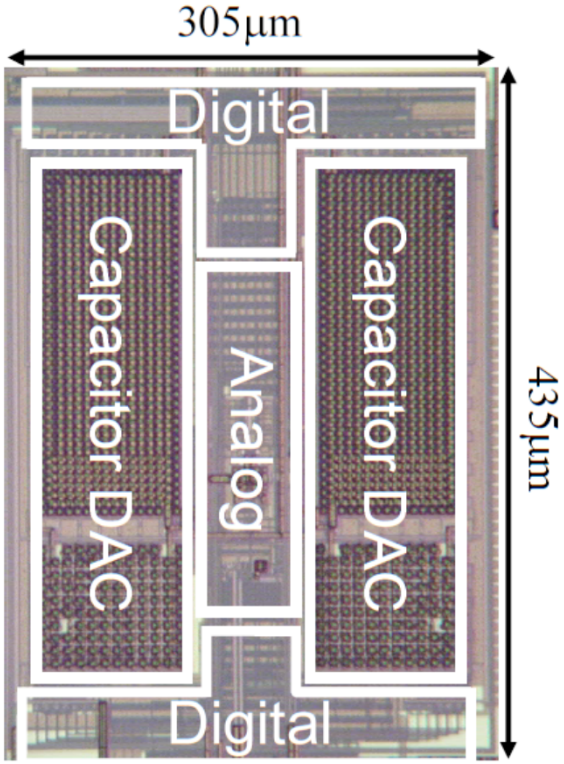
1. **10b SAR like architecture**
2. **Self-clocking**
3. **Single to differential**

3nA @ 30 times/sec

Tuan Minh Vo,Yasuhide Kuramochi, Masaya Miyahara,Takashi Kurashina, and Akira Matsuzawa "A 10-bit, 290 fJ/conv. Steps, 0.13mm22, Zero-Static Power, Self-Timed Capacitance to Digital Converter." SSDM 2009, OC¯



C_X : Capacitive Pressure Sensor

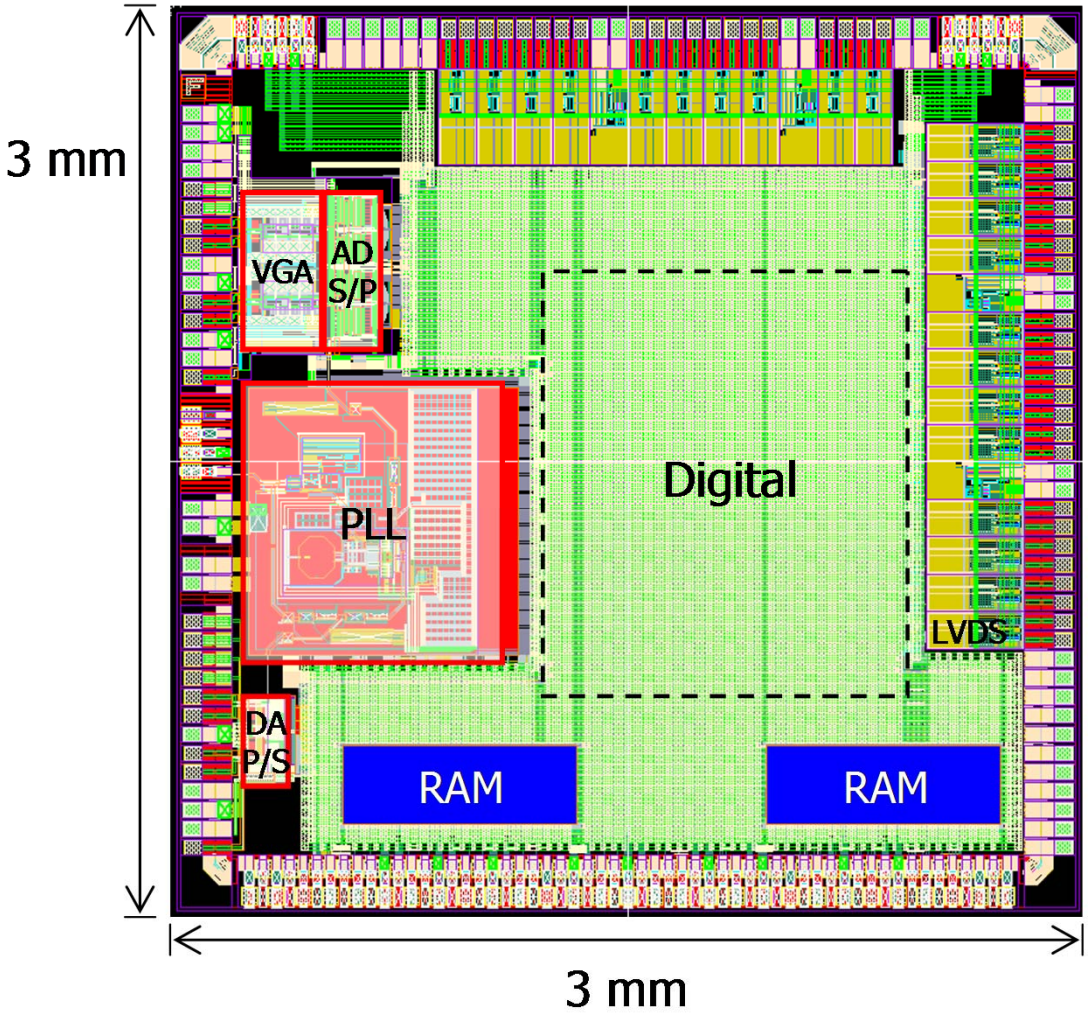


Flash ADCs

Developing baseband SoC

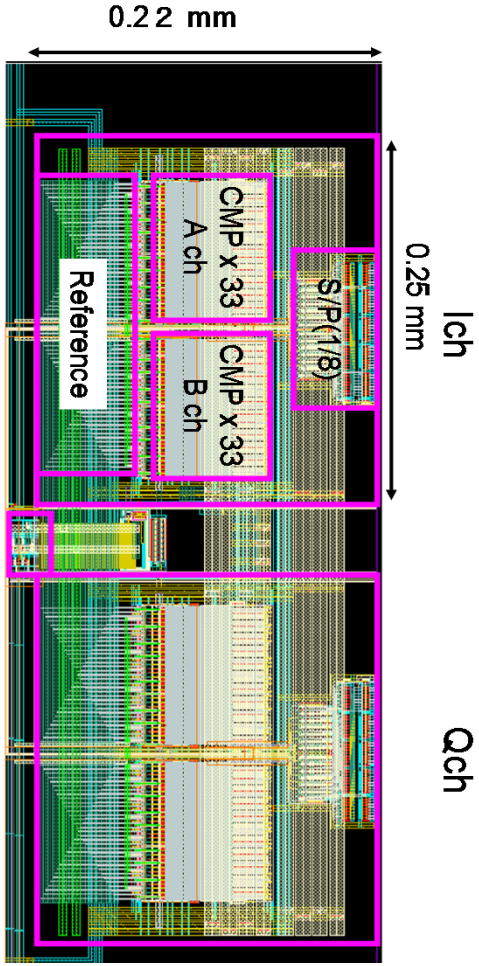
Developed chip for 60GHz transceiver integrating ADC, DAC, VGA, and PLL, using 40nm CMOS technology.

RX: 300mW, TX: 110mW
40nm CMOS technology

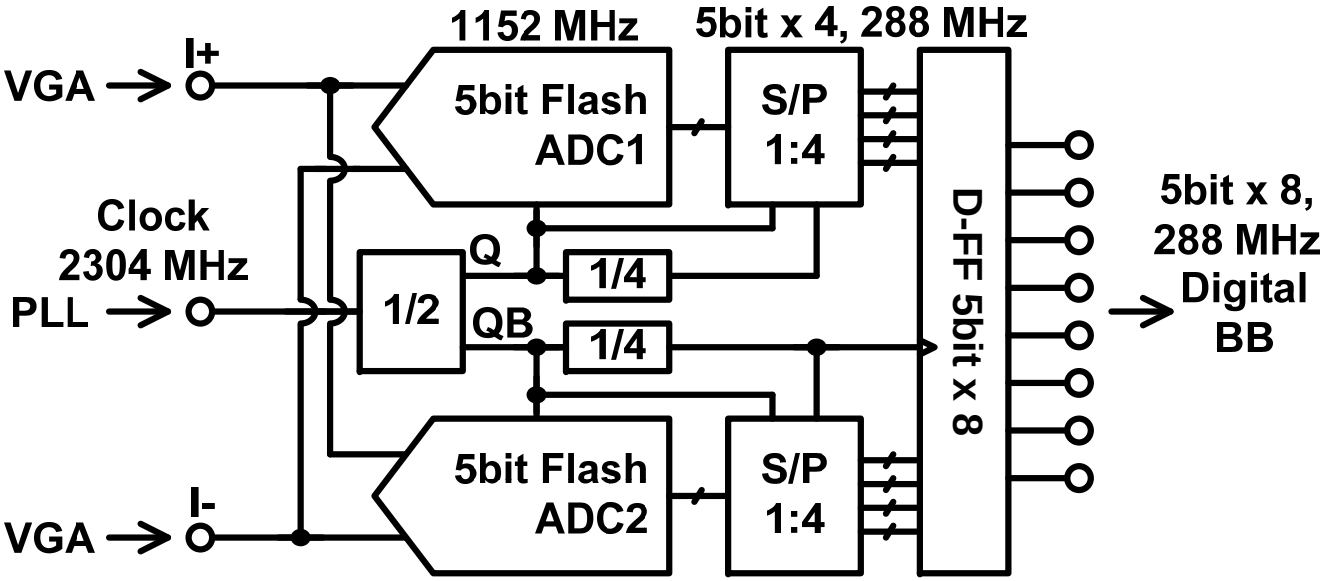


ADC 5b, 2.3GSps, 12mW/ch

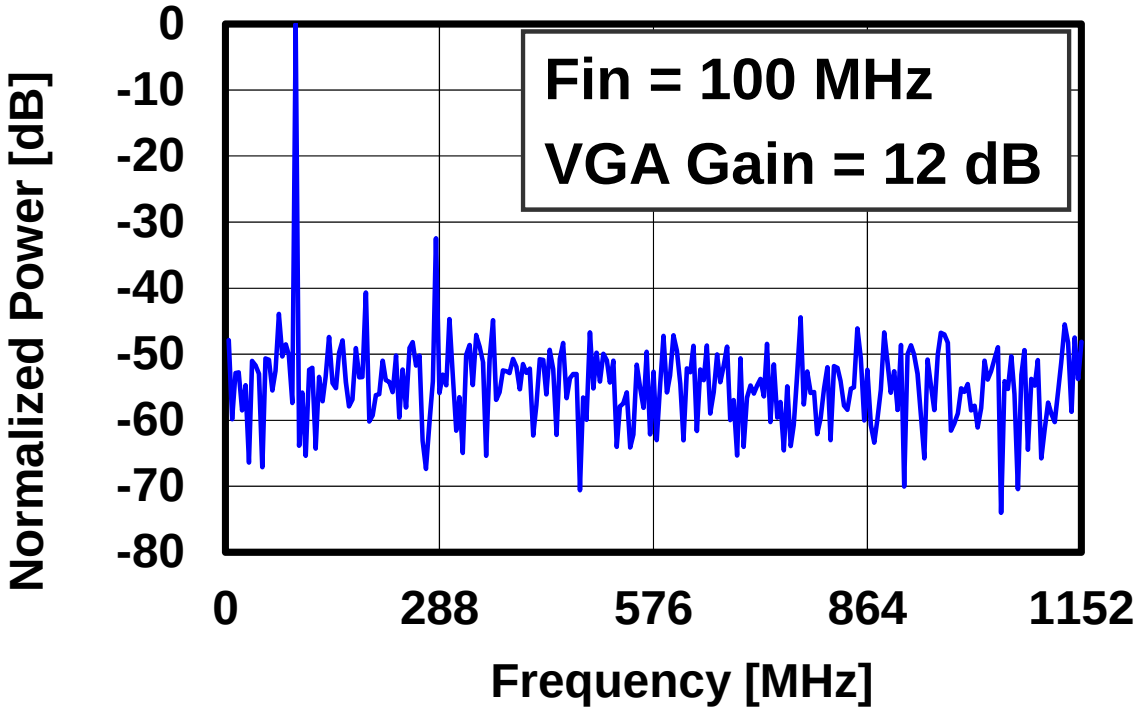
Tokyo tech developed



Analog Baseband : ADC



On-chip foreground calibration



VGA Gain range	0-40 dB
ADC Resolution	5 bit
Sampling rate	2304 MS/s
Power Consumption	VGA : 9 mW ADC : 12 mW*
DNL, INL	< 0.8 LSB
SNDR	26.1 dB
FoM of ADC	316 fJ/conv.-s

*single channel inc. S/P

ADC Comparison

	Architecture	Cal.	fs [GS/s]	SNDR [dB]	Power [mW]	FoM [fJ/-c.s.]	Process [nm]	Area [mm^2]
[1]	Flash	-	3.5	31.2	98	946	90	0.149
[2]	SAR	Internal	2.5	34.0	50	489	45	1
[3]	Folding	Internal	2.7	33.6	50	474	90	0.36
[4]	Pipeline, Folding	External	2.2	31.1	2.6	40	40	0.03
[5]	Flash	Internal	2.88	27.8	36	600	65	0.25
This work	**Flash**	**Internal**	**2.3**	**26.1**	**12**	**316**	**40**	**0.06**

[1] K. Deguchi, *et al*., *VLSI Circuits* 2007 [2] E. Alpman, *et al*., *ISSCC* 2009
[3] Y. Nakajima, *et al*., *VLSI Circuits* 2007 [4] B. Verbruggen, *et al*., *ISSCC* 2010
[5] T. Ito, *et al*., *A-SSCC* 2010

Flash ADC

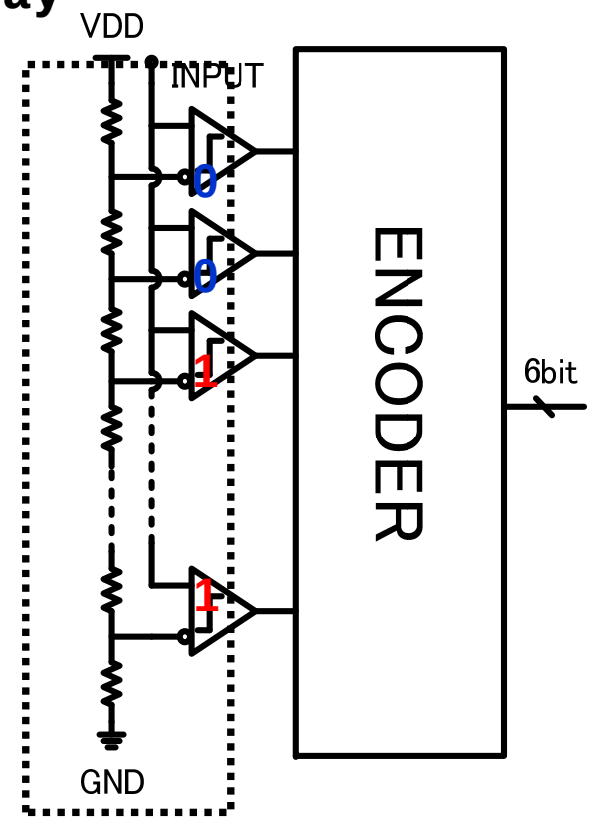
- **Expecting highest speed**
- **Comparator determines the ADC performance**

$$N \leq 6$$

Offset mismatch mainly determines the effective resolution.
Thermal noise can be neglected because of low resolution.

Flash ADC

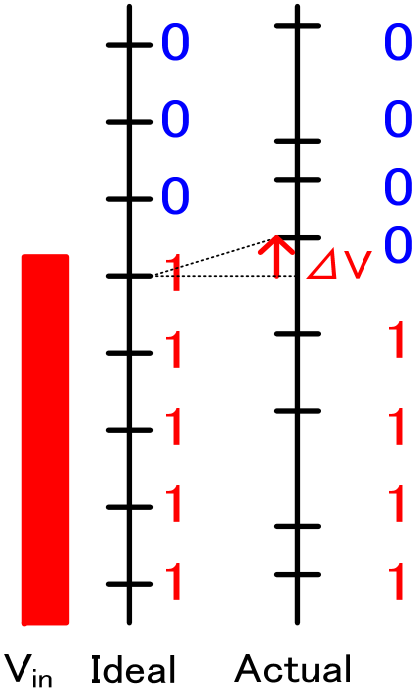
Comparator Array **6b: 63**

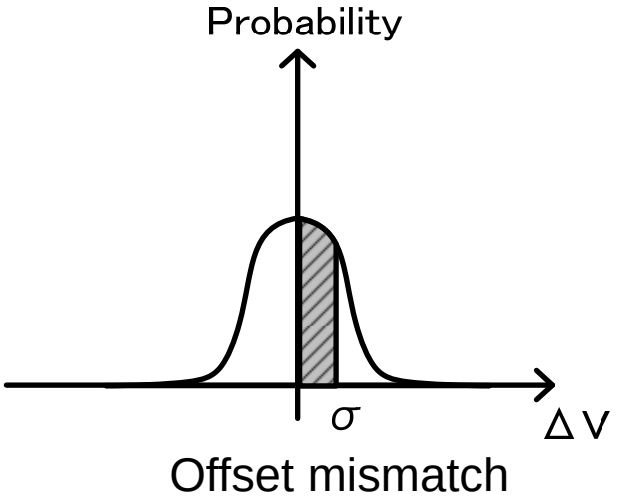


$$V_q = \frac{V_{FS}}{2^N}$$

6b: 63 V_{FS}=1.0V

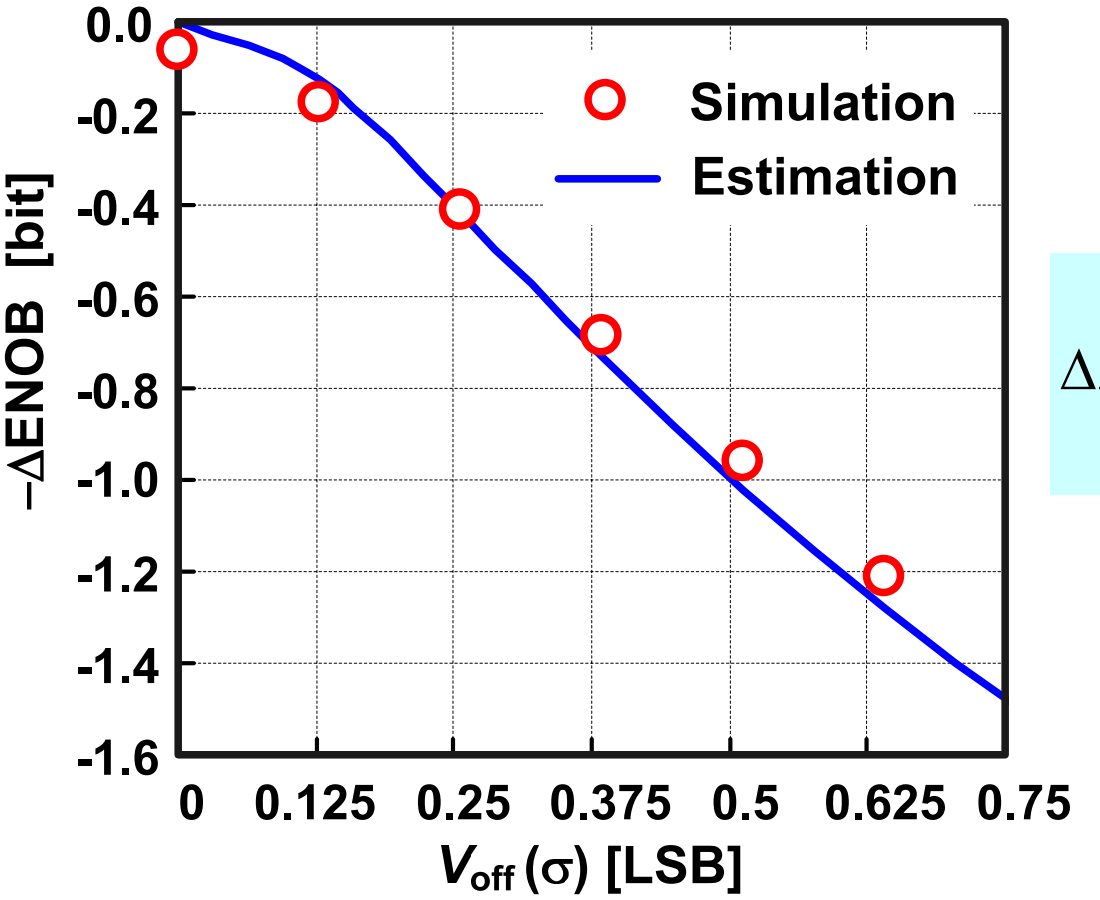
V_q=16mV, Mismatch <3mV





Performance of flash ADC

FoM is degraded by the offset mismatch voltage of the comparator. Offset mismatch voltage should be reduced at low voltage operation.



$$\mathrm{FoM} = \frac{P_d \cdot 2^{\Delta ENOB}}{f_c \times 2^N}$$

$$\Delta ENOB = \frac{1}{2}\log_2\left(1 + 12\left(\frac{V_{\mathrm{off}}(\sigma)}{V_q}\right)^2\right)$$

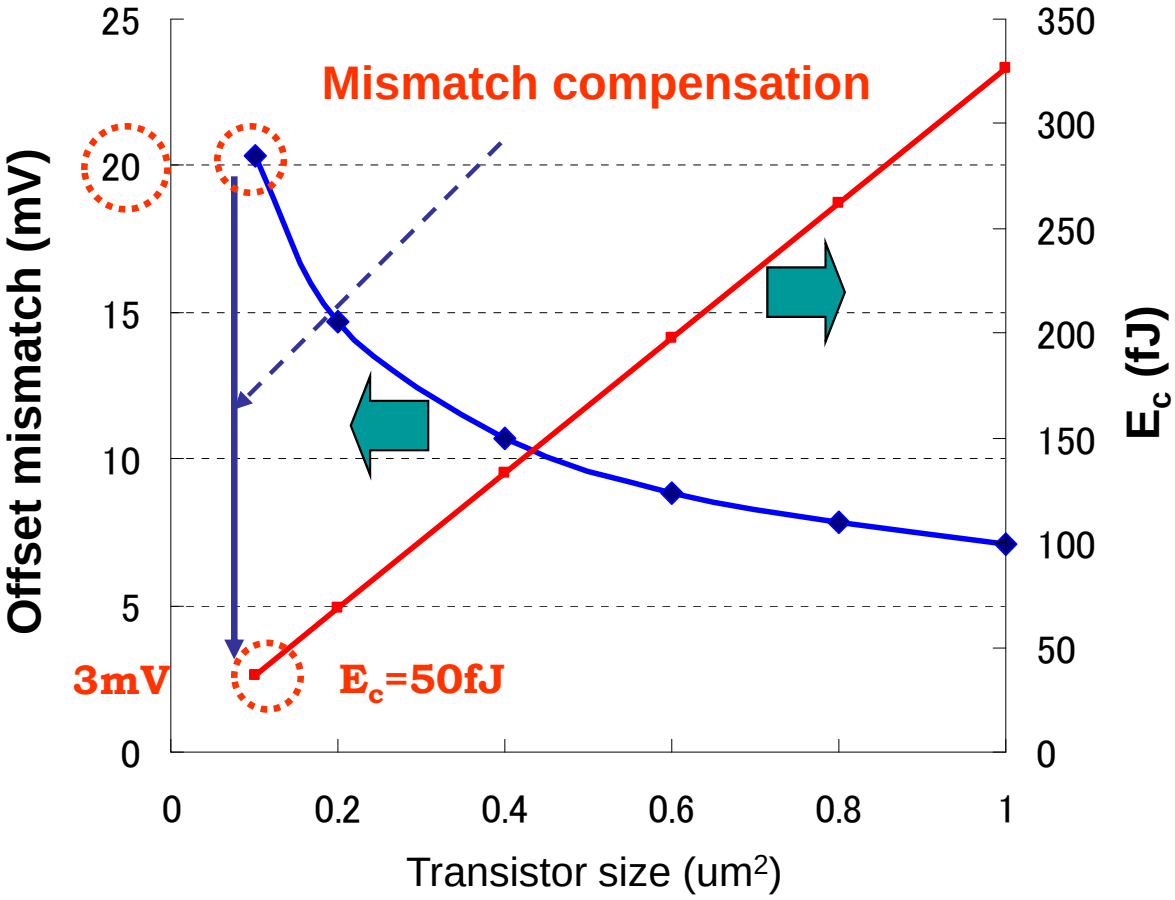
$V_{\mathrm{off}}(\sigma)$: Offset mismatch

V_q : 1LSB voltage

Tradeoff: mismatch and energy consumption

Serious tradeoff between mismatch of transistor and gate area.

Larger transistor is required to reduce mismatch voltage and results in increase of gate area and consumed energy.



Example

6bit ADC: V_{off}<3mV

E_C<50fJ→0.1um²→V_{off}=20mV

Needs mismatch compensation

20mV →3mV

$$V_{\text{offset}}(\sigma) \propto \frac{1}{\sqrt{LW}}$$

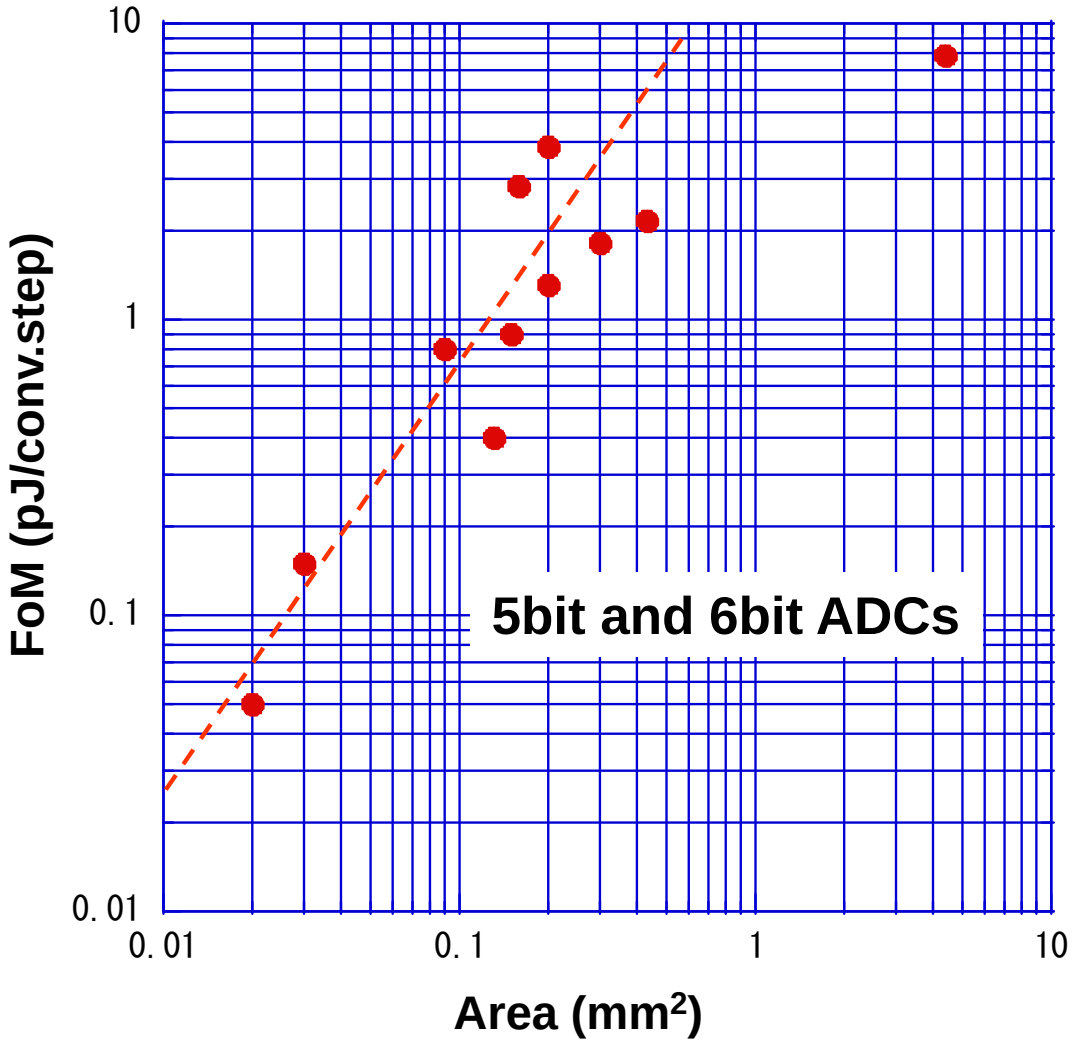
$$E_c \propto C_c \propto LW$$

$$E_c \propto \frac{1}{V_{offset}^2(\sigma)}$$

FoM vs. Area

Occupied area should be reduced to lower the FoM.

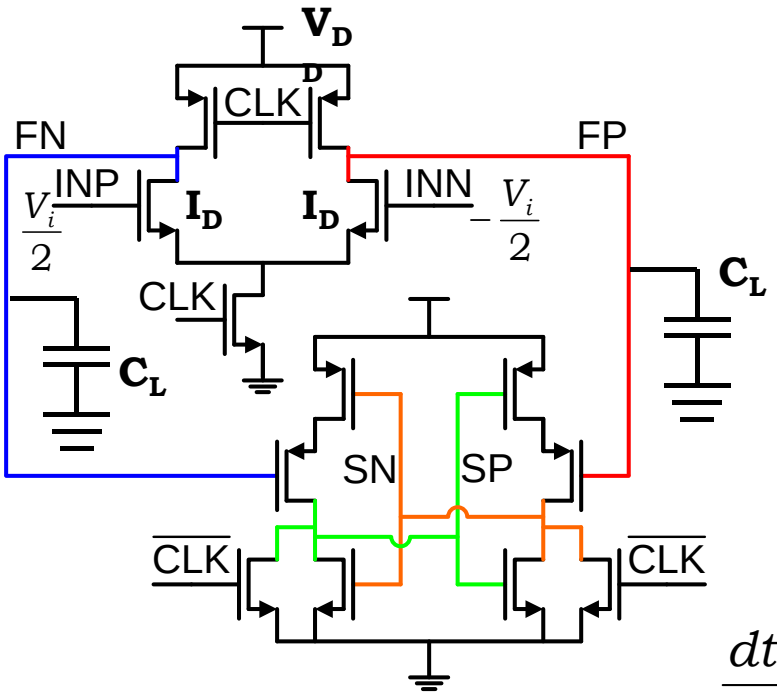
We must pay much attention to the occupied area.



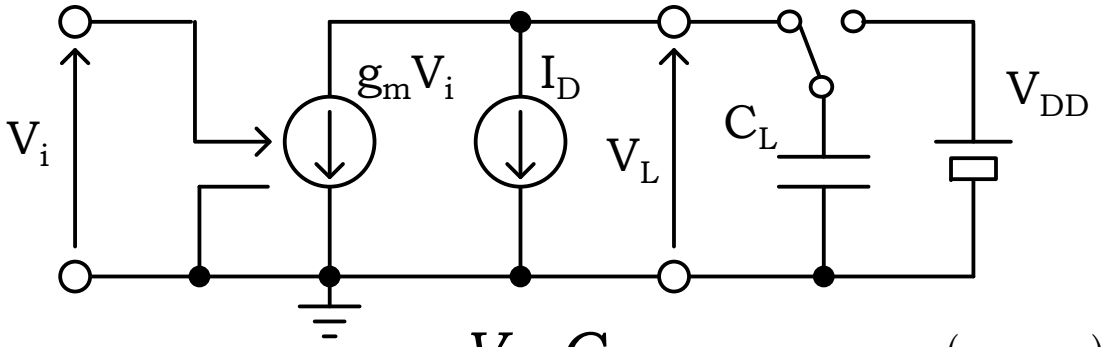
$$E_c \propto C \propto Area$$

Mismatch compensation for the dynamic comparator

Mismatch can be compensated by change of capacitance or current



Equivalent circuit for the fist stage

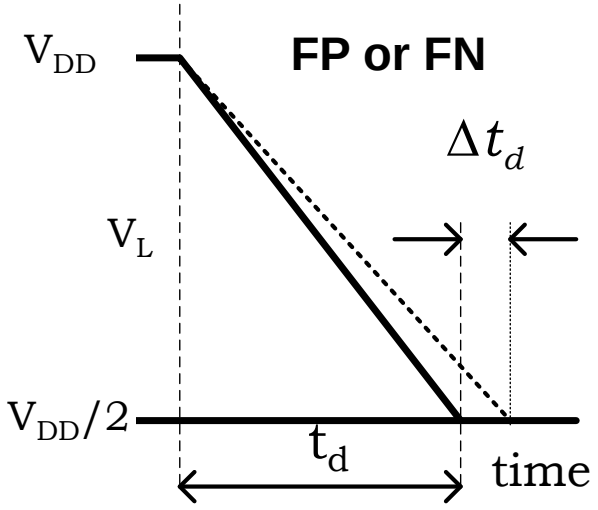


Delay time $t_d = \dfrac{V_{DD} C_L}{2 I_D}$

$$I_D \propto (V_{gs} - V_T)^{\alpha} = V_{eff}^{\alpha}$$

$$g_m = \frac{dI_D}{V_{eff}} = \alpha \frac{I_D}{V_{eff}}$$

$$\frac{dt_d}{dV_i} = \frac{dt_d}{dI_D} \cdot \frac{dI_D}{dV_i} = -\frac{V_{DD} C_L}{2 I_D} \frac{g_m}{I_D} = -t_d \frac{\alpha}{V_{eff}} \qquad \therefore \frac{g_m}{I_D} = \frac{\alpha}{V_{eff}}$$



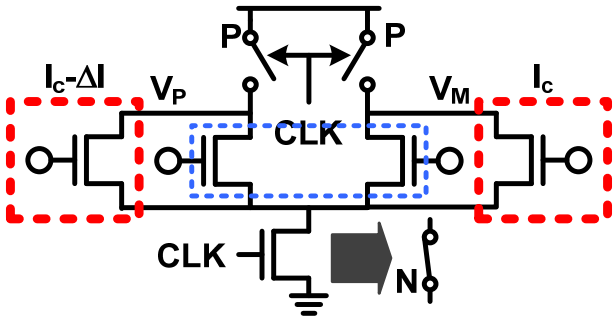
$$\therefore \frac{\Delta t_d}{t_d} = \alpha \frac{\Delta V_i}{V_{eff}} \qquad \frac{\Delta t_d}{t_d} = \left(\frac{\Delta C_L}{C_L} - \frac{\Delta I_D}{I_D} \right)$$

$$\therefore \frac{\Delta t_d}{t_d} = \alpha \frac{\Delta V_i}{V_{eff}}$$

$$\Delta V_i = \frac{V_{eff}}{\alpha} \left(\frac{\Delta C_L}{C_L} - \frac{\Delta I_D}{I_D} \right)$$

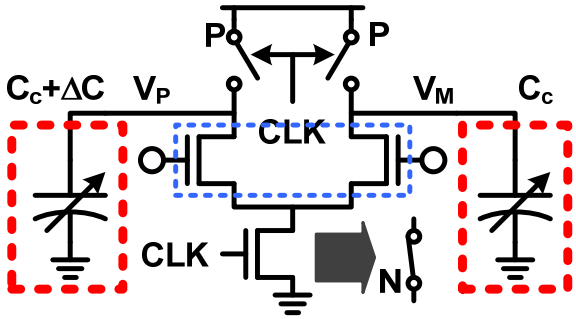
Digital calibration methods for mismatch

Resistor ladder type

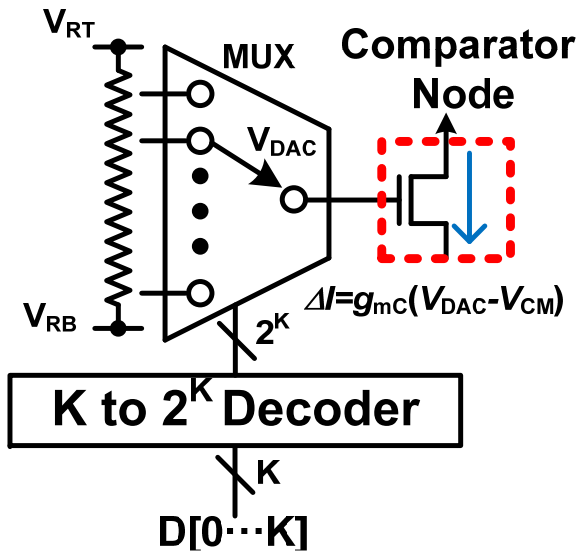


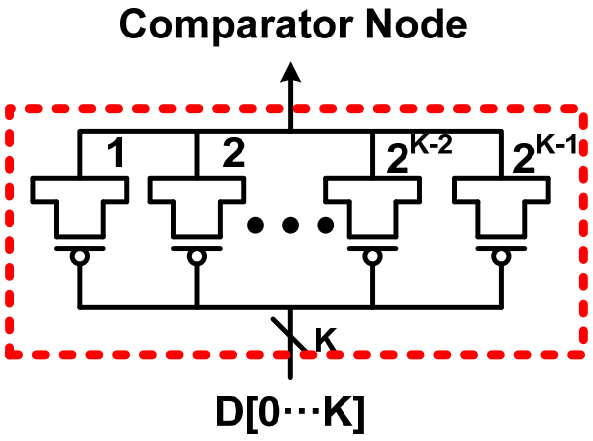
Current calibration

Capacitor array type



Capacitance calibration





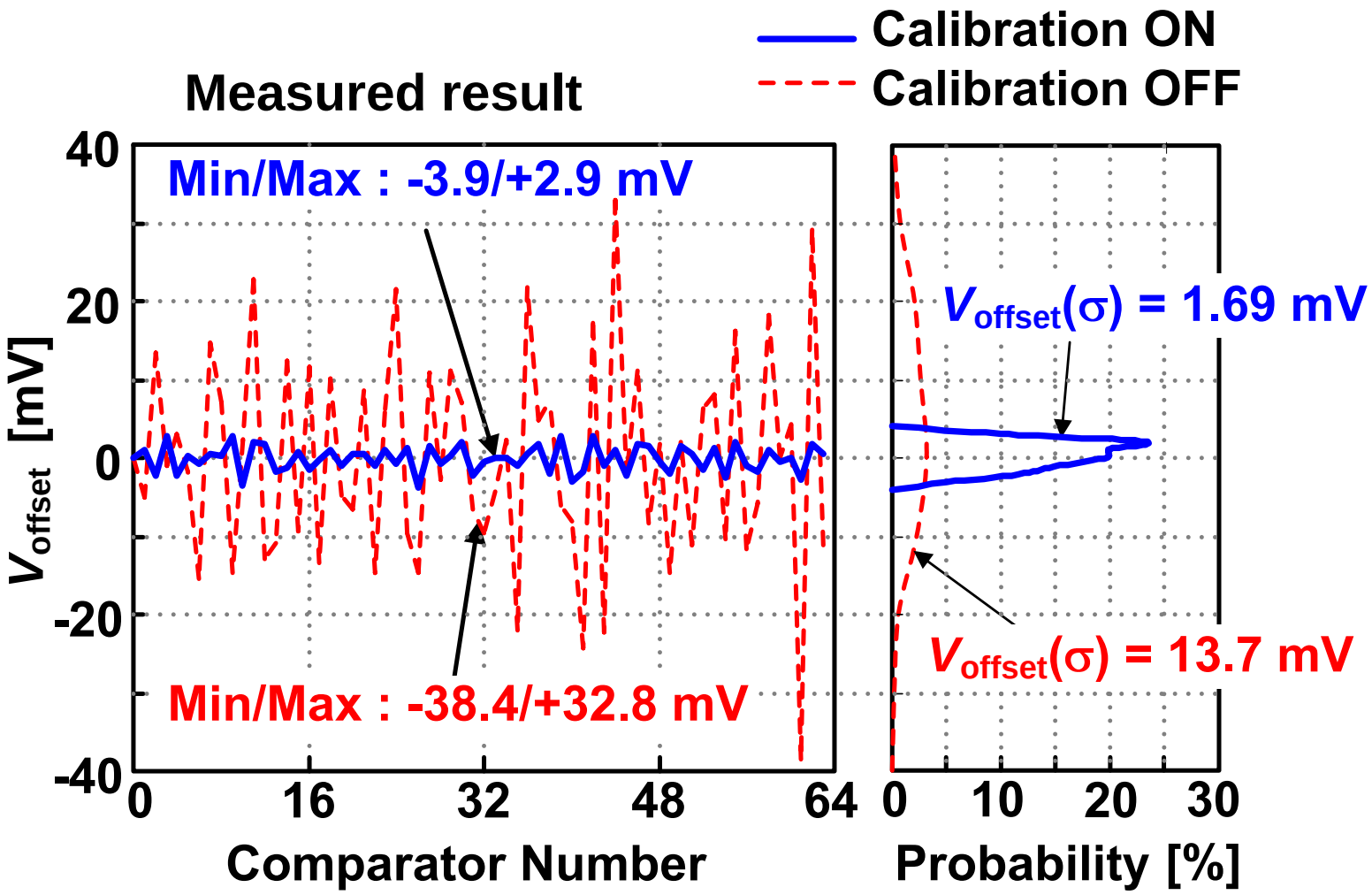
Binary weighted capacitor array

Y. Asada, K. Yoshihara,T. Urano, M. Miyahara and A. Matsuzawa,

"A 6bit, 7mW, 250fJ, 700MS/s Subranging ADC" A-SSCC, pp. 141-144, Nov. 2009.

Effect of digital mismatch compensation

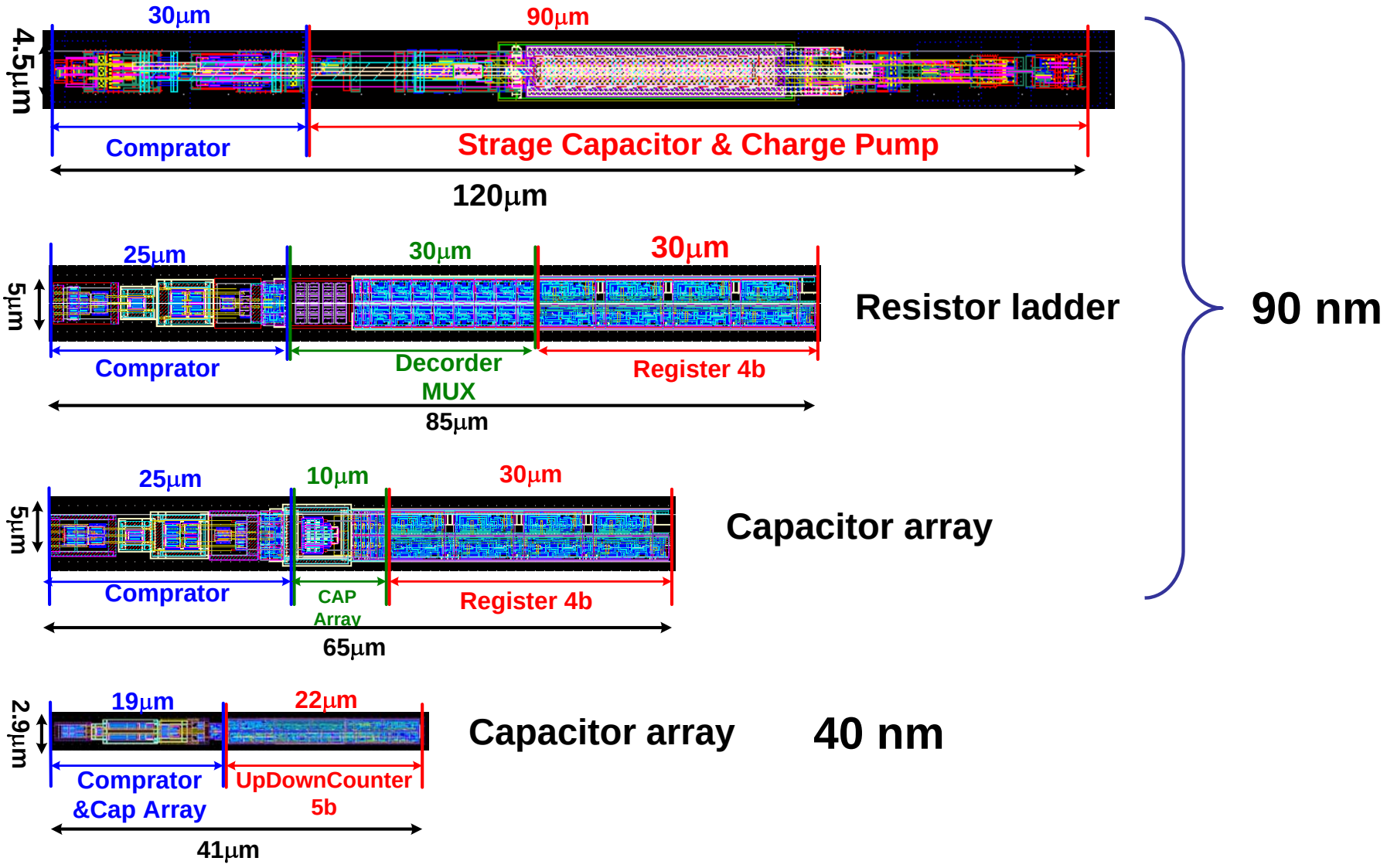
The mismatch voltage can be reduced from 14mV to 1.7mV.



M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," A-SSCC, Nov. 2008.

Area comparison

Penalty area for digital compensation will be reduced with technology scaling.

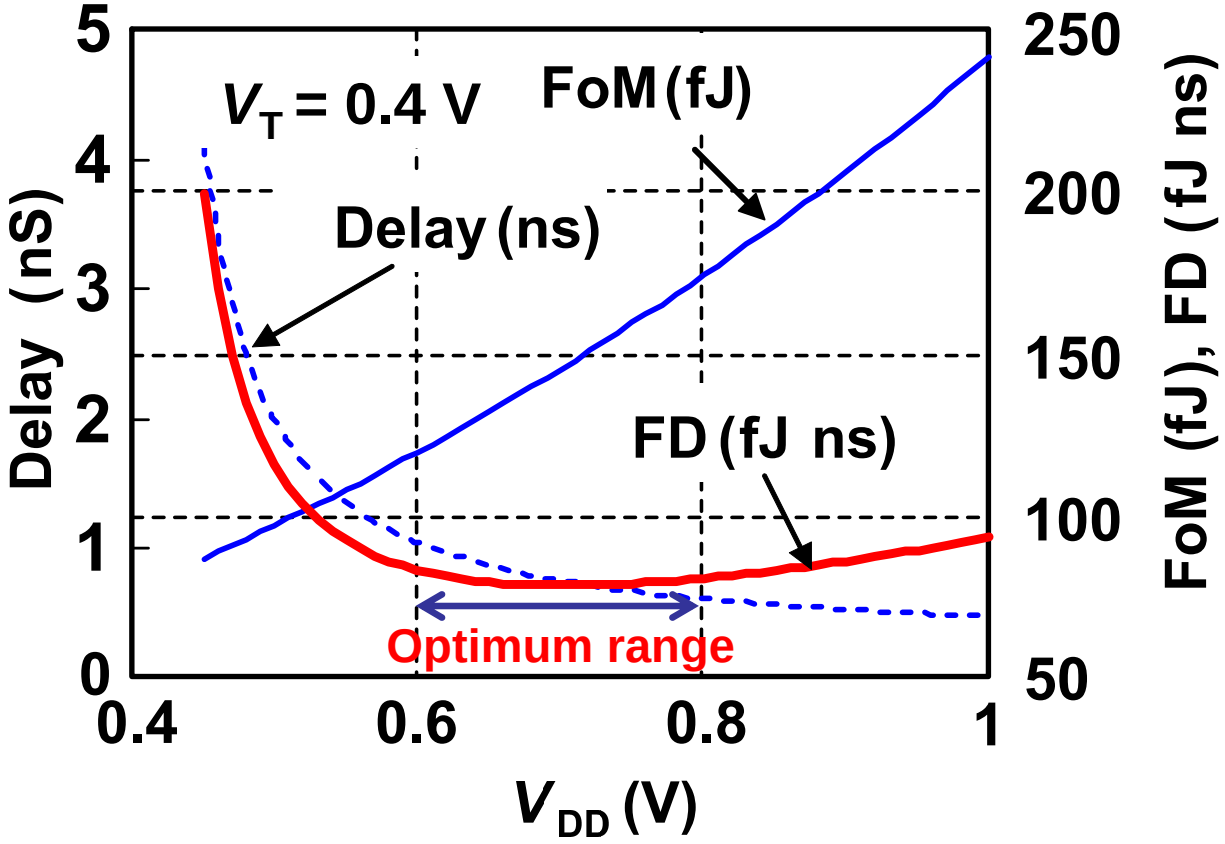


FoM delay (FD) product

The FD product suggests the balance between the number of interleaving and decrease of energy consumption.

Delay is increased and the operating speed is lowered by reducing V_{DD}

We should investigate the optimum V_{DD} by FD product.



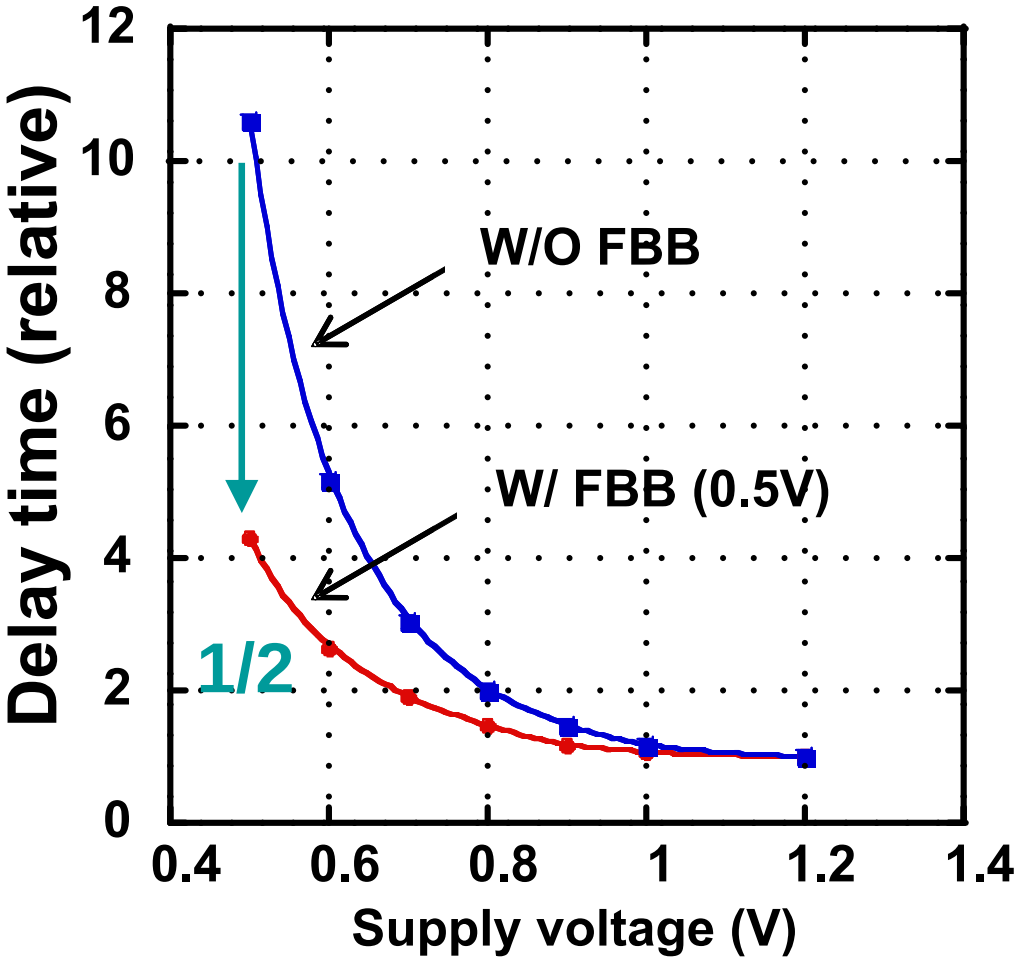
$$FD = FoM \times Delay$$

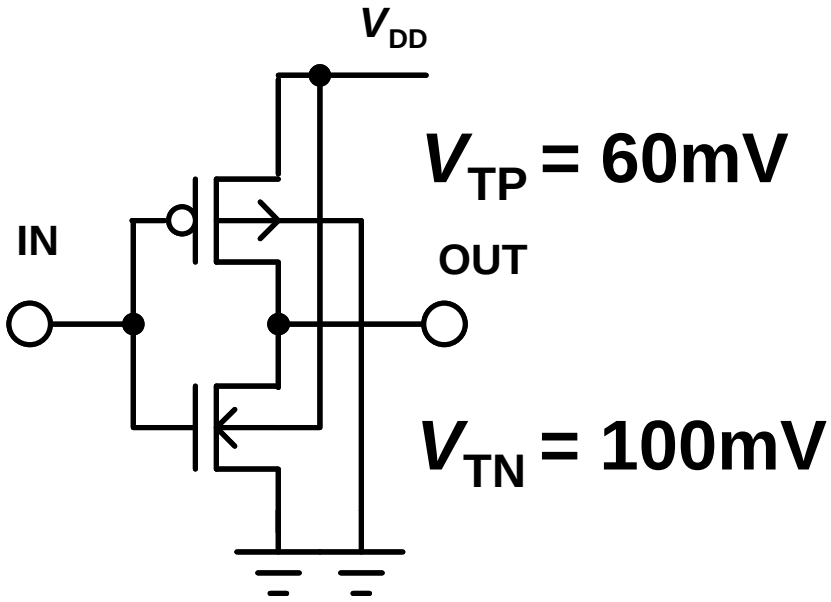
Delay time

$$T_d = k \frac{V_{DD}}{(V_{DD} - V_T)^{\alpha}}$$

Forward body biasing

Forward body biasing can decrease the delay time (1/2) and can be used easily at 0.5 V operation.



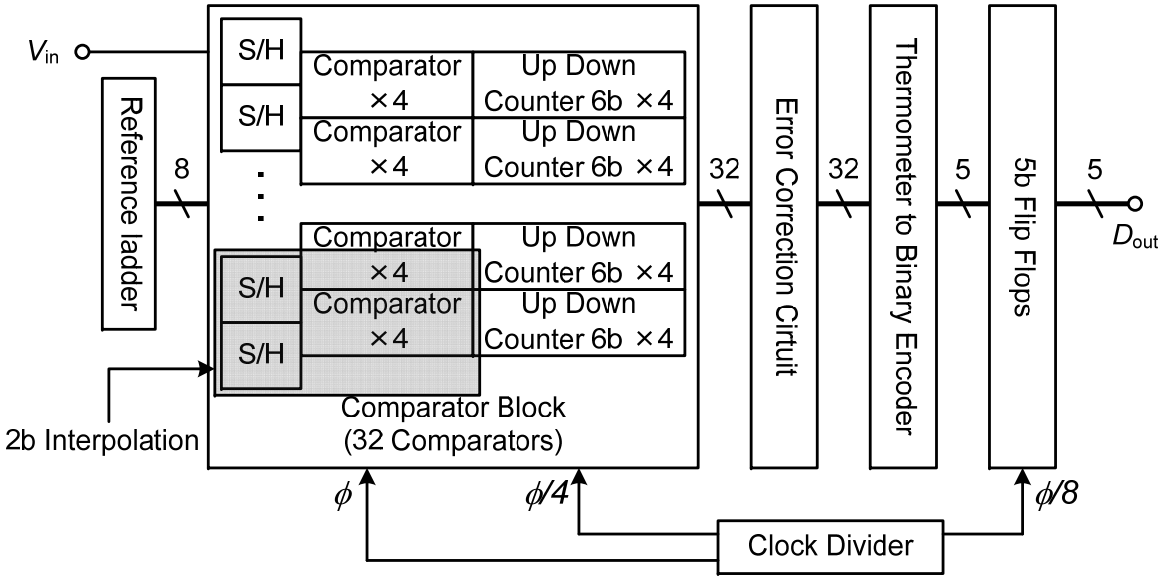


Increased leakage current in the proposed ADC is 0.32 mA by forward body biasing.

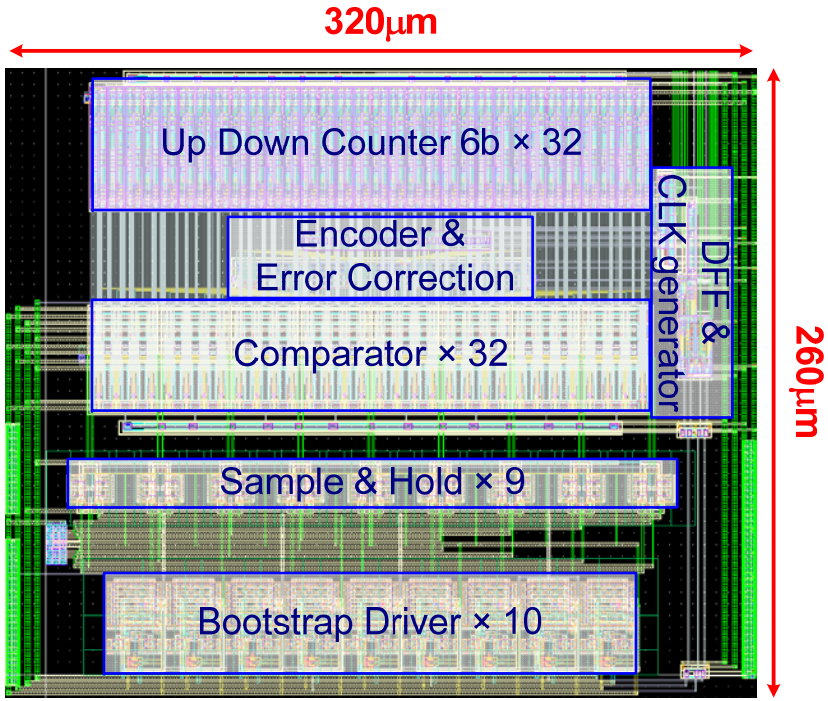
ADC Structure

5bit 0.5V 600MSps Flash ADC is designed and fabricated in 90nm CMOS.

S/H circuits use gate boosted switches.



Block diagram of ADC



Chip microphotograph

M. Miyahara , J. Lin, K. Yoshihara, and A. Matsuzawa,
“A 0.5 V, 1.2mW, 160fJ, 600 MS/s 5 bit Flash ADC”
A-SSCC, pp. 177-180, Nov. 2010.

Performance Summary

A high speed and low FoM 0.5V flash ADC has been realized.

Reference #	[7]	[8]	[9]	[10]	**This work**
Resolution (bit)	5	5	5	5	**5**
fs (GS/s)	0.5	1.75	1.75	0.06	**0.6**
SNDR (dB)	26	30	30	26	**27**
Pd (mW)	5.9	2.2	7.6	1.3	**1.2**
Active area (mm^2)	0.87	0.017	0.03	-	**0.083**
Vdd (V)	1.2	1	1	0.6	**0.5**
FoM(fJ)	750	50	150	1060	**160**
CMOS Tech. (nm)	65	90	90	90	**90**
Architecture	SAR	Fold+Flash	Flash	Flash	**Flash**

FoM_{Fmax} = 160fJ @ 600MSps
FoM_{Best} = 110 fJ @ 360MSps

[7] B. P. Ginsburg, J. Solid-State Circuits 2007.
[8] B. Verbruggen, ISSCC 2008.
[9] B. Verbruggen, VLSI Circuits 2008.
[10] J. E. Proesel, CICC 2008.

Summary of energy efficient ADC design

Reducing static power

Resistor DAC → Capacitor DAC

OpAmp based → Comparator based

Reducing capacitance

$$E_d \approx CV_{DD}^2$$ # of CMP Flash → SAR

$$\Delta V_T \propto \frac{1}{\sqrt{C_G}}$$ TR size Large TR → Small TR with compensation

$$\overline{V_n} \propto \frac{1}{\sqrt{C}}$$ Noise Use complementally ckt.

Clock Use self clocking

Reducing voltage

Effective to digital gates and low resolution ADC

Use forward or adaptive body biasing