Essence and Technology Direction of ADC Design

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Abstract- This paper reviews and discusses an essence and the technology direction of ADC design from the point of view of conversion energy. Conversion energy of a high resolution ADC is reaching the theoretical limit, however there is still a large gap for a low resolution ADC. SAR ADC is the most energy efficient ADC and further energy reduction is possible to optimize the supply voltage. Conversion energy of a flash ADC can be reduced by reducing the transistor size and supply voltage. FD product is proposed to find the balance between the conversion energy and the conversion speed.

Keywards- ADC, low energy, low voltage, SAR, and Flash

I. INTRODUCTION

An ADC is essentially required for almost all the systems and sometimes it causes a bottle neck of the system performance. For example, an ultimate data rate of communication system, C_{max} given by the modification of Shannon's theorem is

$$C_{\max} \approx f_s \cdot N \tag{1}$$

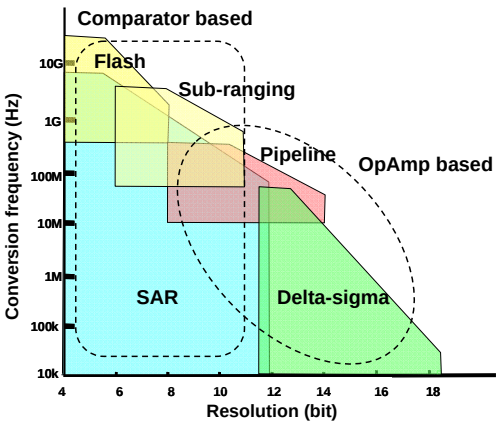

Fig. 1. Resolution range, conversion frequency range, and conversion architecture of ADCs.

where, f_c is a conversion frequency and N is the resolution of the ADC. Therefore, a high speed and high resolution ADC is essentially required for high data rate communications.

There are many ADC architectures according to the resolution and conversion frequency, as shown in Fig. 1. Conventionally low resolution ADCs use a comparator based architecture and higher resolution ADCs use an OpAmp based architecture. In this paper, the comparator based ADCs, such as a SAR ADC and a flash ADC are analyzed in conversion energy and supply voltage.

II. ENERGY CONSUMPTION OF ADC

An ADC needs a sampling circuit and it determines the fundamental energy consumption for a given resolution, N, as follows [1].

$$E_{sample} = 24kT2^{2N} \tag{2}$$

However, an ADC needs a comparison process and it also consumes energy [2]. The energy consumption of an ADC becomes,

$$E_{ADC} \approx N \times E_{sample} \tag{3}$$

Fig. 2 plots recent published ADCs on the plane of the resolution vs. the consumed energy. It also shows E_{sample} and E_{ADC} shown in (2) and (3).

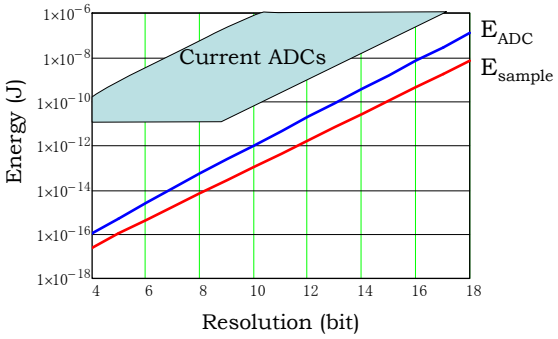

Fig. 2. Resolution and consumed energy of ADCs.

The energy consumption of current ADCs of which resolution is higher than 9 bits is reaching 10x of the fundamental limit. However, a larger gap exists for the lower resolution ADCs. It can be supposed that the energy consumption is not determined by the fundamental thermal noise limitation, but determined by the peripheral circuits such as logic gates, clock buffers, interconnections, and reference circuits.

III. ENERGY EFFICIENT SAR ADC DESIGN

SAR ADC is well known as the most energy efficient ADC architecture if the resolution is lower than 12 bits.

SAR ADC consists of three important building blocks: a S&H circuit, a comparator, and logic gates, as shown in Fig. 3. Fig. 4 shows consumed energies of each circuit and total ADC as a function of supply voltage.

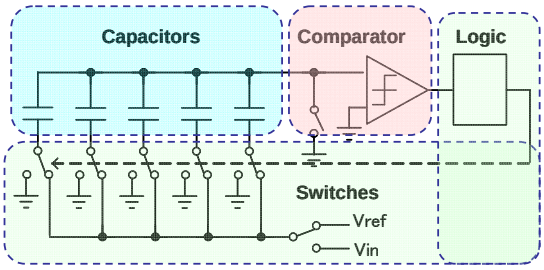

Fig. 3. SAR ADC and its building blocks.

A logic gate can reduce the consumed energy by reducing supply voltage. However, a comparator requires larger capacitance to keep the SNR high enough with reducing supply voltage and results in increase of energy consumption. Therefore A SAR ADC has a optimum supply voltage to reduce the conversion energy.

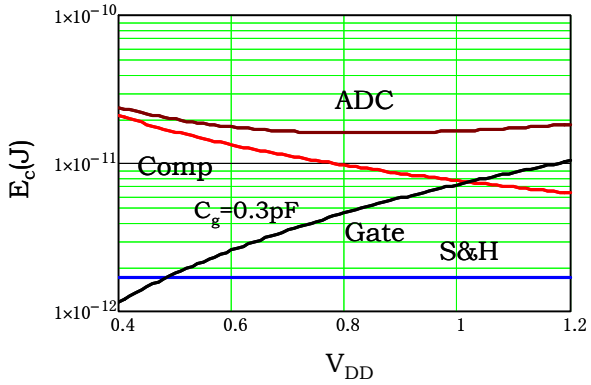

Fig. 4. Ec vs. V_{DD} for SAR ADC.

IV. ENERGY EFFICIENT FLASH ADC DESIGN

A flash ADC architecture, show in fig. 5 is used for high conversion speed and low resolution applications. Energy consumption of a N-bit Flash ADC, E_{c_ADC}, can be expressed as [3],

$$E_{c\_ADC} = 2^N \cdot E_{c\_comp} \quad (4)$$

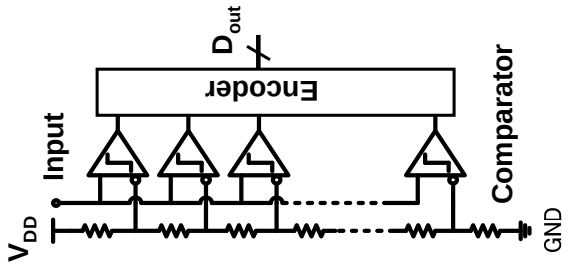

Fig. 5. Flash ADC.

where, E_{c_comp} is an energy consumption of each comparator and its related logic gates.

We can reduce the energy consumption by reducing the transistor size in the comparator, however it results in increase of offset mismatch voltage, as shown in Fig. 6.

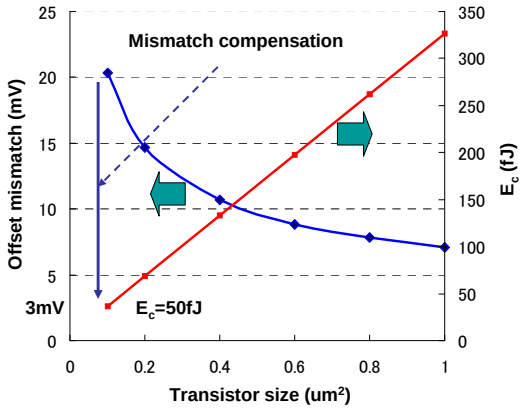

Fig. 6. Offset mismatch and consumed energy of comparator.

A digital mismatch compensation technique can reduce it, even though using smaller transistor size. The supply voltage lowering can reduce the FoM of a flash ADC, however it results in increasing the gate delay and decreasing conversion frequency, as shown in Fig. 7. Therefore, we introduced FD product to find the optimum supply voltage [3]. In this case, V_{DD} form 0.6V to 0.8 V gives the optimum supply voltage.

$$FD = FoM \times Delay \quad (5)$$

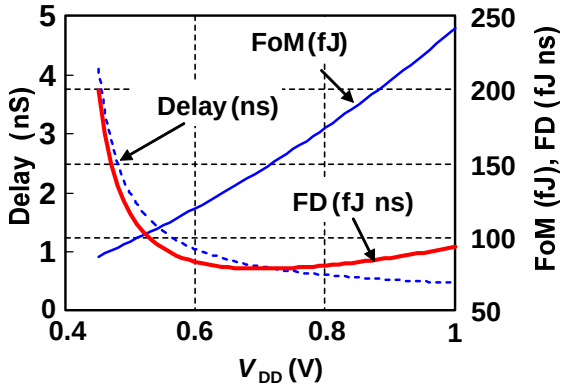

Fig. 7. FoM, delay, and FD vs. V_{DD} for Flash ADC.

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