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A 83-dB SFDR 10-MHz Bandwidth Continuous-Time Delta-Sigma Modulator Employing a One-Element-Shifting Dynamic Element Matching

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SUMMARY This paper considers a simple type of Dynamic Element Matching (DEM), Clocked Averaging (CLA) method referred to as one-element-shifting (OES) and its effectiveness for the implementation of high spurious-free dynamic range (SFDR) multi-bit Delta-Sigma modulators (DSMs). Generic DEM techniques are successful at suppressing the mismatch error and increasing the SFDR of data converters. However, they will induce additional glitch energy in most cases. Some recent DEM methods achieve improvements in minimizing glitch energy but sacrificing their effects in harmonic suppression due to mismatches. OES technique discussed in this paper can suppress the effect of glitch while preserving the reduction of element mismatch effects. Hence, this approach achieves better SFDR performance over the other published DEM methods. With this OES, a 3rd order, 10 MHz bandwidth continuous-time DSM is implemented in 90 nm CMOS process. The measured SFDR attains 83 dB for a 10 MHz bandwidth. The measurement result also shows that OES improves the SFDR by higher than 10 dB.

key words: *delta-sigma modulator, dynamic element matching, glitch energy, mismatch*

1. Introduction

The rapid growth in wireless communication systems has stimulated the development of data conversion interfaces that can be integrated in standard CMOS technologies. For wireless communication applications, such as TV tuner, mobile phone and wireless LAN, analog-to-digital converters (ADCs) with 10 MHz bandwidth are required. Moreover, the reduction of cross-modulation is also needed to improve the quality of communication. This leads to increasing the requirements for the high SFDR ADC design in 10 MHz bandwidth. Among the wide variety of ADC architectures, multi-bit DSMs are the most suitable candidates to meet the needs of high SFDR. The major limitation of DSMs employing multi-bit quantization is the nonlinearity of the internal multi-bit digital-to-analog converter (DAC) caused by mismatch. DEM technique [1] is usually used to reduce the effects of random component mismatches in DAC's. Among the DEM algorithms, data weighted averaging (DWA) is widely used to achieve first-order mismatch shaping but it causes baseband tones for the certain input amplitudes [2], [3]. In recent years, several DWA-like techniques (Bi-DWA, ADWA) [4], [5] have attempted to circumvent the DWA tone problem. However, generic DWA techniques will induce additional glitch energy and decrease the SFDR. In [6], [7], some DEM methods with glitch minimization (Randomized Thermometer Coding (RTC), Random Swapping Thermometer Coding (RSTC)) are introduced, but they are weak in harmonic suppression caused by mismatch. In this work, we discuss a simple type of CLA method referred to as OES [8], [9]. Although CLA has been proposed a long time ago, but its simplicity and effectiveness makes it still attractive and useful in nowadays design, where glitch becomes more critical problem. According to our analysis, OES method can preserve the reduction of element mismatch effects while eliminating the effect of glitch. Hence, a better SFDR can be achieved with the OES method.

This paper is organized as follows: Nonlinear distortion from glitch is described in Sect. 2. In Sect. 3, analysis and verification of OES method are presented. Sections 4, 5 shows the implementation and experimental results of DSM using OES respectively. The conclusions are given in Sect. 6.

2. Nonlinear Distortion by Glitch

Figure 1 shows block schematic of input stage of DSM with internal non-return-to-zero (NRZ) current-steering DAC and its corresponding DAC unity cell. Glitch or spike is generated when the internal DAC output changes from one value to a new value. The major causes for the glitches include signal feedthrough through the gate–drain capacitance, static timing uncertainty between different current cells, and asymmetry up-and-down characteristics for the output [7], as shown in Fig. 1(b). Among these effects, the latest one, non-ideal switching behavior between two consecutive update steps causes the most critical dynamic error which results in degradation of the SFDR [10]. The glitch energy (also called glitch area), a widely used factor to evaluate the effect of the glitch, is defined as the time integral of the analog value of a spike compared with a reference pulse shape [7]. This phenomenon is severe for the high-speed DSM since the glitch area in one sampling period increases with the sampling frequency.

A 3rd-order DSM with a 3-bit quantizer, a 9-level internal current-steering DAC, a 25x OSR, a 10-MHz bandwidth,

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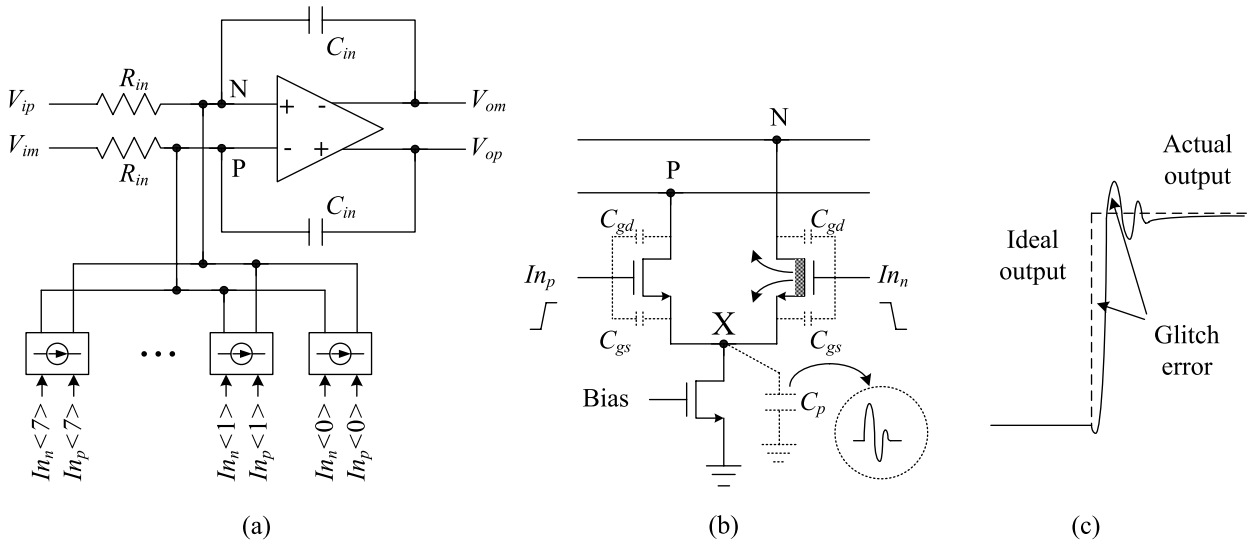

Fig. 1 (a) Block schematic of input stage of DSM with internal non-return-to-zero current-steering DAC, (b) DAC unity cell with nonideal switches, and (c) DAC current waveform.

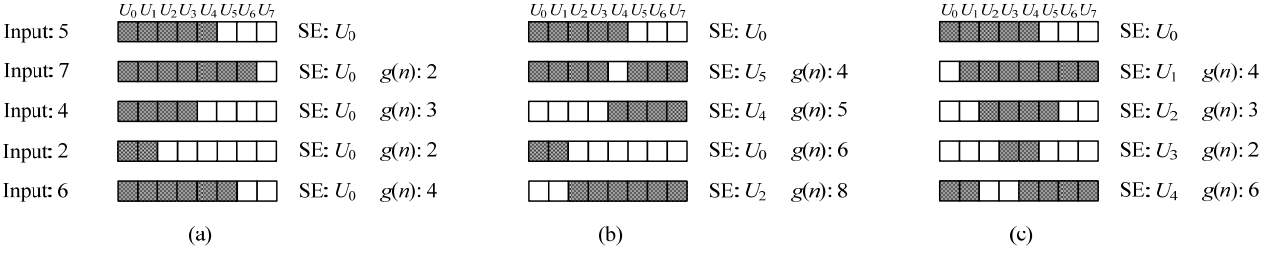

Fig. 2 Example of element selection for (a) conventional thermometer coding, (b) conventional DWA coding and (c) OES.

and a 500-MHz sampling frequency, resulting in an SNDR of 80 dB in the ideal case is used for the analysis in different DEM coding schemes. In order to simplify the algorithm of different DEM coding schemes, only a 9-level DAC are modeled in this analysis, although in real implementation which will be described in Sect. 4, a 17-level DAC are adopted. A non-ideal switching behavior is also modeled to investigate the glitch effect, and it is assumed that all unity cells exhibit exactly the same switching imperfections (no dynamic mismatches). In detail, a 20 ps difference in rise time (and fall time) between inputs of DAC unity cell (In_p and In_n in Fig. 1(b)), i.e 1% of the clock period, is applied. Beside that, C_p is set to 10 fF and for simplification, C_{gd} and C_{gs} will be neglected. This value of C_p is estimated from DAC design where its element mismatch error of current source is suppressed to 1% standard deviation (Sect. 4). Using cascode structure in current source design, this value of C_p will be smaller, but for simplification, 10 fF is chosen and used throughout this paper to examine the effect of glitch.

The glitch energy is proportional to $g(n)$, which is the total number of switched unit current sources for the input from $x(n-1)$ to $x(n)$. Actually, there are two kinds of switching states depending on the previous state of each current cell, i.e. the current cell has been connected to the output node P (or N) before the word transition. However, thanks to differential architecture of DAC and large gain of the integrator (60 dB in this behavior model), the difference between two states can be ignored and the glitch energy can be considered proportional to $g(n)$. Figures 2(a), (b) shows examples of element selection for conventional thermometer coding (TC), conventional DWA coding, respectively. For conventional TC, starting element (SE) of the subsequent selection cycle is unchanged all the time, so $g(n)$ can be expressed briefly as follows:

$$g(n) = |x(n) - x(n-1)| \tag{1}$$

On the other hand, SE of conventional DWA is updated for each selection cycle and $g(n)$ can be obtained as follows:

$$g(n) = \begin{cases} x(n)+x(n-1), x(n)+x(n-1) \le N \\ 2N-x(n)-x(n-1), x(n)+x(n-1) > N \end{cases} \tag{2}$$

where N is the number of DAC element. According to Eqs. (1) and (2), a much larger number of switched unit current sources, as well as glitch energy, can be predicted when DWA is used. In [6], [7], some DEM methods with glitch minimization (RTC, RSTC) are introduced. RSTC

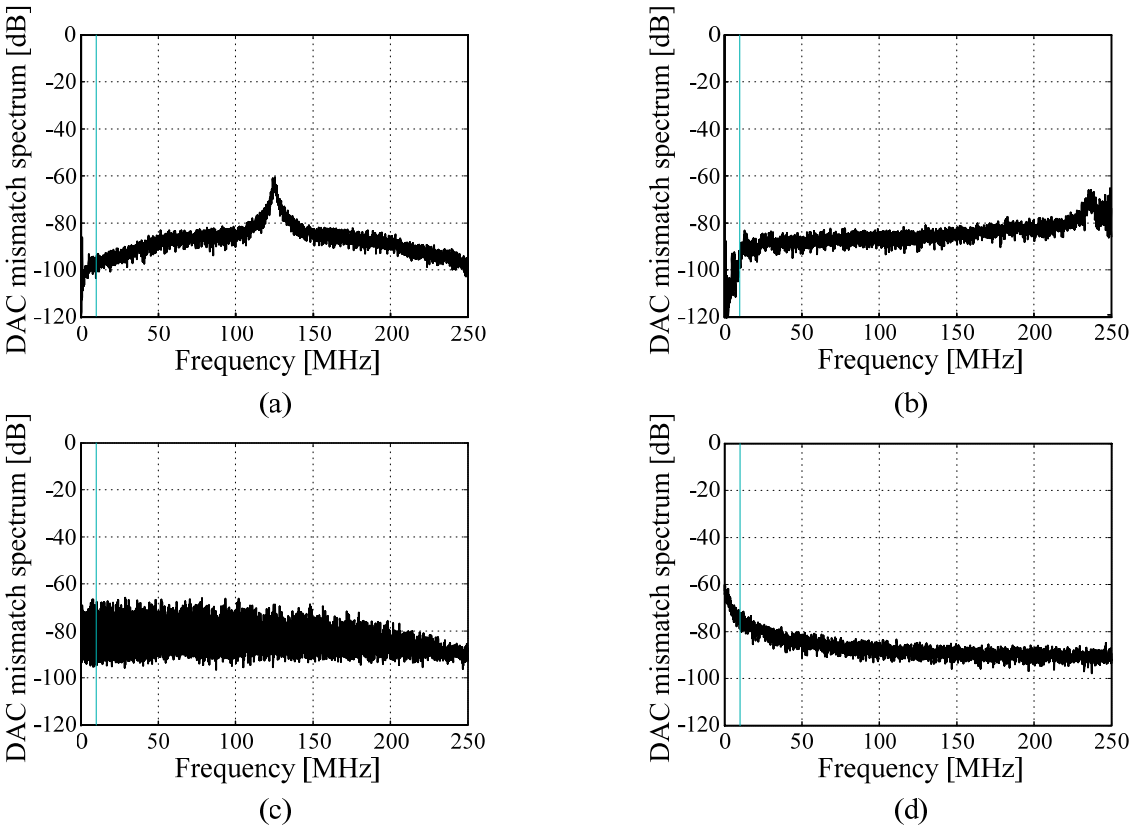

Fig. 3 DAC mismatch spectra of DSM at −30 dB, 1 MHz input employing (a) Bi-DWA. (b) ADWA. (c) RTC. (d) RSTC.

method is successful in keeping $g(n)$ as small as conventional TC, but their weak harmonic suppression ability to the mismatch is a draw back. This conclusion can be verified by using the DAC mismatch spectra for an input level of −30 dB, frequency of 1 MHz with a 1% standard deviation of element mismatch error in internal DAC, as shown in Fig. 3. This figure is obtained by averaging the results of 10-time simulation, with 8192 points per run. For DWA groups (Bi-DWA, ADWA), the first-order mismatch shaping is preserved while the DAC mismatch tones can be shifted away from $f_s/2$, as shown in Figs. 3(a), (b), where f_s is the sampling frequency. On the other hand, for the RTC and RSTC method in Figs. 3(c), (d), the noise floor in the interesting bandwidth of the modulator is raising, especially for the RSTC. Hence, a large degradation in SNDR when applied these coding methods to the DSM can be predicted. Simulation results show that an average of 13 dB (for RTC) and 22 dB (for RSTC) degradation in SNDR compared to DWA groups are obtained respectively when the element mismatch error with a 1% standard deviation is applied to the DAC. This DSM with an ideal internal DAC shows no obvious baseband tones in the modulator output. Hence, it can be assumed that any baseband tones in the DSM output, with a nonideal DAC, are generated by DAC noise due to element mismatch. The degradation of RTC and RSTC method can be understood because they were firstly proposed for DAC operating at Nyquist frequency, and not suitable for the oversampling operation.

The OES method [8], [9] discussed in this paper can overcome these problems. It can preserve the reduction of element mismatch effects while eliminating the effect of glitch by keeping $g(n)$ as small as possible. Detailed analysis and verification will be explained in the next section.

3. Analysis and Verification of OES Method

3.1 Operation Principle of OES Method

Figure 2(c) shows the element sequence in a 3-bit DAC example using OES coding method. In OES, SE of the subsequent selection cycle is determined by advancing a fixed one step from the SE of the previous selection cycle. Its operation is demonstrated using the DAC input codes 5, 7, 2, 4 and 6, as shown in Fig. 2(c). An initial input of 5, the SE is U_0, and the elements $\{U_0, U_1, U_2, U_3, U_4\}$ are selected. For the second input of 7, the SE is advanced from U_0 to U_1, i.e., the elements $\{U_1, U_2, U_3, U_4, U_5, U_6, U_7\}$ are selected. For the following inputs, the SE is advanced regularly by one for each selection cycle, and the elements are selected similarly.

3.2 Eliminate Effect of Glitch

From Fig. 2(c), the number of switched unit current sources

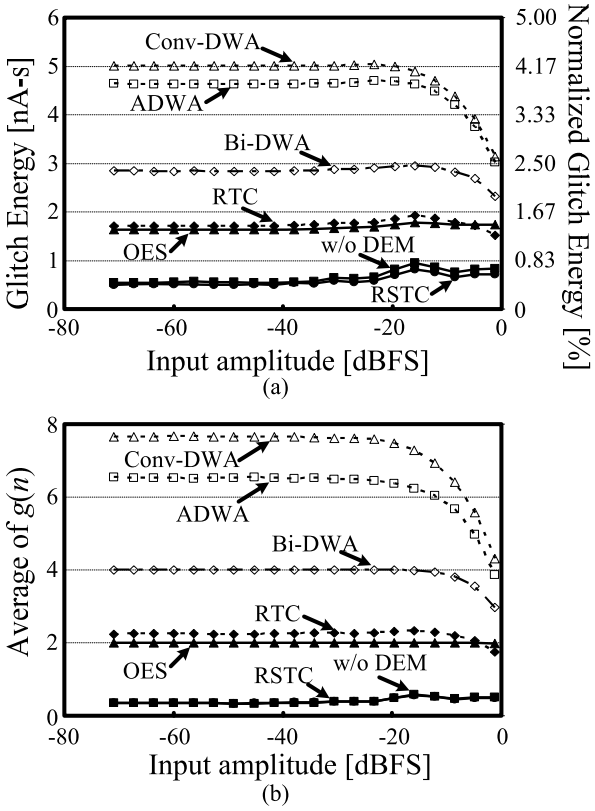

Fig. 4 (a) Glitch energy of internal 3-bit DACs in DSM with different coding schemes for different input level. (b) Its corresponding number of switched element.

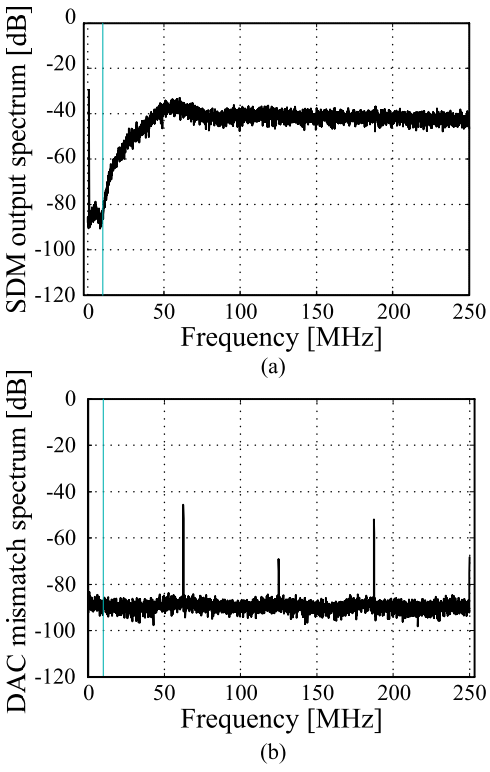

Fig. 5 (a) Output spectrum of DSM employing OES for input level of −30 dB, frequency of 1 MHz. (b) Its corresponding DAC mismatch spectrum.

$g(n)$ can be obtained as follows:

$$g(n) = \begin{cases} 2 + x(n) - x(n-1), x(n) \geq x(n-1) \\ |x(n) - x(n-1)|\,, x(n) < x(n-1) \end{cases} \quad (3)$$

For $x(n) < x(n-1)$, OES has the same value of $g(n)$ compared to conventional TC method. In DSM with a certain input (DC or a sinusoidal input), value of $x(n)-x(n-1)$ is usually belongs to $\{-1, 0, 1\}$, Eq. (3) can be expressed equally to

$$g(n) = 2 + x(n) - x(n-1) \quad (4)$$

Figure 4(a) shows glitch energy of internal 3-bit DAC in DSM with different coding schemes for different input level, and Fig. 4(b) shows its corresponding number of switched element. The glitch model and simulation conditions are described in Sect. 2. With 2^{13} samples per run, the glitch energy and its corresponding number of switched element are calculated by averaging the results of $2^{13}-1$ code transitions instead of the midcode transition only. According to Eq. (4), it can be understood that the average of $g(n)$ in OES is about 2 over the full range of input signal amplitudes in Fig. 4(b). The characteristic of the number of switched element in DWA groups also shows good agreement with (2) and can be explained as follows: For small input signals modulator output mostly consists of code 3, 4, and 5 with code 4 having the highest density. As a result, the higher average of $g(n)$ can be obtained. When the input signal increases, the other codes will appear and according to Eq. (2), the existence of the lower value of $g(n)$ will reduce the average value of $g(n)$.

Glitch energy shows good agreement with the number of switched element. From Fig. 4 it can be noticed that, OES shows smaller glitch energy compared with other DEM structures except the RSTC and conventional TC (without DEM) method.

3.3 Preserve Reduction of Element Mismatch Effect

Figure 5(a) shows the output spectrum of the DSM employing the OES for an input level of −30 dB with a 1% standard deviation of element mismatch error in internal DAC, and Fig. 5(b) shows the corresponding DAC mismatch spectrum. These figures are also obtained by averaging the results of 10-time simulation, with 8192 points per run. As shown in Fig. 5(b), large tones are observable at $f_s/8$, where f_s is the sampling frequency, and can be explained as followed. According to the characteristic of OES method, starting element will be re-chosen after 8 clock cycles, independent on the input DAC value. Compared with the DWA case where the first tone was at $f_s/2$ and caused aliasing, in this case, only the fourth harmonic is at $f_s/2$ and the aliasing caused by $f_s/2$ will be smaller. It is required that DAC error tones should not be allowed in the vicinity of the baseband, and considering a two times margin, the *OSR* should satisfy the condition $OSR > 8$. For the common case, $OSR > N$, where N is the number of DAC element. These discussions about

tones can also be found in [8], [9].

These characteristics can be realized more clearly by obtaining the DAC noise function of OES method. According to [3], the error due to mismatch can be expressed as

$$y_{mis} = \sum_{i=0}^{N-1} d_i \cdot (w_i - w_{mean}) \tag{5}$$

where w_i is the weight of the i-th cell relative to its nominal value, d_i is its control signal and w_{mean} is the average weight for the cells of the array. The mismatch error at time k is given by

$$y_{mis}(k) = \sum_{i=start(k)}^{stop(k)-1} w_i - x(k)w_{mean} \tag{6}$$

where $stop(k) = start(k) + x(k)$, $x(k)$ is the input code of the DAC at time k, and $0 \le start(k), stop(k) < N$ is the pointer containing the address of one cell of the array. For simplification, only the case $stop(k) \ge start(k)$ is considered. In conventional DWA method, $start(k) = stop(k-1)$ and the DAC noise can be shown to be a function of the $IM(stop(k))$ in Z-domain [3]

$$Y_{mis-DWA}(z) = \left(1 - z^{-1}\right) IM(STOP(z)) \tag{7}$$

In OES method, $start(k) = start(k-1) + 1$. Hence, N clock before, the mismatch error at time $k - N$ will be estimated as

$$y_{mis}(k-N) = \sum_{i=start(k-N)}^{stop(k-N)-1} w_i - x(k-N)w_{mean} \tag{8}$$

Because $start(k-N) = start(k)$ in OES method, therefore

$$y_{mis}(k) - y_{mis}(k-N) = \sum_{i=stop(k-N)}^{stop(k)-1} w_i - [x(k) - x(k-N)]\, w_{mean} \tag{9}$$

can be derived. The right hand of Eq. (9) can be considered as a modified version of Eq. (6) with the input code will be $x(k) - x(k-N)$ instead of $x(k)$. Equation (9) can be rewritten in the Z-domain into the form

$$Y_{mis-OES}(z) = \frac{1}{(1 - z^{-N})} Y_{mis-\text{modified}}(z) \tag{10}$$

From Eq. (10), it can be realized that the DAC noise function of OES method will be affected by a function $1/(1 - z^{-N})$. Figure 6 shows an example plot of this function in case N is 8 and the sampling frequency is 500 MHz. Figure 6 shows good agreement with Fig. 5(b), where large tones at times of $f_s/8$ and noise-floor increasing in the interesting band can be observed. Because of this increasing noise floor, the degradation of SNDR can be predicted.

Simulation results show that the degradation in SNDR compared to DWA groups is within 6 dB over the full range of input signal amplitudes. This value is 13 dB for RTC and 22 dB for RSTC respectively as explained in above section. Therefore, it is proven that OES method can preserve the reduction of element mismatch effects while eliminating the effect of glitch.

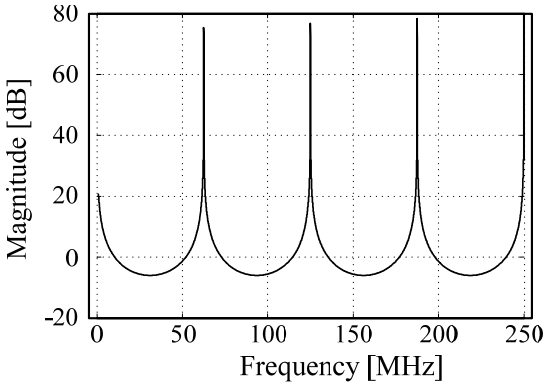

Fig. 6 Response of function $1/(1 - z^{-8})$ with $f_s = 500$ MHz.

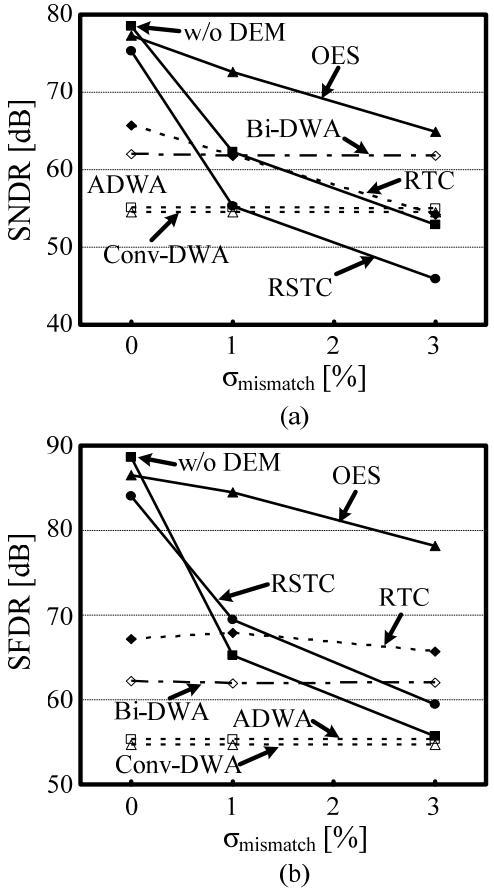

Fig. 7 Simulated (a) SNDR and (b) SFDR with effect of glitch and different mismatch level.

3.4 With Both of Glitch and Element Mismatch Effect

Figure 7 shows simulated SNDR and SFDR with both of glitch and element mismatch effect. The glitch model and simulation conditions are described in Sect. 2. These figures are also obtained by averaging the results of 10-time simula-

tion per mismatch. For small mismatch, RSTC and conventional TC (without DEM) show good performance on SNDR and SFDR but they degrade rapidly when the mismatch increases. In spite of that, the OES method always achieves better SNDR and SFDR performance over the other DEM structures. On average, a 10 dB SFDR improvement can be achieved by the OES technique.

4. Circuit Implementation Details

4.1 Loop Filter

In Sect. 3, OES method shows its effectiveness compared to the other coding schemes. A 3rd order, 10 MHz bandwidth and a 500 MHz sampling frequency continuous-time DSM using OES is implemented in 90 nm CMOS process. The modulator architecture is shown in Fig. 8. In order to maintain a good alias filter characteristic, a combination of feedforward and feedback stabilized loop filter is implemented [11]. Excess loop delay up to one clock is compensated using the method described in [11] to relax the sum circuit before the quantizer.

Amplifiers are the most critical circuits which consume most of the power in the DSM. The whole architecture was simulated at system level to achieve the required stability and SNDR with minimum gain-bandwidth (GBW) and DC-gain of the amplifiers. Two-stage amplifiers with folded-cascode PMOS input stage shown in Fig. 9 are employed to guarantee the output swing. A 67 dB DC-gain, 500 MHz GBW opamp is used in the first integrator. The three opamps of the loop filter reveal a power-drain of 4.7 mW in total.

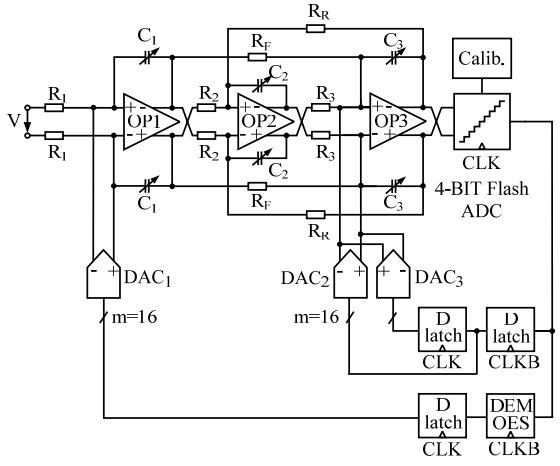

Fig. 8 3rd order, 4-bit ΔΣ modulator.

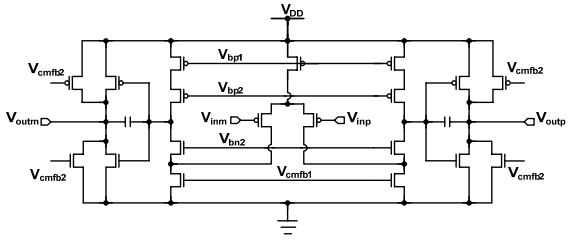

Fig. 9 Simplified schematic of the two-stage opamp.

4.2 Quantizer, DAC and DEM

The quantizer in the DSM consists of a reference ladder and a 4-bit flash ADC with a thermometer-coded output. The 16 comparators of the internal flash ADC are realized with a modified version of double tail latch [12] and a SR latch, shown in Fig. 10. Moreover, capacitive offset calibration circuits are also included in our design.

From Fig. 8, DAC1 realizes an input to the loop filter and, hence, has the highest requirements on linearity and noise performance, which requires a large device size to get the necessary matching and flicker noise performance.

As any nonidealities of DAC2 and DAC3 are suppressed by the gain of the first two integrators, the requirements on noise and linearity can be relaxed. Therefore, OES-DEM method is applied to DAC1 only. Moreover, thanks to one clock compensation of excess loop delay, timing requirement for the OES can be relaxed. All DACs are cascoded to increase their output resistance and shield the large drain capacitance of the current-source transistors from the tail node of the switches. The OES can be implemented with no extra hardware cost, because no extra pointer or extra random number generator is needed. Hence, the shorter extra DEM delay will be added to the modulator as expectation, and is suitable for high speed operation. The block diagram of OES is shown in Fig. 11. Thanks to OES, the element mismatch error of DAC1 can be relaxed to 1% standard deviation compared to 0.1% when no DEM is used.

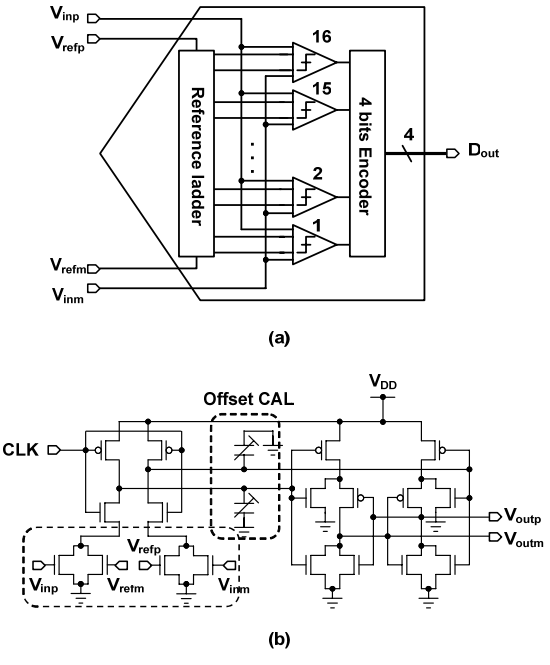

Fig. 10 (a) Four-bit quantizer, and (b) Double-tail latch comparator.

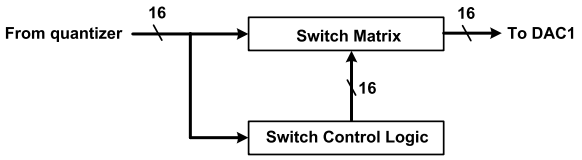

Fig. 11 Block diagram of OES.

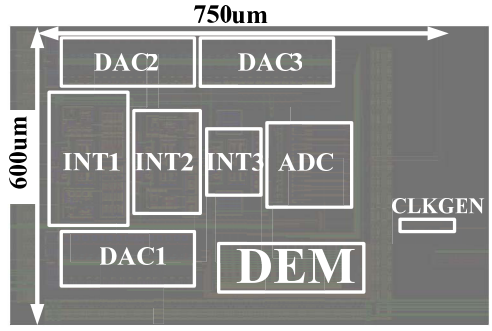

Fig. 12 Chip layout.

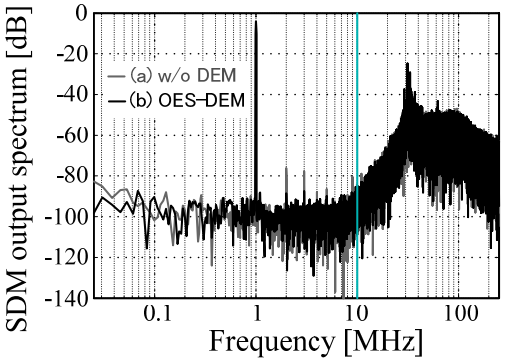

Fig. 13 Measured output spectrum of DSM with (a) w/o DEM, and (b) OES method.

5. Measurement Results

The chip was fabricated in a standard digital 90-nm CMOS technology. The power supply voltage and the common-mode input voltage were 1.2 V and 0.6 V, respectively. The maximum amplitude of the input signal (full-scale) was 0.6 V. The chip core size was 750 μm×600 μm, as illustrated in Fig. 12.

Figure 13 shows the DSM output spectrum using a Hanning windowed 65536 point FFT at 1 MHz input with no DEM and the OES method enabled respectively. The measured SFDR exceeds 83 dB for a 10 MHz bandwidth, a 10 dB improvement is obtained when compared to without DEM. The measured SNDR and SFDR for different input frequency are plotted in Fig. 14. From Fig. 14, it is noticed that an 8 dB improvement of SFDR is still achieved using OES DEM at 3 MHz input frequency. Moreover, the measurement results using two-tone method are also included, as shown in Figs. 15 and 16. An average of 4 dB IMD3 improvement can be observed when OES DEM is used according to Fig. 16. The degradation of SFDR at 3 MHz input can be explained by non-linearity of opamp, not by the OES method. The same tendency of simulation results was obtained when non-linearity behavior of opamp was modeled, with assuming that the gain of opamp at full-scale output swing drops down from DC gain (for example 5 dB) and other circuit blocks were ideal. The OES DEM occupied 9% of the core area and consumed 6% of the core power consumption. The measurement results are summarized in Table 1, and the comparison of modulator discussed in this work and other state-of-the-art converters is also included

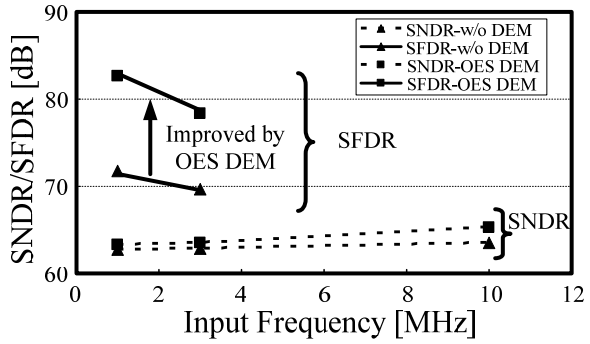

Fig. 14 Measured SNDR/SFDR with w/o DEM, and OES method.

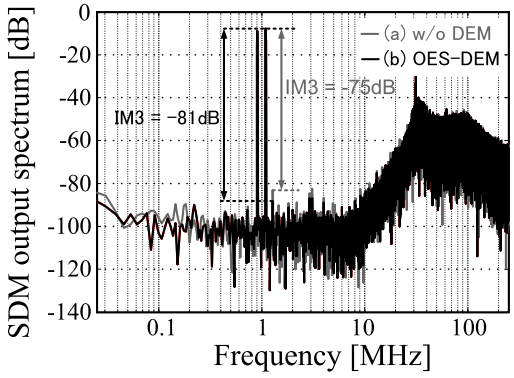

Fig. 15 Measured output spectrum of DSM using two-tone input with (a) w/o DEM, and (b) OES method.

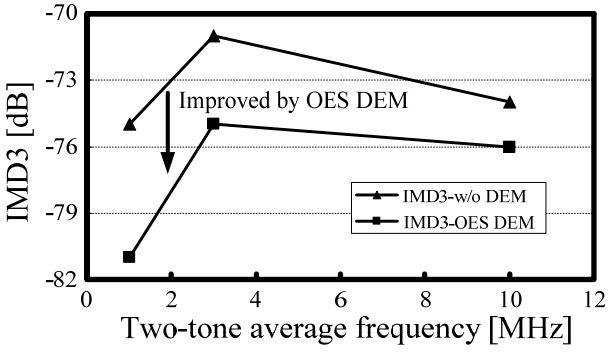

Fig. 16 Measured IMD3 versus average frequency of two-tone input with w/o DEM, and OES method.

Table 1 Comparison with state-of-the-art DSM.

	Unit	This work	ISCAS 2011 [13]	ASSCC 2010 [14]	CICC 2010 [15]	JSSCC 2010 [16]	ESSCIRC 2010 [17]	VLSI 2009 [18]	VLSI 2009 [19]
Type/ DEM		CT/OES	DT/DWA	CT/DWA	CT/DWA-Dither	DT/DEM**	DT/DEM**	CT/DWA	CT/1b Quan.
Bandwidth	MHz	10	6.25	20	4	5	10	10	10
Sampling frequency	MHz	500	100	640	140	80	240	300	640
SFDR	dB	**83**	74.5*	77*	82.5	85	84.8*	64*	72
SNDR	dB	65	63.7	63.9	69.8	75.4	66	62.5	65
Dynamic Range	dB	66	-	68	-	-	71	70.2	67
Power consumption	mW	**15.7**	52.2	58	3.6	36	20.2	5.31	6.8
CMOS process	nm	90	130	130	65	180	130	110	90
Figure of Merit	fJ/conv	**530**	3300	1130	180	750	600	240	240

* Graphically estimated, ** No detail

to value the effectiveness of DEM method. Figure of Merit (*FoM*) is defined by the following equation

$$FoM = \frac{P}{2 \cdot BW \cdot 2^{ENOB}} \tag{11}$$

where P is power consumption, BW is bandwidth and $ENOB$ is effective number of bit of the modulator [11]. According to Table 1, because of using only 1bit quantizer, it is difficult to achieve high SFDR in [19]. Our discussed OES shows better SFDR compared with conventional DEM method using in [13], [14], [18]. Moreover, with the almost same SFDR, our modulator consumes less power than [16], [17]. Hence, it is proven that the OES technique employed in this design is a very effective means for obtaining a high SFDR with lower power consumption and hardware cost thanks to its simplicity.

6. Conclusion

A simple type of CLA, OES DEM method has been discussed in this paper. The simulation and measurement results show that the OES substantially suppresses the both effects of the mismatch and glitch. Although OES has been proposed a long time ago, but its simplicity and effectiveness makes it still attractive and prefer for cost and power considerations, and is good enough for almost all the applications.

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References

[1] R.J. van de Plassche, "Dynamic element matching for high accuracy monolithic D/A converters," IEEE J. Solid-State Circuits, vol.SC-11, no.6, pp.795–800, Dec. 1976.

[2] R.T. Baird and T.S. Fiez, "Linearity enhancement of multibit ΔΣ A/D and D/A converters using data weighted averaging," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol.42, no.12, pp.753–762, Dec. 1995.

[3] O.J.A.P. Nys and R.K. Henderson, "An analysis of dynamic element matching techniques in sigma-delta modulation," IEEE Proc. ISCAS'96, pp.231–234, May 1996.

[4] I. Fujimori, L. Longo, A. Hairapetian, K. Seiyama, S. Kosic, J. Cao, and S.L. Chan, "A 90-dB SNR 2.5-MHz output-rate ADC using cascaded multibit delta-sigma modulation at 8X oversampling ratio," IEEE J. Solid-State Circuits, vol.35, no.12, pp.1820–1828, Dec. 2000.

[5] D.H. Lee and T.H. Kuo, "Advancing data weighted averaging technique for multi-bit sigma-delta modulators," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol.54, no.10, pp.838–842, Oct. 2007.

[6] D.H. Lee, T.H. Kuo, and K.L. Wen, "Low-cost 14-bit current-steering DAC with a randomized thermometer-coding method," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol.56, no.2, pp.137–141, Feb. 2009.

[7] M.H. Shen, J.H. Tsai, and P.C. Huang, "Random swapping dynamic element matching technique for glitch energy minimization in current-steering DAC," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol.57, no.5, pp.369–373, May 2010.

[8] S.R. Norsworthy, R. Schreier, and G.C. Temes, Delta-Sigma Data Converters, Theory, Design, and Simulation, IEEE Press, 8.3.3.2, 1997.

[9] Y. Geerts, M. Steyaert, and W. Sansen, Design of Multi-bit Delta-Sigma A/D Converters, Kluwer Academic Publishers, 2.6.4.2, 2003.

[10] A.V. Bosh, M. Borremans, M. Steyaert, and W. Sansen, "A 12b 500 Msamples/s current-steering CMOS D/A converter," Proc. IEEE 2001 ISSCC, vol.XLIV, pp.366–367, Feb. 2001.

[11] G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, and E. Romani, "A 20-mW 640-MHz CMOS continuous-time ΣΔ ADC with 20-MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB," IEEE J. Solid-State Circuits, vol.41, no.12, pp.2641–2649, Dec. 2006.

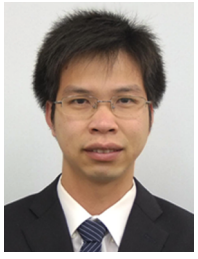
[12] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," ASSCC Dig. Tech. Papers, pp.269–272, Nov. 2008.

[13] C.S. Shin, M.H. Yoon, K.I. Cho, Y.J. Kim, K.S. Kim, S.H. Lee, and G.C. Ahn, "A 6.25 MHz BW 8-OSR fifth-order single-stage sigma-delta ADC," IEEE Symp. on Circuits and Systems, pp.1117–1120, May 2011.

[14] J.G. Jo, J. Noh, and C. Yoo, "A 20 MHz bandwidth continuous-time ΣΔ modulator with jitter immunity improved full-clock period SCR (FSCR) DAC and high speed DWA," ASSCC Dig. Tech. Papers, pp.1–4, Nov. 2010.

[15] K. Matsukawa, Y. Mitani, M. Takayama, K. Obata, Y. Tokunaga, S. Sakiyama, and S. Dosho, "A 69.8 dB SNDR 3rd-order continuous time delta-sigma modulator with an ultimate low power tuning system for a worldwide digital TV-receiver," IEEE Custom Integrated

Circuits Conference, pp.1–4, June 2009.
[16] O. Rajaee, T. Musah, N. Maghari, S. Takeuchi, M. Aniya, K. Hamashita, and U.K. Moon, "Design of a 79 dB 80 MHz 8X-OSR hybrid delta-sigma pipelined ADC," IEEE J. Solid-State Circuits, vol.45, no.4, pp.719–730, April 2010.
[17] T. Christen and Q. Huang, "A 0.13 μm CMOS 0.1–20 MHz bandwidth 86–70 dB DR multi-mode DT $\Delta\Sigma$ ADC for IMT-advanced," ESSCIRC Dig. Tech. Papers, pp.414–417, Sept. 2010.
[18] K. Matsukawa, Y. Mitani, M. Takayama, K. Obata, S. Dosho, and A. Matsuzawa, "A 5th-order delta-sigma modulator with single-opamp resonator," IEEE Symp. on VLSI Circuits, pp.68–69, June 2009.
[19] P. Crombez, G. Van der Plas, M. Steyaert, and J. Craninckx, "A 500 kHz–10 MHz multimode power-performance scalable 83-to-67 dB DR CT$\Delta\Sigma$ in 90 nm digital CMOS with flexible analog core circuitry," IEEE Symp. on VLSI Circuits, pp.70–71, June 2009.



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