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PAPER Special Section on Analog Circuit Techniques and Related Topics

An Analysis on a Dynamic Amplifier and Calibration Methods for a Pseudo-Differential Dynamic Comparator

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SUMMARY This paper analyzes a pseudo-differential dynamic comparator with a dynamic pre-amplifier. The transient gain of a dynamic pre-amplifier is derived and applied to equations of the thermal noise and the regeneration time of a comparator. This analysis enhances understanding of the roles of transistor's parameters in pre-amplifier's gain. Based on the calculated gain, two calibration methods are also analyzed. One is calibration of a load capacitance and the other is calibration of a bypass current. The analysis helps designers' estimation for the accuracy of calibration, dead-zone of a comparator with a calibration circuit, and the influence of PVT variation. The analyzed comparator uses 90-nm CMOS technology as an example and each estimation is compared with simulation results.

key words: *dynamic amplifier, dynamic comparator, load capacitance, bypass current, calibration, and PVT variation*

1. Introduction

ADCs are necessary components for baseband systems and have been mainly studied to reduce their FoMs, which are one of evaluation indices. Many researches on reducing FoM — decreasing power consumption, accomplishing high conversion frequency, and increasing resolution — of an ADC have been presented [1]. Low FoM can be easily obtained by low power consumption. In order to get low power consumption, some parts, especially an operational amplifier in conventional ADCs, have been removed. Current ADCs have more simple structures, thus power consumption of ADCs has been reduced only to satisfy physical limits [2].

A comparator is the essential building block in an ADC to convert an analog signal into a digital signal. To suppress its power dissipation, recently published researches have used dynamic comparators [3]–[5]. Since current flows only when they are triggered, they are more power efficient than comparators dissipating static current. When a comparator is as accurate as an ideal comparator which means no mismatch, there is no need to implement an amplifier in front of a comparator and power consumption would be close to the lower boundary satisfying thermal noise condition. However, mismatch always exists in an actual comparator and offset voltage occurs. One of the methods to reducing mismatch is to make a transistor large [6]. This method increases parasitic capacitance and power consumption, which is proportional to load capacitance. To suppress mismatch and power consumption, calibration methods were proposed for dynamic comparators [4], [5]. However, this topology, an inverter chain, has deficiency, because, regeneration depends on the gain of an inverter — or the intrinsic gain of a transistor —, and as process is scaled down, its accuracy will become worse.

To address this issue, a latch with a dynamic amplifier, whose gain is approximately 5 times in 65-nm process [7], is proposed by D. Schinkel, et al. in 2007 [8]. This is called a double-tail latch-type comparator, which attained high accuracy with low power. However, this requires two phase of latching clocks. In 2008, We proposed a modified version of the double-tail latch-type comparator [9]. We removed the tail current of the second stage, which was triggered by inverse phase of a latching clock, and generated a trigger signal by using the outputs of a pre-amplifier. This modification can suppress the influence of skew between two phases of latching clocks [9] and guarantees the second stage is turned on after the output of a pre-amplifier reaches certain voltage. However, both comparators suffer kick-back noise. To suppress the kick-back noise, in 2010, a pseudo-differential topology was introduced [10].

Those comparators with calibration circuits should be analyzed for their characteristics and optimizations. Thermal noise [7], [11]–[15] and mismatch [16] analysis methods about a dynamic comparator were already reported. In this paper, calibration methods for the pseudo-differential dynamic comparator will be analyzed in 90-nm process. The gain of a dynamic amplifier will also be deduced for this analysis. This paper is organized as follows: Sect. 2 analyzes the general characteristic of a dynamic amplifier and a pseudo-differential dynamic comparator. Section 3 and Sect. 4 analyze two conventional calibration methods of a load capacitance and a bypass current. Two calibration methods will be compared in Sect. 5 and the analysis will be concluded in Sect. 6.

2. Comparator under Analysis

Pseudo-differential dynamic comparator will be briefly analyzed in this section. Its schematic is described in Fig. 1. This comparator is comprised of two stages. The first stage is a dynamic amplifier, or a pre-amplifier, which integrates differential input signals as time passes. The second stage actually performs the regeneration. In this paper, the aspect ratio of all transistors are designed as $2\,\mu$m/100 nm.

Before analyzing the comparator, we describe its tran-

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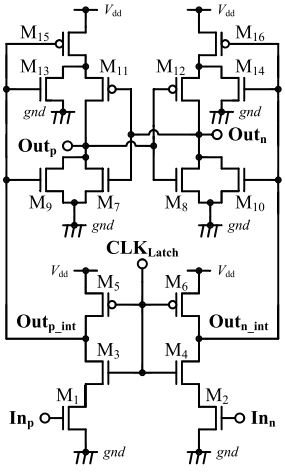

Fig. 1 Pseudo-differential dynamic comparator [10].

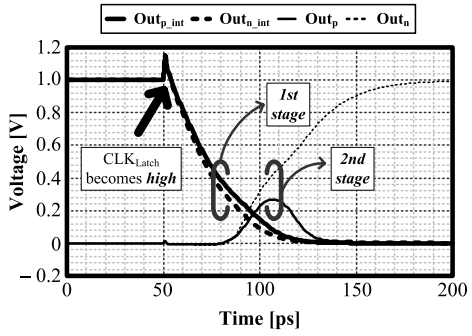

Fig. 2 Transient waveform of the comparator from simulation results (V_{dd} = 1.0 V and V_{in_com} = 0.5 V).

sient performance. As shown in Fig. 2, when CLK_{Latch} is low, M_5 and M_6 are on while M_3 and M_4 are off. Here, V_{dd} means a supply voltage and V_{in_com} is an input common-mode voltage. Then, parasitic capacitors on nodes Out_{p_int} and Out_{n_int} are charged up to supply voltage. The second stage is turned off, because M_{15} and M_{16} are off. After CLK_{Latch} becomes high, M_3 and M_4 are on; while M_5 and M_6 are off. Accordingly, electric charge on the node Out_{p_int} and Out_{n_int} flows into *gnd*. Drain currents of M_3 and M_4 are determined by input signals of M_1 and M_2. Differences of flowing electric charge per time at the nodes Out_{p_int} and Out_{n_int} induce a voltage difference at the nodes, and the voltage difference becomes larger as time passes. If voltages on the node Out_{p_int} and Out_{n_int} drop sufficiently, then the second stage regenerates the voltage difference between node Out_{p_int} and Out_{n_int}.

Before we address the performance of the comparator, we presume that rising time of CLK_{Latch} is very short and transistors of M_3 and M_4 are in the deep triode region when CLK_{Latch} is high. In actual case, it may be too difficult to sharpen the slew-rate of CLK_{Latch}. When the slew-rate of CLK_{Latch} isn't sufficiently larger than the slew-rate of a pre-amplifier, the drain current of M_1 (or M_2) starts to flow and output voltage of a pre-amplifier drops before CLK_{Latch} reaches the supply voltage. And M_3 (or M_4) is first in the saturation region and goes to the deep triode region as the drain current of M_1 (or M_2) flows down. However, to simplify the analysis, we set the rising time of CLK_{Latch} to 1 ps as the simulation condition and M_3 and M_4 are in the deep triode region when CLK_{Latch} is high.

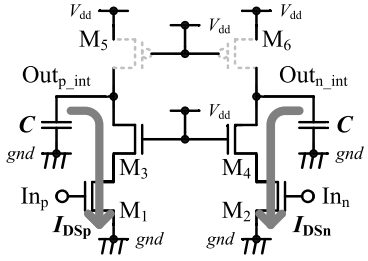

Fig. 3 Simplified schematic of a dynamic amplifier when the CLK_{Latch} is high.

2.1 Gain of Dynamic Amplifier

Pre-amplifier increases the difference between the differential input signals. To figure out its gain, G_{amp}, let us simplify the first stage of dynamic comparator when CLK_{Latch} is high as depicted in Fig. 3. The output of a pre-amplifier is described as below;

$$V_{out\_int} = V_{dd} - \frac{I_{DS}}{C}t \tag{1}$$

where I_{DS} is a drain current of the input transistors, C is a total load capacitance on its output node, and t is a integration time. When there is no additional capacitor on the output node, C equals to C_{PS}, a parasitic capacitance induced by transistors connected to the node. Ideally, when a transistor is in the saturation region, I_{DS} follows the square-law as shown in Eq. (2);

$$I_{DS\_ideal} = \frac{1}{2}\mu C_{OX}\frac{W}{L} \times V_{eff}^2 \tag{2}$$

$$V_{eff} \equiv V_{GS} - V_{th} \tag{3}$$

where μ is a mobility of charge carriers, C_{OX} is a gate oxide capacitance per unit area, W is a channel width, L is a channel length, V_{GS} is a gate-source voltage, and V_{th} is a threshold voltage. However, as process is scaled down, I_{DS} no longer follows Eq. (2). One of the reasons could be channel-length modulation [6]. When we consider channel-length modulation, Eq. (2) is modified as below;

$$I_{DS} = \frac{1}{2}\mu C_{OX}\frac{W}{L}V_{eff}^2\left(1 + \lambda\left(V_{DS} - V_{DS\_sat}\right)\right) \tag{4}$$

where V_{DS} means a drain-source voltage, V_{DS_sat} is a saturation condition of drain-source voltage, which equals V_{eff}, and λ indicates a channel-length modulation coefficient. Figure 4 shows the influence of channel-length modulation. When M_3 (or M_4) is in the deep triode region, V_{out_int} which is a voltage of node Out_{int} can be approximated as the drain voltage of M_1 (or M_2). When V_{out_int} is decreased from V_{dd} to V_{DS}, an average drain current, I_{DS}, is expressed as below;

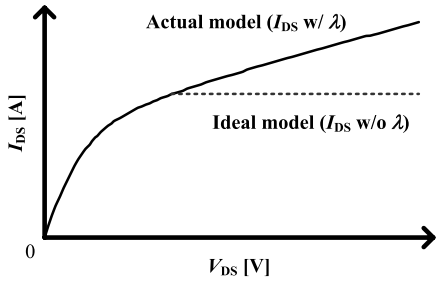

Fig. 4 Influence of channel-length modulation.

$$\overline{I_{\mathrm{DS}}} = \frac{1}{V_{\mathrm{dd}} - V_{\mathrm{DS}}} \int_{V_{\mathrm{DS}}}^{V_{\mathrm{dd}}} I_{\mathrm{DS}} dV_{\mathrm{DS}} = I_{\mathrm{DS\_ideal}} \times \left(1 + \frac{\lambda}{2}\left(V_{\mathrm{dd}} + V_{\mathrm{DS}} - 2\,V_{\mathrm{eff}}\right)\right). \quad (5)$$

Substituting Eq. (5) into Eq. (1), then the integration time can be represented as;

$$t = \frac{(V_{\mathrm{dd}} - V_{\mathrm{DS}})\,C}{\overline{I_{\mathrm{DS}}}}. \quad (6)$$

Based on the above equations, the gain of pre-amplifier is deduced. From Eq. (4), a transconductance, g_{m}, and a signal current due to g_{m}, i_{DS1}, are expressed as below;

$$g_{\mathrm{m}} = \mu C_{\mathrm{OX}} \frac{W}{L} V_{\mathrm{eff}} \left(1 + \lambda \left(V_{\mathrm{DS}} - V_{\mathrm{DS\_sat}}\right)\right) \quad (7)$$

$$i_{\mathrm{DS1}} = g_{\mathrm{m}} v_{\mathrm{in}} \quad (8)$$

where v_{in} is an input signal. As described in Eq. (8), g_{m} amplifies input signal.

However, there is one more factor affecting the gain of pre-amplifier, which is λ representing the influence of channel-length modulation. From Eq. (4), an output conductance, g_{DS}, and a signal current due to g_{DS}, i_{DS2}, are expressed as below;

$$g_{\mathrm{DS}} = \frac{1}{2} \mu C_{\mathrm{OX}} \frac{W}{L} V_{\mathrm{eff}}^2 \lambda \quad (9)$$

$$i_{\mathrm{DS2}} = g_{\mathrm{DS}} v_{\mathrm{out}} \quad (10)$$

where v_{out} is an output signal integrated on a load capacitor. Substituting Eqs. (5) and (6) into Eq. (1), then an output differential signal, $v_{\mathrm{out\_diff}}$, of a pre-amplifier is deduced;

$$v_{\mathrm{out\_diff}} \equiv V_{\mathrm{outp\_int}}(t) - V_{\mathrm{outn\_int}}(t) = -\frac{2\,(V_{\mathrm{dd}} - V_{\mathrm{DS}})}{V_{\mathrm{eff}}} v_{\mathrm{in\_diff}} \quad (11)$$

where $v_{\mathrm{in\_diff}}$ is an input differential signal, $2v_{\mathrm{in}}$. Substituting Eq. (11) into Eq. (10), then

$$i_{\mathrm{DS2}} = -g_{\mathrm{DS}} \frac{2\,(V_{\mathrm{dd}} - V_{\mathrm{DS}})}{V_{\mathrm{eff}}} v_{\mathrm{in}}. \quad (12)$$

As shown in Eq. (12) and Fig. 5, the signal current due to g_{DS} has the opposite sign of v_{in} and attenuates an integrated output signal by g_{m}. i_{DS2} becomes larger as the integrated output signal increases — or $V_{\mathrm{out\_int}}$ decreases from V_{dd}. A

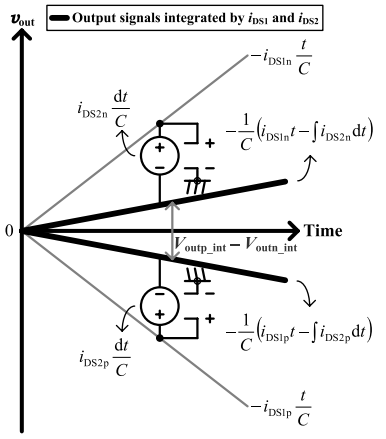

Fig. 5 Effects of g_{m} and g_{DS} on i_{DS} ($v_{\mathrm{in}} > 0$ V).

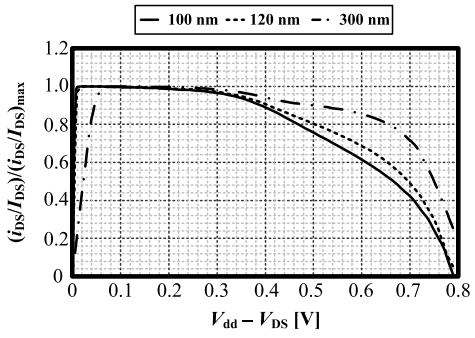

Fig. 6 Influence of channel-length modulation on i_{DS} (V_{dd} = 1.0 V, V_{eff} = 0.2 V, and v_{in} = 1 mV).

total signal current, i_{DS}, is a sum of i_{DS1} and i_{DS2}.

$$i_{\mathrm{DS}} = i_{\mathrm{DS1}} + i_{\mathrm{DS2}} = \mu C_{\mathrm{OX}} \frac{W}{L} V_{\mathrm{eff}} \left(1 + \lambda \left(2\,V_{\mathrm{DS}} - V_{\mathrm{dd}} - V_{\mathrm{eff}}\right)\right) \times v_{\mathrm{in}} \quad (13)$$

From Eq. (13), as λ decreases — or channel length increases, the total signal current increases. Figure 6 is simulation results of Eq. (13). In Fig. 6, the vertical axis is $(i_{\mathrm{DS}}/I_{\mathrm{DS}})$. This is because i_{DS1} from Eq. (8) also includes the influence of channel modulation and the channel modulation effect affects i_{DS1} as the same as I_{DS}. To remove this influence and to show only influence of g_{DS}, i_{DS} is divided by I_{DS}. In Fig. 6, $(i_{\mathrm{DS}}/I_{\mathrm{DS}})$ is normalized by its maximum value. From Eq. (1), the horizontal axis of Fig. 6 could be relabeled as time and then the area of the waveform would be proportional to charges integrated on a load capacitor. Therefore, as channel length increases, area of the waveform increases and the gain of pre-amplifier becomes larger. An average total signal current, $\overline{i_{\mathrm{DS}}}$, is

$$\overline{i_{\mathrm{DS}}} = \frac{1}{t}\int_0^t i_{\mathrm{DS}} dt = \frac{1}{V_{\mathrm{DS}} - V_{\mathrm{dd}}} \int_{V_{\mathrm{dd}}}^{V_{\mathrm{DS}}} i_{\mathrm{DS}} dV_{\mathrm{DS}} = \mu C_{\mathrm{OX}} \frac{W}{L} V_{\mathrm{eff}} \left(1 + \lambda \left(V_{\mathrm{DS}} - V_{\mathrm{eff}}\right)\right) \times v_{\mathrm{in}} = g_{m(V_{\mathrm{out\_int}} = V_{\mathrm{DS}})} v_{\mathrm{in}}. \quad (14)$$

From Eqs. (1) and (14), a transient gain, $G_{\mathrm{amp\_trans}}$, is ex-

pressed as below;

$$G_{\text{amp\_trans}} = \frac{v_{\text{out}}}{v_{\text{in}}} = -\frac{\overline{i_{\text{DS}}t}}{Cv_{\text{in}}} = -\frac{2\,(V_{\text{dd}} - V_{\text{DS}})}{V_{\text{eff}}} \times \frac{1 + \lambda\,(V_{\text{DS}} - V_{\text{eff}})}{1 + \frac{\lambda}{2}\,(V_{\text{dd}} + V_{\text{DS}} - 2\,V_{\text{eff}})}. \quad (15)$$

From Eq. (13), if λ is smaller than $1/(V_{\text{dd}} - V_{\text{eff}})$, i_{DS} always has the same sign as v_{in}. Thus, in the saturation region and satisfying this λ condition, $|G_{\text{amp\_trans}}|$ always increases as $V_{\text{out\_int}}$ reaches V_{eff}.

However, when input transistors enter the triode region, i_{DS} doesn't always have the same sign as v_{in}. Drain current in the triode region is

$$I_{\text{DS\_tri}} = \frac{1}{2}\mu C_{\text{OX}}\frac{W}{L}\,(2\,V_{\text{eff}} - V_{\text{DS}})\,V_{\text{DS}}. \quad (16)$$

From Eq. (16), a transconductance and an output conductance in the triode region are

$$g_{\text{m\_tri}} = \mu C_{\text{OX}}\frac{W}{L}\,(V_{\text{DS}} + v_{\text{out}}) \quad (17)$$

$$g_{\text{DS\_tri}} = \mu C_{\text{OX}}\frac{W}{L}\,((V_{\text{eff}} + v_{\text{in}}) - (V_{\text{DS}} + v_{\text{out}})) \quad (18)$$

where an input signal and an output signal are considered. A total signal current in the triode region, $i_{\text{DS\_tri}}$, is

$$i_{\text{DS\_tri}} = g_{\text{m\_tri}}v_{\text{in}} + g_{\text{DS\_tri}}v_{\text{out}} = \mu C_{\text{OX}}\frac{W}{L}\begin{pmatrix}(V_{\text{DS}}+v_{\text{out}})\,v_{\text{in}} \\ +\,((V_{\text{eff}}+v_{\text{in}})-(V_{\text{DS}}+v_{\text{out}}))\,v_{\text{out}}\end{pmatrix}. \quad (19)$$

Differential value of the total signal current in the triode region, $i_{\text{DS\_tri\_diff}}$, is

$$\begin{aligned} i_{\text{DS\_tri\_diff}} &= i_{\text{DSp\_tri}} - i_{\text{DSn\_tri}} \\ &= \mu C_{\text{OX}}\frac{W}{L}\begin{pmatrix} V_{\text{DS}}\left(v_{\text{inp}} - v_{\text{inn}}\right) \\ +2\left(v_{\text{inp}}v_{\text{outp}} - v_{\text{inn}}v_{\text{outn}}\right) \\ +\,(V_{\text{eff}} - V_{\text{DS}})\left(v_{\text{outp}} - v_{\text{outn}}\right) \\ -\left(v_{\text{outp}}^2 - v_{\text{outn}}^2\right)\end{pmatrix} \\ &\approx \mu C_{\text{OX}}\frac{W}{L}\,(V_{\text{DS}}v_{\text{in\_diff}} + (V_{\text{eff}} - V_{\text{DS}})\,v_{\text{out\_diff}}) \\ &= \mu C_{\text{OX}}\frac{W}{L}\left(V_{\text{DS}} - (V_{\text{eff}} - V_{\text{DS}})\left|G_{\text{amp\_trans}}\right|\right)v_{\text{in\_diff}} \end{aligned} \quad (20)$$

$|G_{\text{amp\_trans}}|$ reaches its maximum value when $i_{\text{DS\_tri\_diff}}$ becomes 0 A and reduces as V_{DS} drops from the value.

$$i_{\text{DS\_tri\_diff}} = 0 \longrightarrow V_{\text{DS}} = \frac{V_{\text{eff}}}{1 + 1/\left|G_{\text{amp\_trans}}\right|} \approx V_{\text{eff}} \quad (21)$$

From Eq. (21), the maximum gain is attained when V_{DS} reaches V_{eff}. Equations (15) and (21) are compared with simulation results in Fig. 7. In Fig. 7(a), the estimated gain, when input transistors are in the triode region, is also calculated by the gain equation deduced from the saturation condition. Thus, the difference with the simulation results becomes large when V_{DS} is smaller than V_{eff}. When V_{eff} is designed between 0.15 V and 0.35 V, the estimation is valid. For V_{eff} smaller than 0.15 V, it is close to the sub-threshold region, and V_{eff} larger than 0.35 V may induce carrier velocity saturation [6], [17];

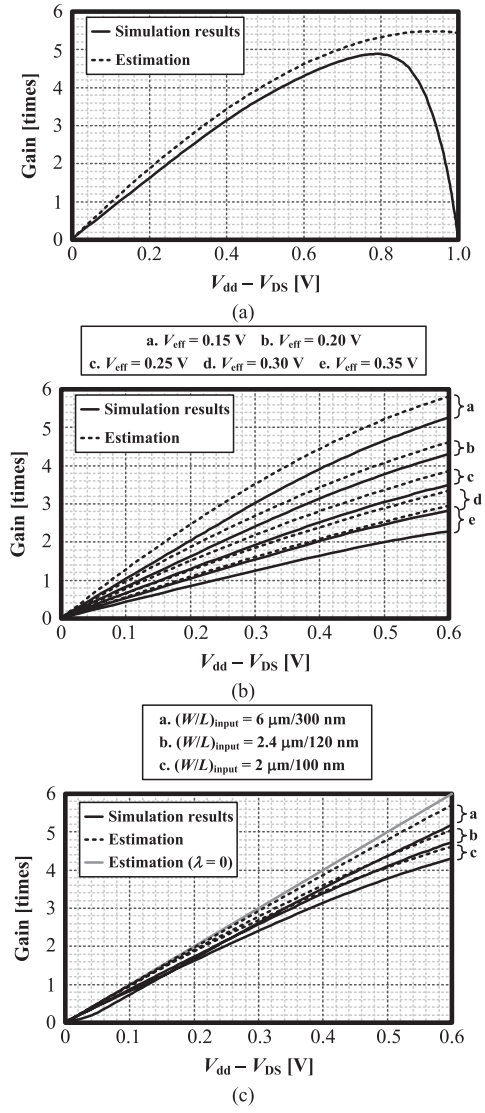

Fig. 7 Gain of pre-amplifier (a) V_{eff} = 0.2 V, (b) various V_{eff}, and (c) various channel length when V_{eff} is 0.2 V.

$$\mu_{\text{n}}\,(eff) = \frac{\mu_{\text{no}}}{1 + \eta \cdot V_{\text{eff}}} \quad (22)$$

where μ_{no} is the low-field surface electron mobility and η is an empirical coefficient. In both the former and the latter cases, the drain current doesn't satisfy Eq. (4). Therefore, there may be large difference between the estimation and the simulation results in the above cases.

As shown in Fig. 7(b) and Eq. (15), $|G_{\text{amp\_trans}}|$ increases as V_{eff} decreases. Compared with an amplifier which

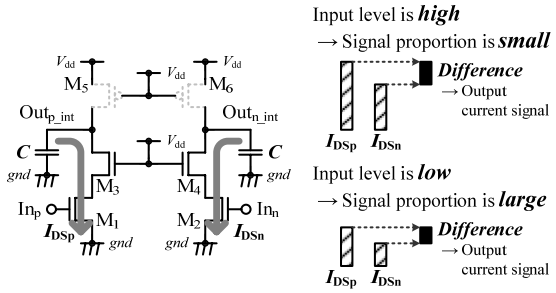

Fig. 8 Simplified schematic of a pre-amplifier and drain current variation of input transistors by input common-mode voltage.

consumes static current, this relation is reversed. This is because, in terms of I_{DS}, a signal proportion of small V_{eff} is larger than one of large V_{eff} as shown in Fig. 8 [10]. As this ratio is large — or V_{eff} is small —, integration time relatively becomes long. Thus, in dynamic amplifier, $|G_{\mathrm{amp\_trans}}|$ is inversely proportional to V_{eff}. A ratio of the signal current to the drain current is deduced from Eq. (15);

$$v_{\mathrm{out}} \propto \frac{i_{\mathrm{DS}}}{I_{\mathrm{DS}}} = \frac{2v_{\mathrm{in}}}{V_{\mathrm{eff}}}. \quad (\text{if } \lambda \text{ is ignorable}) \tag{23}$$

2.2 Thermal Noise

The gain of pre-amplifier increases signal power of the second stage, thus it reduces dead-zone of the comparator. Thermal noise of a dynamic amplifier was already reported in recently published papers [7], [11]–[15]. In this section, we compare simulation results to estimation with Eq. (15). Assuming an input signal of the second stage is decided when gain reaches its maximum, integration time and the gain of pre-amplifier become

$$t_{(V_{\mathrm{DS}}=V_{\mathrm{eff}})} = \frac{(V_{\mathrm{dd}} - V_{\mathrm{eff}})\,C}{\overline{I_{\mathrm{DS}}}} \equiv t_1. \tag{24}$$

$$\begin{aligned} G_{\mathrm{amp}} &\equiv G_{\mathrm{amp\_trans}(V_{\mathrm{DS}}=V_{\mathrm{eff}})} \\ &= -\frac{2\,(V_{\mathrm{dd}} - V_{\mathrm{eff}})}{V_{\mathrm{eff}}} \times \frac{1}{1 + \frac{\lambda}{2}\,(V_{\mathrm{dd}} - V_{\mathrm{eff}})}. \end{aligned} \tag{25}$$

When a time constant, τ_1, is sufficiently larger than t_1, then an input-referred thermal noise due to a transistor is expressed as below;

$$\overline{v_{\mathrm{n\_MOS}}^2} = 2kT\gamma\overline{g_{\mathrm{m}}} \times \frac{t_1}{\left(C \cdot G_{\mathrm{amp}}\right)^2} \tag{26}$$

$$\tau_1 = \frac{C}{\lambda I_{\mathrm{DS\_ideal}}} \tag{27}$$

where k is a Boltzmann constant, T is an ambient temperature, γ is a noise factor, and $\overline{g_{\mathrm{m}}}$ is an average transconductance. Substituting Eqs. (24) and (25) into Eq. (26), then

$$\overline{v_{\mathrm{n\_MOS}}^2} = \frac{2kT\gamma}{C} \times \left(1 + \frac{\lambda}{2}\,(V_{\mathrm{dd}} - V_{\mathrm{eff}})\right) \times \frac{1}{\left|G_{\mathrm{amp}}\right|}. \tag{28}$$

An initial noise on the output node also exists and its input-referred value is expressed as below;

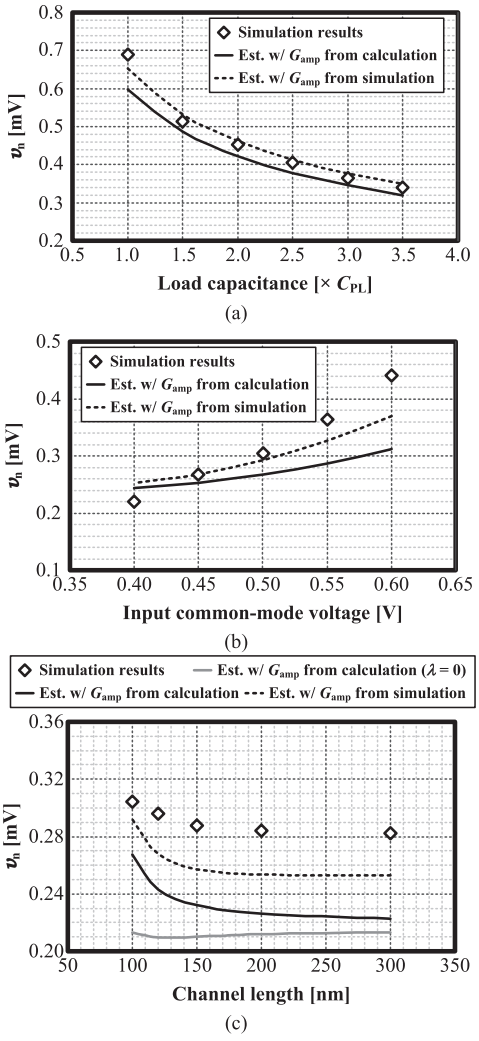

Fig. 9 Influence on thermal noise (a) load capacitance, (b) input common-mode voltage, and (c) channel length (V_{dd} = 1.0 V, $V_{\mathrm{in\_com}}$ = 0.5 V, $C = 5C_{PL}$, $C_{PL} \approx$ 10.8 fF, T = 300 K, γ = 2/3, and a number of the simulation is 500).

$$\overline{v_{\mathrm{n\_initial}}^2} = \frac{kT}{C}\exp\left(-\frac{t_1}{\tau_1}\right) \times \frac{1}{G_{\mathrm{amp}}^2}. \tag{29}$$

Assuming the gain of pre-amplifier is sufficiently large, thermal noise of the second stage may be ignored and the input-referred thermal noise of the comparator is deduced as below;

$$\begin{aligned} \overline{v_{\mathrm{n}}^2} = {} & \frac{2kT}{C\left|G_{\mathrm{amp}}\right|} \\ & \times \left(2\gamma\left(1 + \frac{\lambda}{2}\,(V_{\mathrm{dd}} - V_{\mathrm{eff}})\right) + \frac{1}{\left|G_{\mathrm{amp}}\right|}\exp\left(-\frac{t_1}{\tau_1}\right)\right). \end{aligned} \tag{30}$$

From Eq. (30), thermal noise can be modified by load capacitance and input common-mode voltage. Figure 9 compares the estimation and simulation results when γ is 2/3. Figure 9(c) shows channel-length modulation decreases the gain of pre-amplifier and increases the input-referred thermal noise.

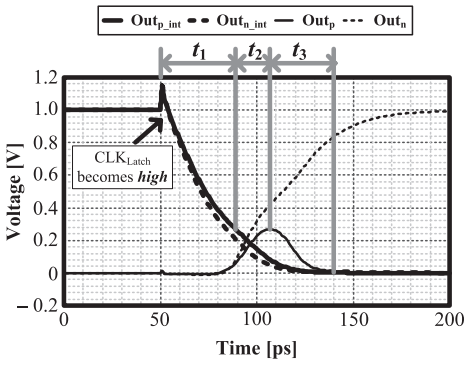

Fig. 10 A division of total regeneration time.

2.3 Regeneration Time

As analyzed in the previous sections, small V_{eff} increases the gain of pre-amplifier and decreases dead-zone. However, a regeneration time increases as V_{eff} becomes smaller. For simplicity, we divide regeneration into three segments as depicted in Fig. 10. t_1 is the integration time of pre-amplifier, t_2 is the response delay of the second stage, and t_3 is the regeneration time of the second stage. t_1 is determined by Eq. (6) by substituting V_{eff} into V_{DS}. t_2 is decided as calculated results are close to simulation results and the time is set as 17 ps in this paper. Without this variable, the estimation is very different from simulation results as shown in reference [10]. Assuming an inverter chain of the second stage enters unstable equilibrium after $(t_1 + t_2)$, t_3 is expressed as below [17], [18];

$$t_3 = \frac{\tau_2}{|G_{\text{inv}}| - 1} \times \ln\left(\frac{\Delta V}{g_{\text{m\_M9}} r_{\text{o\_2nd}} \times \left(\left|G_{\text{amp}}\right| v_{\text{in}}\right)}\right) \quad (31)$$

where ΔV is a voltage difference between the output voltages of the second stage, G_{inv} is a low-frequency gain of each inverter implemented in the second stage, τ_2 is a time constant at the output node of each inverter, $g_{\text{m\_M9}}$ is a transconductance of M_9 (or M_{10}) in Fig. 1, and $r_{\text{o\_2nd}}$ is an output resistance of the second stage. Therefore, total regeneration time is

$$t_{\text{reg}} = \frac{2\,(V_{\text{dd}} - V_{\text{eff}})\,C}{\overline{I_{\text{DS}}}} + t_2 + \frac{\tau_2}{|G_{\text{inv}}|-1} \times \ln\left(\frac{\Delta V}{g_{\text{m\_M9}} r_{\text{o\_2nd}} \times \left(\left|G_{\text{amp}}\right| v_{\text{in}}\right)}\right). \quad (32)$$

In Fig. 11, Eq. (32) is compared with simulation results. As shown in Eq. (32) and Fig. 11, small V_{eff} increases regeneration time.

2.4 Mismatch

Although the size of every transistor is the same, mismatch contribution is different due to their position. Table 1 and Fig. 12 show the mismatch contribution of each transistor pair in the comparator depicted in Fig. 1. Simulation data demonstrate that offset voltage is dominated by a pair of input transistors. From simulation data, they occupy about 86% of the entire mismatch. Mismatch variation is inversely proportional to the size of a transistor [6];

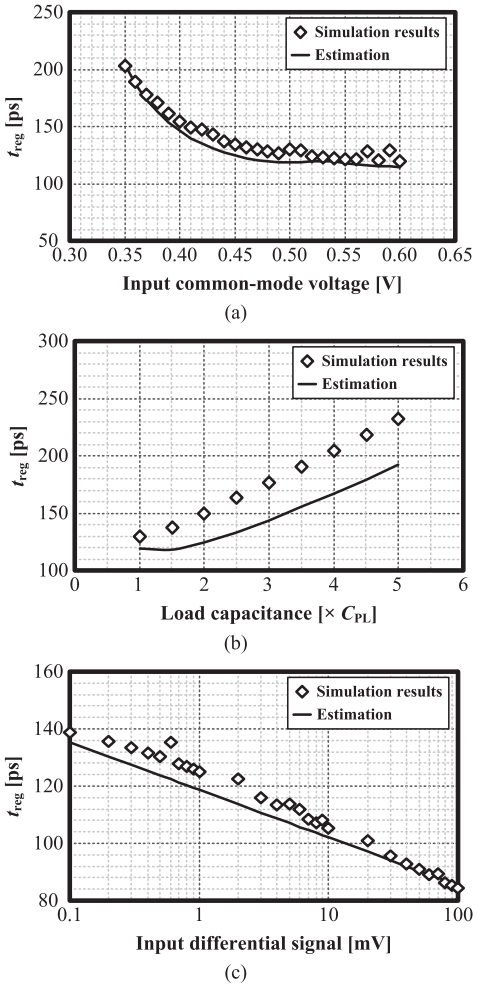

Fig. 11 Regeneration time affected by (a) input common-mode voltage, (b) load capacitance of the first stage, and (c) input differential signal (V_{dd} = 1.0 V, $V_{\text{in\_com}}$ = 0.5 V, ΔV = 0.9 V_{dd}, and $v_{\text{in\_diff}}$ = 1 mV).

Table 1 Mismatch contribution of each transistor pair (V_{dd} = 1.0 V, $V_{\text{in\_com}}$ = 0.5 V, and a number of the Monte Carlo simulation is 500).

A pair of transistors	$\sigma_{V\ \text{offset}}$ [mV]
M_1 and M_2	9.12
M_3 and M_4	1.58
M_5 and M_6	0.529
M_7 and M_8	0.491
M_9 and M_{10}	0.654
M_{11} and M_{12}	1.82
M_{13} and M_{14}	1.26
M_{15} and M_{16}	2.32
Total	9.85

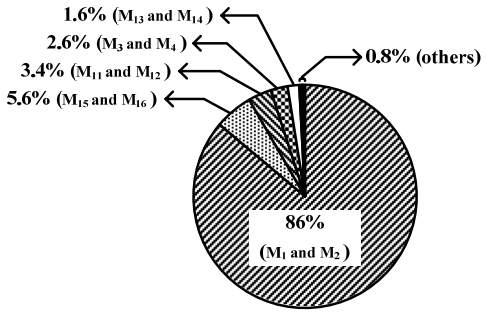

Fig. 12 Mismatch contribution of each transistor pair.

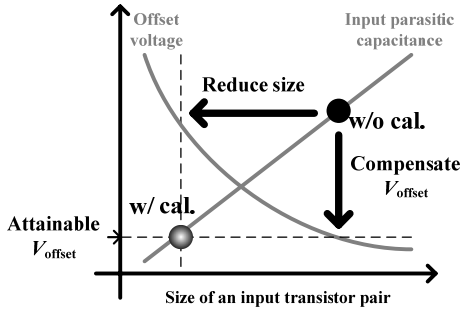

Fig. 13 Calibration effect.

$$\Delta V_{\mathrm{th}} \propto \frac{1}{\sqrt{W \cdot L}}. \tag{33}$$

Therefore, by increasing size of the input transistors, offset voltage may be suppressed without increasing power consumption of the comparator described in Fig. 1. Because its power consumption, P_{C}, is proportional to load capacitance of a pre-amplifier and the second stage;

$$P_C \propto fCV_{\mathrm{dd}}^2. \tag{34}$$

However, this method may significantly increase input parasitic capacitance. For example, when we implement a sample-and-hold circuit in front of the comparator, this input parasitic capacitance attenuates signal. Consequently, this may expand the input-referred dead-zone of the comparator. However, calibration can suppress mismatch despite a small size as described in Fig. 13. To effectively reduce offset voltage, calibration should compensate mismatch induced by a pair of input transistors. Equation (1) shows that when there is mismatch due to input transistors, I_{DS} changes from the designed value and the output of a pre-amplifier also varies from the ideal value. To compensate the mismatch, calibration of load capacitance [4], [5] and bypass current [9], [10] has been commonly selected. In the following sections, we will discuss the characteristic of each calibration method.

3. Capacitance Calibration

The capacitance calibration [4], [5] changes load capacitance where a signal is integrated as depicted in Fig. 14 [19]. In Fig. 14, transistors of D_{Dummy} and DB_{Dummy} are implemented for analysis, and their number of unit transistor is

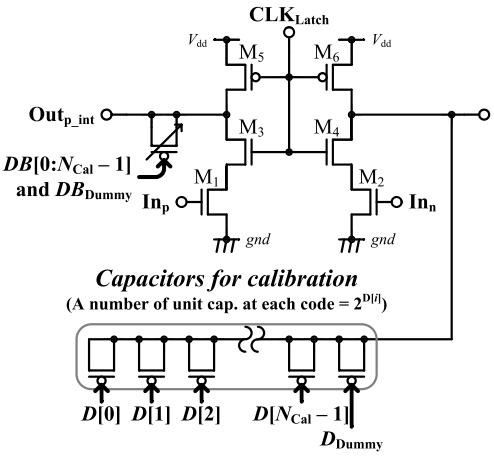

Fig. 14 A pre-amplifier with calibration capacitors attached on output nodes.

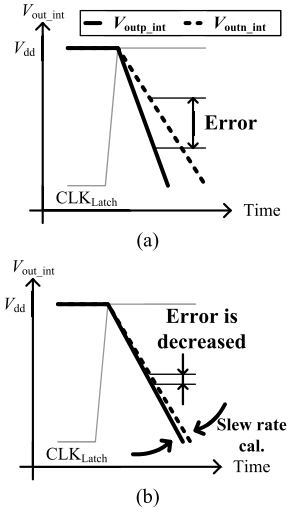

Fig. 15 Error reduction by a slew-rate calibration on the output nodes of a pre-amplifier (a) before calibration and (b) after calibration (in both cases, a differential input signal is 0 V).

1. Without these transistors, offset voltage doesn't become 0 V when a calibration code is in the middle of its maximum code. In actual design, these transistors are not required. The capacitance of a PMOS capacitor varies whether transistor is turned on or off, and this calibration uses the difference between the capacitance of the two states. From Eq. (1), the slew rate, I_{DS}/C, is inversely proportional to load capacitance. When the calibration is conducted, these slew rates become closer together and the offset voltage is compensated as described in Fig. 15.

3.1 Input-Referred Compensated Voltage

Based on Eq. (1), let us estimate the input-referred compensated voltage of the capacitance calibration. First, differentiate Eq. (1) with respect to capacitance;

$$\frac{dV_{\mathrm{out\_int}}}{dC} = \frac{\overline{I_{\mathrm{DS}}}}{C^2} t_1. \tag{35}$$

Substituting Eq. (6) into Eq. (35), then

$$\frac{dV_{\text{out\_int}}}{dC} = \frac{V_{\text{dd}} - V_{\text{eff}}}{C} \tag{36}$$

From Eqs. (25) and (36), an input-referred variation is deduced as below;

$$\left(\frac{dV_{\text{out\_int}}}{dC}\right)_{\text{input-referred}} = -\frac{V_{\text{eff}}}{2C} \times \left(1 + \frac{\lambda}{2}\left(V_{\text{dd}} - V_{\text{eff}}\right)\right) \equiv A_1 \tag{37}$$

$$v_{\text{in\_cal}} \equiv A_1 \Delta C_{\text{cal}} \tag{38}$$

where ΔC_{cal} is a changed capacitance by calibration code and $v_{\text{in\_cal}}$ is an input-referred compensated voltage due to ΔC_{cal}. The load capacitance, C, in Eq. (37) differs between calibration codes.

$$v_{\text{in\_cal}} = A_1 C \times \int_{2^{N_{\text{cal}}-1}}^{N_{\text{Code}}} \frac{C_{\text{d}}}{C + C_{\text{d}}\left(N_{\text{Code}} - 2^{N_{\text{cal}}-1}\right)} dN_{\text{Code}} \quad \left(C_{\text{d}} \equiv C_{\text{on}} - C_{\text{off}}\right) \tag{39}$$

where C_{on} and C_{off} are capacitances of a unit-sized transistor capacitor which is turned on and off, respectively; N_{Code} is a calibration code; and N_{cal} is a calibration resolution. The input-referred compensated voltage is calculated by conducting integration of Eq. (39) with respect to capacitance.

$$v_{\text{inp\_cal}} \equiv A_1 C \times \ln\left(1 + \frac{C_{\text{d}}}{C}\left(N_{\text{Code}} - 2^{N_{\text{cal}}-1}\right)\right) \tag{40}$$

$$v_{\text{inn\_cal}} \equiv A_1 C \times \ln\left(1 - \frac{C_{\text{d}}}{C}\left(N_{\text{Code}} - 2^{N_{\text{cal}}-1}\right)\right) \tag{41}$$

$$v_{\text{in\_diff\_cal}} \equiv v_{\text{inp\_cal}} - v_{\text{inn\_cal}} = A_1 C \times \ln\left(\frac{C + C_{\text{d}}\left(N_{\text{Code}} - 2^{N_{\text{cal}}-1}\right)}{C - C_{\text{d}}\left(N_{\text{Code}} - 2^{N_{\text{cal}}-1}\right)}\right) \tag{42}$$

The input-referred compensated voltage of Eq. (42) is a little bit complicated. Assuming the load capacitance doesn't vary from the capacitance when calibration code is in the middle of its maximum code, the input-referred compensated voltage can be simplified.

$$v_{\text{inp\_cal}} = A_1 \times \left(N_{\text{Code}} - 2^{N_{\text{cal}}-1}\right) C_{\text{d}} \tag{43}$$

$$v_{\text{inn\_cal}} = -A_1 \times \left(N_{\text{Code}} - 2^{N_{\text{cal}}-1}\right) C_{\text{d}} \tag{44}$$

$$v_{\text{in\_diff\_cal}} = 2A_1 \times \left(N_{\text{Code}} - 2^{N_{\text{cal}}-1}\right) C_{\text{d}} \tag{45}$$

Estimations of Eqs. (42) and (45) are almost the same and Fig. 16 compares Eq. (45) with simulation results.

3.2 Mismatch

Every component has mismatch, thus PMOS capacitors for calibration also induce offset voltage. Assuming calibration code, N_{Code}, is at the center which is 2^{Ncal-1}, let us deduce an offset voltage, $\sigma_{\text{V\_Ccal}}$, due to the calibration capacitors. From the Eq. (38), offset voltage is

$$\sigma_{\text{V\_Ccal}} = |A_1|\, \sigma_{\text{C\_Ccal}} \tag{46}$$

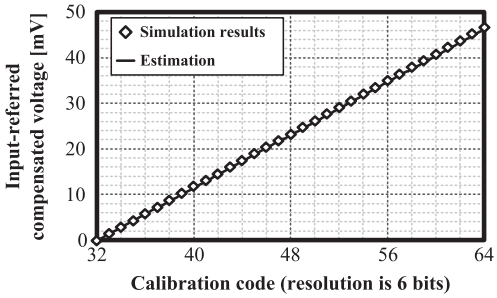

Fig. 16 Input-referred compensated voltage by the capacitance calibration (V_{dd} = 1.0 V, $V_{\text{in\_com}}$ = 0.5 V, calibration resolution is 6 bits, and unit PMOS capacitor size is W/L = 600 nm/100 nm).

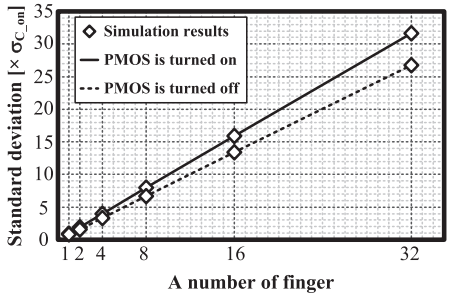

Fig. 17 A number of finger versus capacitance mismatch (unit PMOS capacitor size is W/L = 600 nm/100 nm and a number of the Monte Carlo simulation is 100).

$$\sigma^2_{\text{C\_Ccal}} \equiv \sigma^2_{\text{C\_Ccalp}} + \sigma^2_{\text{C\_Ccaln}} \tag{47}$$

where $\sigma_{\text{C\_Ccalp}}$ is a capacitance mismatch due to calibration capacitors in positive side, $\sigma_{\text{C\_Ccaln}}$ is a capacitance mismatch due to calibration capacitors in negative side, and $\sigma_{\text{C\_Ccal}}$ is a total capacitance mismatch caused by calibration capacitors attached on both sides. Assuming each PMOS capacitor, whose digital code D[i] is the same, is located as close as finger structure, then their mismatch will be correlated. These simulation results are shown in Fig. 17. In Fig. 17, standard deviation of capacitance is normalized by standard deviation of a unit PMOS capacitor which is turned on, $\sigma_{\text{C\_on}}$. When calibration code is at its center, $\sigma_{\text{C\_Ccal\_p}}$ and $\sigma_{\text{C\_Ccal\_n}}$ are written as follow;

$$\sigma^2_{\text{C\_Calp}} = \sigma^2_{\text{C\_off}} + (2\sigma_{\text{C\_off}})^2 + (4\sigma_{\text{C\_off}})^2 + \cdots + \left(2^{N_c-2}\sigma_{\text{C\_off}}\right)^2 + \left(2^{N_c-1}\sigma_{\text{C\_on}}\right)^2 + \sigma^2_{\text{C\_off}} \tag{48}$$

$$\sigma^2_{\text{C\_Caln}} = \sigma^2_{\text{C\_on}} + (2\sigma_{\text{C\_on}})^2 + (4\sigma_{\text{C\_on}})^2 + \cdots + \left(2^{N_c-2}\sigma_{\text{C\_on}}\right)^2 + \left(2^{N_c-1}\sigma_{\text{C\_off}}\right)^2 + \sigma^2_{\text{C\_on}} \tag{49}$$

where $\sigma_{\text{C\_on}}$ and $\sigma_{\text{C\_off}}$ are standard deviations of unit PMOS capacitances which are turned on and off, respectively. From Eqs. (48) and (49), the offset voltage due to the calibration capacitors is derived.

$$\sigma^2_{\text{C\_Cal}} = \left(\frac{2}{3} + \frac{4^{N_{\text{cal}}}}{3}\right) \times \left(\sigma^2_{\text{C\_on}} + \sigma^2_{\text{C\_off}}\right) \tag{50}$$

$$\sigma_{\text{V\_Ccal}} = |A_1| \times \sqrt{\left(\frac{2}{3} + \frac{4^{N_{\text{cal}}}}{3}\right) \times \left(\sigma^2_{\text{C\_on}} + \sigma^2_{\text{C\_off}}\right)} \tag{51}$$

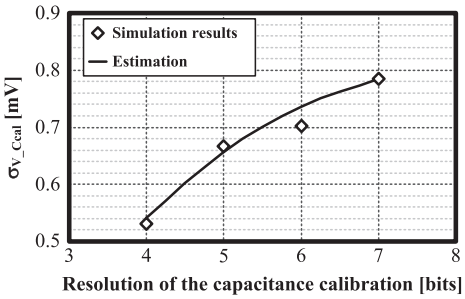

Fig. 18 σ_{V_Ccal} due to the capacitance calibration (V_{dd} = 1.0 V, V_{in_com} = 0.5 V, unit PMOS capacitor size is W/L = 600 nm/100 nm, and a number of the Monte Carlo simulation is 500).

Comparison between Eq. (51) and simulation results is shown in Fig. 18. Assuming resolution of the capacitance calibration is 6 bits, σ_{V_Ccal} is about 0.758 mV from the estimation. From the simulation results of Table 1, the offset voltage of a comparator is about 9.85 mV. Then, the offset voltage of a comparator with the capacitance calibration will be 9.89 mV, and this value is almost the same as the Monte Carlo simulation results of 9.88 mV. Compared with the offset voltage of a comparator, offset voltage induced by the capacitance calibration is negligible.

3.3 Thermal Noise

The capacitance calibration has robustness about thermal noise. Additional load capacitance reduces thermal noise of a pre-amplifier and initial noise. From Eq. (30), when V_{dd} is 1.0 V; V_{in_com} is 0.5 V; a unit PMOS capacitor size is W/L = 600 nm/100 nm; and calibration resolution is 6 bits, thermal noise, v_n (σ), is estimated to be 0.288 mV — from the simulation data, thermal noise was 0.259 mV. The capacitance calibration reduces thermal noise power by 85.9% from the value without the capacitance calibration.

3.4 PVT Variation

If circuits are implemented on a chip, their performance is affected by circumstances such as a process variation, a voltage fluctuation, and a temperature change. These are called PVT variation. They degrade compensation accuracy if the surrounding condition is varied after calibration was conducted. Influence of process is fixed in the factory and this doesn't affect the offset after calibration. In this section, only voltage fluctuation and temperature change are considered.

From Eq. (25), G_{amp} is decided by a ratio of V_{dd} to V_{eff} and λ. If temperature is changed, then V_{th} and λ are varied. Influence of voltage fluctuation on G_{amp} is easy to understand. In Eq. (45), A_1 is inversely proportional to G_{amp}, thus input-referred compensated voltages also change and the variation differs in each calibration code. If an error due to PVT variation, σ_{V_PVT}, is uncorrelated with an offset after calibration, $\sigma_{V\_offset0}$, then a total offset voltage, σ_{V_offset}, can be expressed as

$$\sigma^2_{V\_offset} = \sigma^2_{V\_offset0} + \sigma^2_{V\_PVT}. \tag{52}$$

From Eq. (45), if input common-mode voltage, V_{in_com}, is fluctuated, then

$$\begin{aligned}\Delta v_{in\_diff\_cal} &= \frac{dv_{in\_diff\_cal}}{dV_{in\_com}} \times \Delta V_{in\_com} \\ &= 2\,|A_1| \times \left(\frac{\Delta V_{eff}}{V_{eff}} + \frac{(V_{dd} - V_{eff})\,\frac{\Delta\lambda}{2} - \frac{\lambda}{2}\Delta V_{eff}}{1 + \frac{\lambda}{2}(V_{dd} - V_{eff})} \right) \\ &\quad \times \left(N_{Code} - 2^{N_{cal}-1} \right) C_d. \end{aligned} \tag{53}$$

From Eq. (53), when a standard deviation of calibration code is σ_{Code}, errors due to changes of V_{eff}, λ, and $(V_{dd} - V_{eff})$ are expressed as

$$\text{Error due to } V_{eff} = 2\,|A_1| \times \frac{\Delta V_{eff}}{V_{eff}} \times C_d \sigma_{Code} \tag{54}$$

$$\text{Error due to } \lambda = 2\,|A_1| \times \frac{(V_{dd} - V_{eff})\,\frac{\Delta\lambda}{2}}{1 + \frac{\lambda}{2}(V_{dd} - V_{eff})} \times C_d \sigma_{Code} \tag{55}$$

$$\text{Error due to } (V_{dd} - V_{eff}) = 2\,|A_1| \times \frac{-\frac{\lambda}{2}\Delta V_{eff}}{1 + \frac{\lambda}{2}(V_{dd} - V_{eff})} \times C_d \sigma_{Code}. \tag{56}$$

If variations of V_{eff} and λ are uncorrelated, then σ_{V_PVT} due to input common-mode voltage, $\sigma_{V\_PVT\_Vcom}$, is deduced as below;

$$\begin{aligned}&\sigma_{V\_PVT\_VCOM} \\ &= 2\,|A_1| \sqrt{\left(\frac{\Delta V_{eff}}{V_{eff}} - \frac{\lambda \Delta V_{eff}}{2 + \lambda (V_{dd} - V_{eff})} \right)^2 + \left(\frac{(V_{dd} - V_{eff})\,\Delta\lambda}{2 + \lambda (V_{dd} - V_{eff})} \right)^2} \\ &\quad \times C_d \sigma_{Code}. \end{aligned} \tag{57}$$

If supply voltage, V_{dd}, is fluctuated, then σ_{V_PVT} due to supply voltage, $\sigma_{V\_PVT\_Vdd}$, is

$$\sigma_{V\_PVT\_Vdd} = 2\,|A_1| \times \sqrt{\left(\frac{\lambda \Delta V_{dd}}{2 + \lambda (V_{dd} - V_{eff})} \right)^2} \times C_d \sigma_{Code}. \tag{58}$$

If temperature is fluctuated, then σ_{V_PVT} due to temperature, $\sigma_{V\_PVT\_T}$, is

$$\begin{aligned}&\sigma_{V\_PVT\_T} \\ &= 2\,|A_1| \sqrt{\left(-\frac{\Delta V_{th}}{V_{eff}} + \frac{\lambda \Delta V_{th}}{2 + \lambda (V_{dd} - V_{eff})} \right)^2 + \left(\frac{(V_{dd} - V_{eff})\,\Delta\lambda}{2 + \lambda (V_{dd} - V_{eff})} \right)^2} \\ &\quad \times C_d \sigma_{Code}. \end{aligned} \tag{59}$$

Figure 19 compares the estimation with simulation results. Calibration is conducted when V_{dd} is 1.0 V, V_{in_com} is 0.5 V, and T is 27°C. Figure 19 also shows SNDR decrease which is calculated from estimated σ_{V_offset}. Assuming an input signal is a sine wave and the architecture of an ADC is flash, SNDR decrease is expressed as

$$SNDR = 10 \log \left(\frac{\left(2^N V_q / \left(2\sqrt{2} \right) \right)^2}{V_q^2/12 + \sigma_V^2} \right)$$

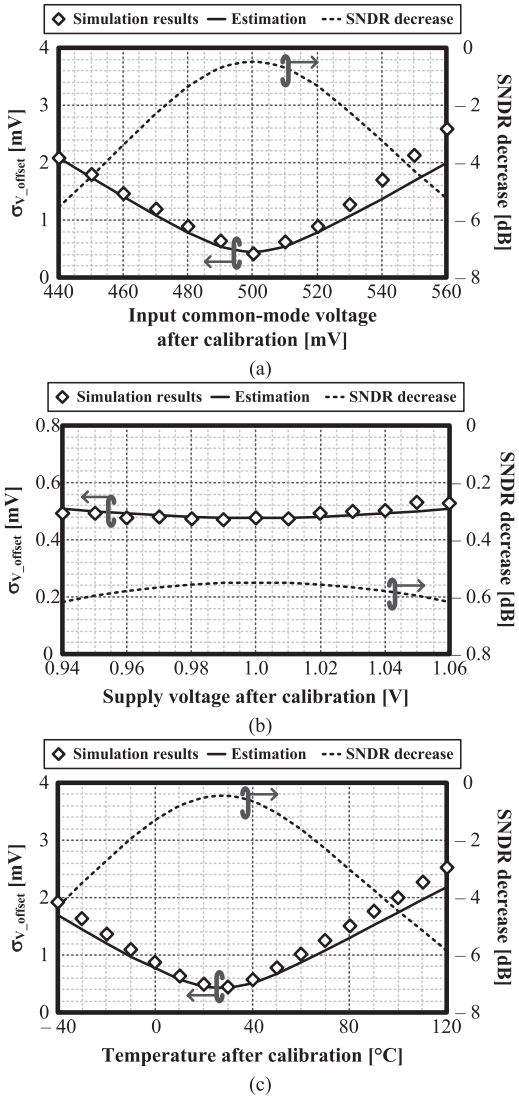

Fig. 19 Influence of PVT variation on the capacitance calibration (a) input common-mode voltage, (b) supply voltage, and (c) temperature (1 LSB = 4.5 mV and a number of the Monte Carlo simulation is 500).

$$= SQNR - 10\log\left(1 + \frac{12}{V_q^2}\sigma_V^2\right)$$

$$\longrightarrow SNDR_{\text{decrease}} = -10\log\left(1 + \frac{12}{V_q^2}\sigma_V^2\right) \quad (60)$$

where N is resolution of an ADC and V_q is 1 LSB. In Fig. 19, V_q is supposed to be three times of the least changeable voltage in calibration which equals 4.5 mV. From the estimation and the simulation results, if input common-mode voltage is varied about 60 mV or temperature is changed from 27°C to 120°C, ENOB will decrease about 1 bit.

3.5 Limitations

Input-referred compensated voltage of 1 LSB and calibration range are limited by C_{on}, C_{off}, and calibration resolution. From Eq. (45), input-referred compensated voltage of 1 LSB is

$$\begin{aligned} v_{\text{in\_diff\_cal\_1LSB}} &= 2\,|A_1|\,C_{\text{d}} \\ &= V_{\text{eff}} \times \left(1 + \frac{\lambda}{2}\left(V_{\text{dd}} - V_{\text{eff}}\right)\right) \\ &\quad \times \frac{C_{\text{on}} - C_{\text{off}}}{C_{PL} + 2^{N_{\text{cal}}-1} \times (C_{\text{on}} + C_{\text{off}})} \end{aligned} \quad (61)$$

and the maximum calibration range is

$$\begin{aligned} v_{\text{in\_diff\_cal\_max}} &= \lim_{N_{\text{cal}} \to \infty} 2\,|A_1|\left(2^{N_{\text{cal}}-1} C_{\text{d}}\right) \\ &= V_{\text{eff}} \times \left(1 + \frac{\lambda}{2}\left(V_{\text{dd}} - V_{\text{eff}}\right)\right) \\ &\quad \times \frac{C_{\text{on}} - C_{\text{off}}}{C_{\text{on}} + C_{\text{off}}} \end{aligned} \quad (62)$$

If a unit PMOS capacitor size is W/L = 600 nm/100 nm, the maximum calibration range is ±52.6 mV. When a unit PMOS capacitor size is W/L = 600 nm/100 nm and calibration resolution is 6 bits, the input-referred compensated voltage of 1 LSB is about 1.44 mV and the calibration range reaches 5 times of $\sigma_{\text{V\_offset}}$ including mismatch due to the capacitance calibration. And, in this condition, the capacitance calibration increases load capacitance by 77.6 fF.

In the capacitance calibration, additional load capacitance delays regeneration time and increases power consumption as shown in Eqs. (32) and (34). In Sect. 5, Table 2 compares those indices based on simulation results.

4. Current Calibration

The current calibration [9], [10] changes the drain current of a pre-amplifier by adding additional transistors, as described in Fig. 20. From Eq. (1), the slew rate is proportional to the drain current. When calibration is conducted, the slew rates become closer to each other and the offset voltage is compensated as described in Fig. 15. To generate the gate voltage of a bypass transistor, a charge pump [9], [10] or a resistor string can be selected.

4.1 Gain of Dynamic Amplifier

Bypass transistors flow additional drain current, thus gain differs from Eq. (15) due to the additional transistors. g_{DS}, $v_{\text{out\_diff}}$, and the integration time differ from Eqs. (6), (9), and (11);

$$t = \frac{(V_{\text{dd}} - V_{\text{DS}})\,C}{\overline{I_{\text{DS\_in}}} + \overline{I_{\text{DS\_cal}}}} \quad (63)$$

$$g_{\text{DS}} = g_{\text{DS\_in}} + g_{\text{DS\_cal}} \quad (64)$$

$$v_{\text{out\_diff}} = -\frac{2\,(V_{\text{dd}} - V_{\text{DS}})}{V_{\text{eff}}} \times \frac{\overline{I_{\text{DS\_in}}}}{\overline{I_{\text{DS\_in}}} + \overline{I_{\text{DS\_cal}}}} v_{\text{in\_diff}} \quad (65)$$

where variables with subscripts "in" and "cal" are parameters of an input transistor and parameters of a bypass transistor, respectively. A total signal current is

$$i_{\text{DS}} = g_{\text{m\_in}} v_{\text{in}} + (g_{\text{DS\_in}} + g_{\text{DS\_cal}})\,v_{\text{out}}. \quad (66)$$

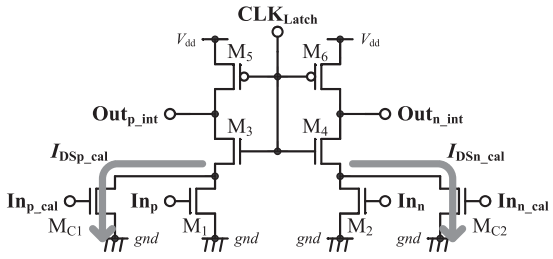

Fig. 20 A pre-amplifter with the current calibration.

Substituting Eqs. (63) and (66) into Eq. (15), then

$$G_{\text{amp\_trans}} = -\frac{2\,(V_{\text{dd}} - V_{\text{DS}})}{V_{\text{eff\_in}}} \times \left(1 - \frac{(g_{\text{DS\_in}} + g_{\text{DS\_cal}}) \times (V_{\text{dd}} - V_{\text{DS}})}{2\left(\overline{I_{\text{DS\_in}}} + \overline{I_{\text{DS\_cal}}}\right)}\right) \times \frac{\overline{I_{\text{DS\_in}}}}{\overline{I_{\text{DS\_in}}} + \overline{I_{\text{DS\_cal}}}}. \quad (67)$$

If channel length and V_{GS} of an input transistor and a bypass transistor are the same, then Eq. (67) is reduced as below;

$$G_{\text{amp\_trans}} = -\frac{2\,(V_{\text{dd}} - V_{\text{DS}})}{V_{\text{eff\_in}}} \times \frac{1+\lambda\,(V_{\text{DS}} - V_{\text{eff}})}{1+\frac{\lambda}{2}\,(V_{\text{dd}} + V_{\text{DS}} - 2V_{\text{eff}})} \times \frac{W_{\text{in}}}{W_{\text{in}} + W_{\text{cal}}}. \quad (68)$$

Compared with Eq. (15), gain is decreased in the current calibration. This is because the drain current of the calibration transistor doesn't amplify signal. Comparison between the estimation and simulation results are shown in Fig. 21.

4.2 Input-Referred Compensated Voltage

Input-referred compensated voltage of the current calibration is estimated by using Eq. (67). This equation means how large signal portion of an input transistor amplifies when signal portion of a bypass transistor is 0 V. Conducting the same calculation, small signal ratio of output to calibration input is

$$G_{\text{amp\_cal\_trans}} = -\frac{2\,(V_{\text{dd}} - V_{\text{DS}})}{V_{\text{eff\_call}}} \times \left(1 - \frac{(g_{\text{DS\_in}} + g_{\text{DS\_cal}}) \times (V_{\text{dd}} - V_{\text{DS}})}{2\left(\overline{I_{\text{DS\_in}}} + \overline{I_{\text{DS\_cal}}}\right)}\right) \times \frac{\overline{I_{\text{DS\_cal}}}}{\overline{I_{\text{DS\_in}}} + \overline{I_{\text{DS\_cal}}}}. \quad (69)$$

When a step size of compensating voltage is v_{d}, then

$$v_{\text{in\_diff\_cal}} \equiv \frac{G_{\text{amp\_cal}}}{G_{\text{amp}}}\left(N_{\text{Code}} - 2^{N_{\text{cal}}-1}\right) v_{\text{d}}. \quad (70)$$

λ differs as V_{GS} varies. If λ of an input transistor and λ of a bypass transistor are close to each other, then we could figure out V_{DS} where $G_{\text{amp\_trans}}$ becomes its maximum value

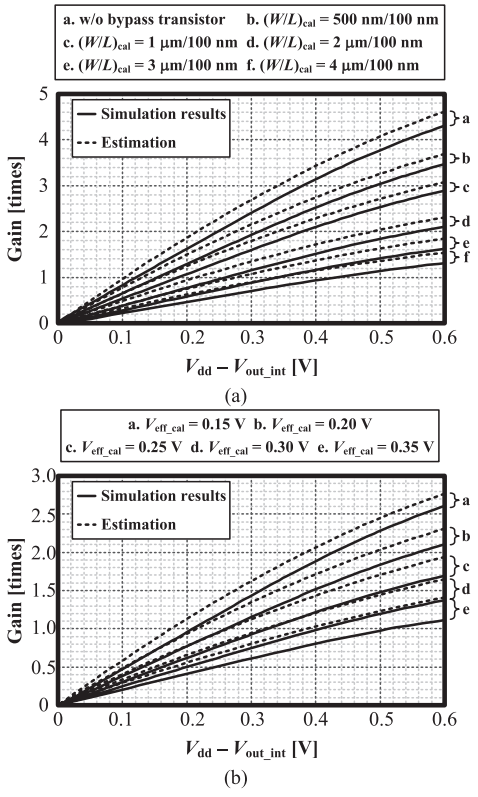

Fig. 21 Gain of pre-amplifier with bypass transistors (a) various channel length of a bypass transistor and (b) various $V_{\text{eff\_call}}$ ($V_{\text{dd}} = 1.0$ V and $V_{\text{eff}} = V_{\text{eff\_call}} = 0.2$ V, and $(W/L)_{\text{cal}} = 2\,\mu$m/100 nm).

as shown in Eq. (21). Based on the assumption, an input transistor and a bypass transistor could be substituted with an equivalent transistor whose effective V_{GS} is $V_{\text{eff\_c}}$;

$$\frac{1}{2}\left((\mu C_{\text{OX}})_{\text{in}}\left(\frac{W}{L}\right)_{\text{in}} + (\mu C_{\text{OX}})_{\text{cal}}\left(\frac{W}{L}\right)_{\text{cal}}\right) V_{\text{eff\_c}}^2 \equiv I_{\text{DS\_in\_ideal}} + I_{\text{DS\_cal\_ideal}} \quad (71)$$

$$V_{\text{eff\_c}} = \sqrt{\frac{(\mu C_{\text{OX}})_{\text{in}}\left(\frac{W}{L}\right)_{\text{in}} V_{\text{eff\_in}}^2 + (\mu C_{\text{OX}})_{\text{cal}}\left(\frac{W}{L}\right)_{\text{cal}} V_{\text{eff\_call}}^2}{(\mu C_{\text{OX}})_{\text{in}}\left(\frac{W}{L}\right)_{\text{in}} + (\mu C_{\text{OX}})_{\text{cal}}\left(\frac{W}{L}\right)_{\text{cal}}}}. \quad (72)$$

Substituting Eq. (72) into Eqs. (67) and (69), G_{amp} and $G_{\text{amp\_cal}}$ of the current calibration are calculated and Eq. (70) becomes

$$v_{\text{in\_diff\_cal}} \approx \frac{\overline{g_{\text{m\_cal}}}}{\overline{g_{\text{m\_in}}}}\left(N_{\text{Code}} - 2^{N_{\text{cal}}-1}\right) v_{\text{d}}. \quad (73)$$

Figure 22 compares the estimation with simulation results. Input-referred compensated voltage of 1 LSB is designed as 1.5 mV. To cover 5σ, calibration resolution is set as 7 bits. Under the condition of Fig. 22, v_{d} is calculated as about 4.06 mV. However, to match the simulation results, v_{d} should be 4.42 mV and this error causes gradient difference between the estimation and the simulation results in Fig. 22.

4.3 Mismatch

A bypass transistor induces mismatch and increases offset

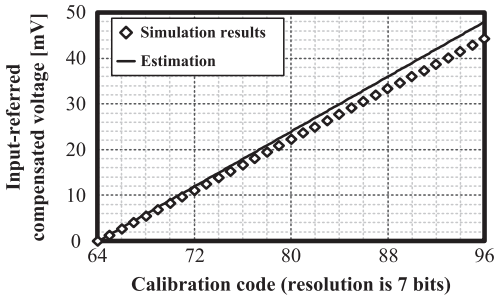

Fig. 22 Input-referred compensated voltage by the current calibration (V_{dd} = 1.0 V, V_{com_in} = 0.5 V, V_{com_cal} = 0.4 V, and $(W/L)_{cal}$ = 1 μm/100 nm).

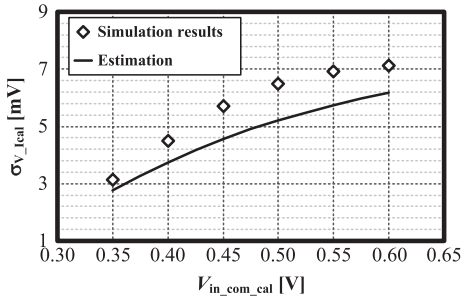

Fig. 23 σ_{V_Ical} due to the current calibration (V_{dd} = 1.0 V, V_{in_com} = 0.5 V, $(W/L)_{cal}$ = 1 μm/100 nm, and a number of the Monte Carlo simulation is 500).

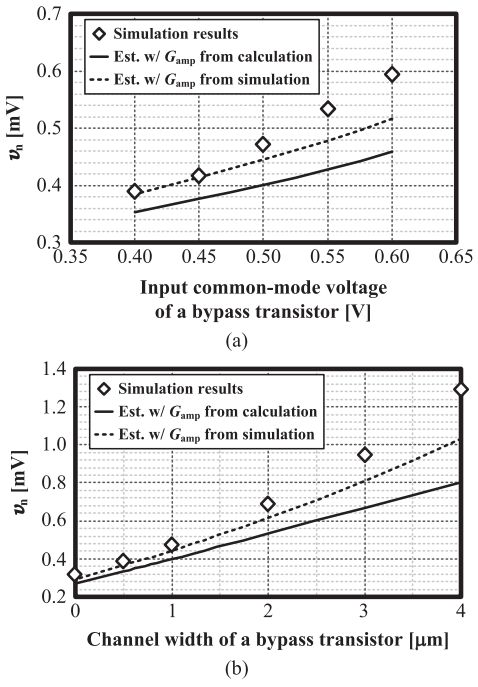

Fig. 24 Input-referred thermal noise with the current calibration (a) influence of input common-mode voltage and (b) influence of channel width of a bypass transistor (V_{dd} = 1.0 V, V_{in_com} = $V_{in\_com\_cal}$ = 0.5 V, $(W/L)_{cal}$ = 1 μm/100 nm, $C = 5C_{PL}$, T = 300 K, γ = 2/3, and a number of the simulation is 500).

voltage. Assuming v_{cal_diff} is 0 V, let's deduce an offset voltage, σ_{V_Ical}, due to a pair of calibration transistors. From Eq. (73), offset voltage is

$$\sigma_{V\_Ical} = \frac{\overline{g_{m\_cal}}}{\overline{g_{m\_in}}}\sigma_{V\_Ical\_mis} \tag{74}$$

where $\sigma_{V\_Ical\_mis}$ is a mismatch of bypass transistors. Figure 23 shows the comparison between Eq. (74) and simulation results.

4.4 Thermal Noise

A bypass transistor not only induces thermal noise but also decreases the gain of pre-amplifier, thus expands dead-zone. Input-referred thermal noise due to an input transistor and a calibration transistor is expressed as below;

$$\begin{aligned}\overline{v_{n\_MOS}^2} &\equiv \overline{v_{n\_MOS\_in}^2} + \overline{v_{n\_MOS\_cal}^2} \\ &= \frac{2kT\gamma}{C\left|G_{amp}\right|}\left(1+\frac{\overline{g_{m\_cal}}}{\overline{g_{m\_in}}}\right) \\ &\quad\times\left(1-\frac{(g_{DS\_in}+g_{DS\_cal})\times(V_{dd}-V_{eff\_c})}{2\left(\overline{I_{DS\_in}}+\overline{I_{DS\_cal}}\right)}\right)^{-1}\end{aligned} \tag{75}$$

In the initial noise of Eq. (29), time constant is changed due to a bypass transistor;

$$\tau_2 = \frac{C}{\lambda I_{DS\_ideal} + \lambda_{cal} I_{DS\_cal\_ideal}} \tag{76}$$

Assuming the gain of pre-amplifier is sufficiently large, thermal noise of the second stage may be ignored. Consequently, the input-referred thermal noise of the current calibration is deduced as below;

$$\begin{aligned}\overline{v_n^2} &= \frac{4kT\gamma}{C\left|G_{amp}\right|}\left(1+\frac{\overline{g_{m\_cal}}}{\overline{g_{m\_in}}}\right) \\ &\quad\times\left(1-\frac{(g_{DS\_in}+g_{DS\_cal})\times(V_{dd}-V_{eff\_c})}{2\left(\overline{I_{DS\_in}}+\overline{I_{DS\_cal}}\right)}\right)^{-1} \\ &\quad+\frac{2kT}{CG_{amp}^2}\exp\left(-\frac{t_1}{\tau_2}\right)\end{aligned} \tag{77}$$

Figures 24 compares the estimation with simulation results.

The current calibration can reduce regeneration time due to the drain current of a bypass transistor. However, additional transistors attenuate a ratio of the signal current to the drain current expressed in Eq. (23), and the results are shown in Fig. 21. The additional transistors also increase dead-zone as shown in Fig. 24.

4.5 PVT Variation

PVT variation degrades compensation accuracy. In this section, only voltage fluctuation and temperature change are considered.

From Eq. (73), compensated voltage will be varied as voltage and temperature are changed. This is because

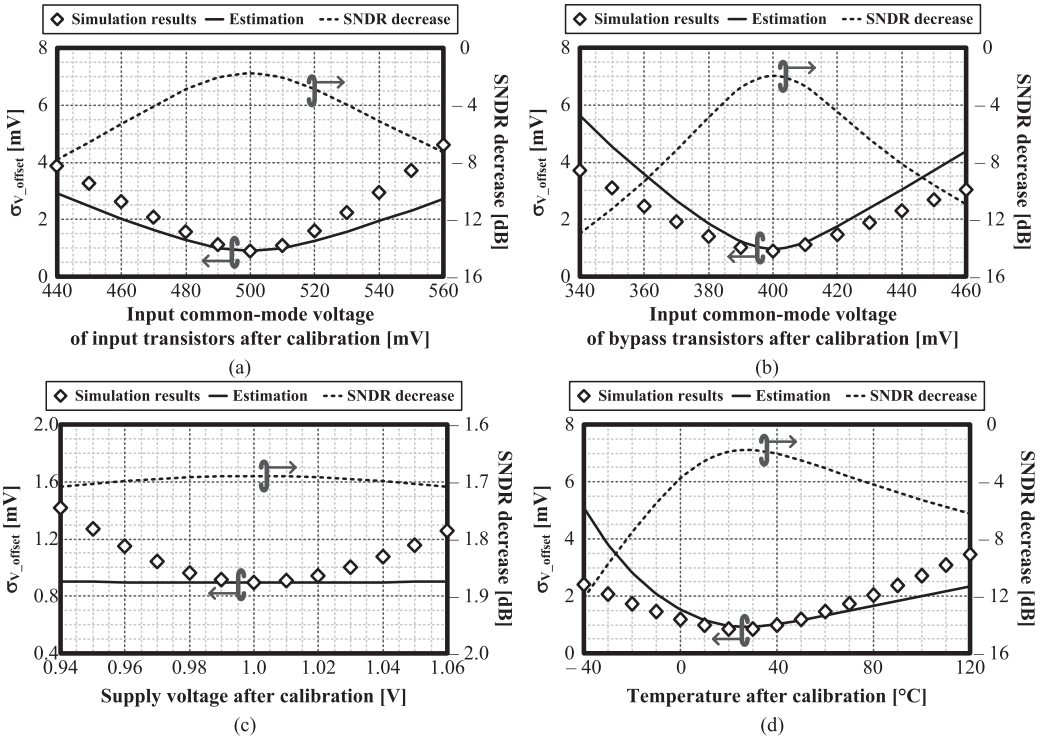

Fig. 25 Influence of PVT variation on the current calibration. (a) input common-mode voltage of input transistors, (b) input common-mode voltage of bypass transistors, (c) supply voltage, and (d) temperature (1 LSB = 4.5 mV and a number of the Monte Carlo simulation is 500).

transconductances of an input transistor and a bypass transistor are affected by those variation. Thus, input-referred compensated voltages also change and the variation differs in each $v_{\mathrm{cal\_diff}}$. From Eq. (73), $\sigma_{\mathrm{V\_PVT}}$ is

$$\sigma_{\mathrm{V\_PVT}} = \frac{\overline{g_{\mathrm{m\_cal}}}}{\overline{g_{\mathrm{m\_in}}}} \times \sqrt{\left(\frac{\Delta\overline{g_{\mathrm{m\_cal}}}}{\overline{g_{\mathrm{m\_cal}}}} - \frac{\Delta\overline{g_{\mathrm{m\_in}}}}{\overline{g_{\mathrm{m\_in}}}}\right)^2} \times v_{\mathrm{d}}\sigma_{\mathrm{code}}. \quad (78)$$

Figure 25 compares the estimation with simulation results. Calibration is conducted when V_{dd} is 1.0 V, $V_{\mathrm{in\_com}}$ is 0.5 V, $V_{\mathrm{in\_com\_cal}}$ is 0.4 V, $(W/L)_{\mathrm{cal}}$ is 1 μm/100 nm, and T is 27°C. Figure 25 also shows SNDR decrease, which is calculated from estimated $\sigma_{\mathrm{V\_offset}}$.

5. Comparison

In Table 2, two calibration methods are compared. Comparison criteria are the same step size of input-referred compensated voltage and covering a range of $5\sigma_{\mathrm{V\_offset}}$. Thus, for the comparison, the capacitance calibration is set as 6 bits and a unit PMOS capacitor is sized as $W/L = 600$ nm/100 nm when input common-mode voltage is 0.5 V. In the current calibration, size of a bypass transistor is designed as $W/L = 1\,\mu$m/100 nm. This is because, a narrow width increases mismatch and is hard to cover a calibration range of $5\sigma_{\mathrm{V\_offset}}$, and a wide width increases thermal noise. When $(W/L)_{\mathrm{cal}}$ is designed as 1 μm/100 nm, as expressed in Eqs. (33), (74), and (75), input-referred offset voltage and thermal noise voltage caused by bypass transistors are $1/\sqrt{2}$ of those caused by input transistors, respectively. To suppress influence of PVT variation as addressed in Sect. 4.5, input common-mode voltage of a bypass transistor is set as the same voltage of an input transistor.

Table 2 Comparison of the calibration methods.

Comparison \ Calibration		w/o calibration circuit	w/ calibration circuit	
			Capacitor	Current
Calibration resolution [bits]		0	6	7
$\sigma_{\mathrm{V\_offset}}$ [mV]	due to cal.	0	0.702	6.49
	after cal.	9.85	0.417	0.969
v_{n} [mV]		0.689	0.259	1.12
t_{reg} [ps] @$V_{\mathrm{in\_com}}$ = 0.5 V		130	347	123
SNDR decrease [dB] @1 LSB = 4.5 mV		– 17.7	– 0.580	– 3.62
Energy per a comparison [fJ]		64.2	246	67.2

(A step of input-referred compensated voltage is 1.5 mV and calibration covers about $5\sigma_{\mathrm{V\_offset}}$)

In the maximum available range, the current calibration can compensate wider range than the capacitance calibration. From Eqs. (62) and (73), the maximum available range of each calibration method is calculated. When the influence of λ is negligible in the capacitance calibration, its

maximum range is expressed as

$$v_{\text{in\_diff\_cal\_max}} \approx \frac{C_{\text{on}} - C_{\text{off}}}{C_{\text{on}} + C_{\text{off}}} \times V_{\text{eff}}. \quad (79)$$

When $V_{\text{in\_com}}$ and $V_{\text{in\_com\_cal}}$ are the same in the current calibration, its maximum range is expressed as

$$v_{\text{in\_diff\_cal\_max}} \approx \frac{W_{\text{cal}}}{W_{\text{in}}} \times V_{\text{eff}}. \quad (80)$$

In the above condition, $W_{\text{cal}}/W_{\text{in}}$ is larger than $(C_{\text{on}} - C_{\text{off}})/(C_{\text{on}} + C_{\text{off}})$.

6. Conclusions

This work analyzed a dynamic amplifier and a pseudo-differential dynamic comparator with calibration circuits. The analyzed comparator uses 90-nm CMOS process as an example. The gain of dynamic amplifier was expressed by a ratio of V_{dd} to V_{eff} and λ of an input transistor. The estimations thoroughly explained the influences of each parameters and were compared with simulation results. Based on the deduced gain, the capacitance calibration and the current calibration were analyzed. Two calibration methods have different pros and cons. The capacitance calibration has a narrower dead-zone, but a slower response speed. By using back-ground calibration, the capacitance calibration can become more tolerant to PVT variation. The current calibration is faster and more robust to in PVT variation if input common-mode voltages of the input transistors and the bypass transistors are the same. The dead-zone of the current calibration can be reduced by increasing the load capacitance of a pre-amplifier.

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