広ロックレンジ 20GHz プログレッシブミキシング周波数分周器
A Progressive Mixing 20GHz ILFD with Wide Locking Range for Higher Division Ratios

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1. Introduction

Modern high frequency PLL systems employ high frequency dividers in the initial division stages. These dividers consume a considerable percentage of the total PLL power consumption [1]. They are implemented as Current Model Logic (CML) dividers and Injection Locked Frequency Dividers (ILFD). CML dividers are more robust but consume high power. ILFDs on the other hand consume much less power and can divide by higher than 2 which further saves power. However, they suffer from narrow locking range especially for higher division ratios. Most ILFDs use the same principle of direct mixing to generate the correct harmonic to be injected into the oscillator for locking as shown in Fig.1(a). As this method is not suitable for higher division ratios, progressive mixing [2] is proposed to enhance the locking range. It performs a multistep mixing that uses much stronger harmonics in the mixing process to widen the locking range.

2. Progressive Mixing ILFD

The proposed PMILFD uses a multistep conversion model. In this model the injected signal at the Nth harmonic mixes with the (N/2)th harmonic of the oscillator fundamental frequency and then again by the (N/4)th and so on log N times until a harmonic that is close to the oscillator fundamental is generated. For a divide-by-4 configuration as shown in Fig.1(b), the injected signal mixes with the second harmonic and fundamental to generate the injection signal. The main advantage is that the injected signal mixes first with the (N/2)th harmonic instead of the conventional (N-1)th since the former is much stronger than the later and thus will produce a stronger injection signal. A feature of such architecture is that intermediate stages can also be used as injection points for lower division ratios. The divide-by-4 circuit consists of a 4-stage ring oscillator as shown in Fig.2. PMOS transistors are used for the delay cell to allow frequency tuning. Tail transistors of each stage were connected as shown in the figure to form a 2-stage ring oscillator running at twice the fundamental frequency. Additional tail transistors M5 and M6 are used to facilitate injection and to act as current sources. The gates of transistors M1 and M3 are used as a second input (RF2) if the PMILFD is to be used as a divide-by-2 circuit.

3. Measurement Results

A divide-by-4 PMILFD is fabricated in 65nm CMOS process. It consumes a 3.9mW from a 1.2V supply and has a free-running tuning range from 2GHz to 8GHz. Fig.3 shows the locking range for divide-by-4 operation with injection applied to (RF4) terminals and (RF2) terminals are grounded. The locking range is 3.7GHz (39.7%) and up to 7.9GHz (31.4%) at the highest frequency. As for divide-by-2 operation with input applied to (RF2) terminals and (RF4) terminals are grounded, locking range is 2.5GHz (53.7%) and up to 11.6GHz (92.1%) at the highest frequency. The proposed divider almost doubles the widest locking range reported to date for a divide-by-4 ILFDs.

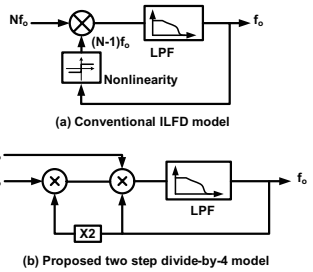

Fig. 1. ILFD models: (a) Conventional (b) Proposed two-step divide-by-4

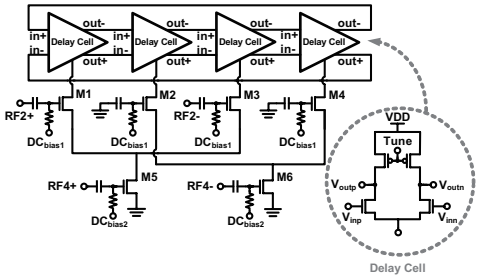

Fig.2. Proposed PMILFD divide-by-4 circuit.

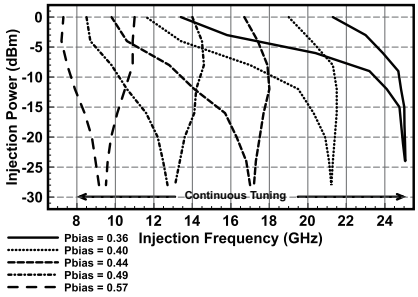

Fig 3. Divide-by-4 locking range

4. Conclusion

Progressive Mixing technique is proposed to enhance the locking range of higher division ratio ILFDs. It achieves the widest locking range published to date and is extendable to higher division ratios to further save power consumption.

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References

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[2] A. Musa, *et al*., IEEE A-SSCC, pp.85-88, Nov. 2011.