A Comparison between Common-source and Cascode Topologies for 60GHz Amplifier Design in 65nm CMOS

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Outline

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- Topologies used in this work
  - Common-source (CS) versus Cascode (Cas.) topology
  - Gain-boost Cascode (Cas.) topology
- One stage power amplifier using CS and gain-boost topologies
- Measurememt results
- Conclusion

CS topology at mmW frequency

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◆The features of CS Topology comparing with Cas. Topology

- ✓ Small noise figure
- ✓ Reasonable power gain
- ✕Larger power consumption
- ✕Worse instability factor

Cas. topology at mmW frequency

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- At lower frequencies, obtains a high gain.
- At mmW frequencies, a reduction of the reverse isolation S_{12}.
  - ✓ Increase maximum gain
  - ✓ Increase stability
  - ✕ Larger parasitic capacitance in the inter-stage node

Cas. structure with inductance (1)

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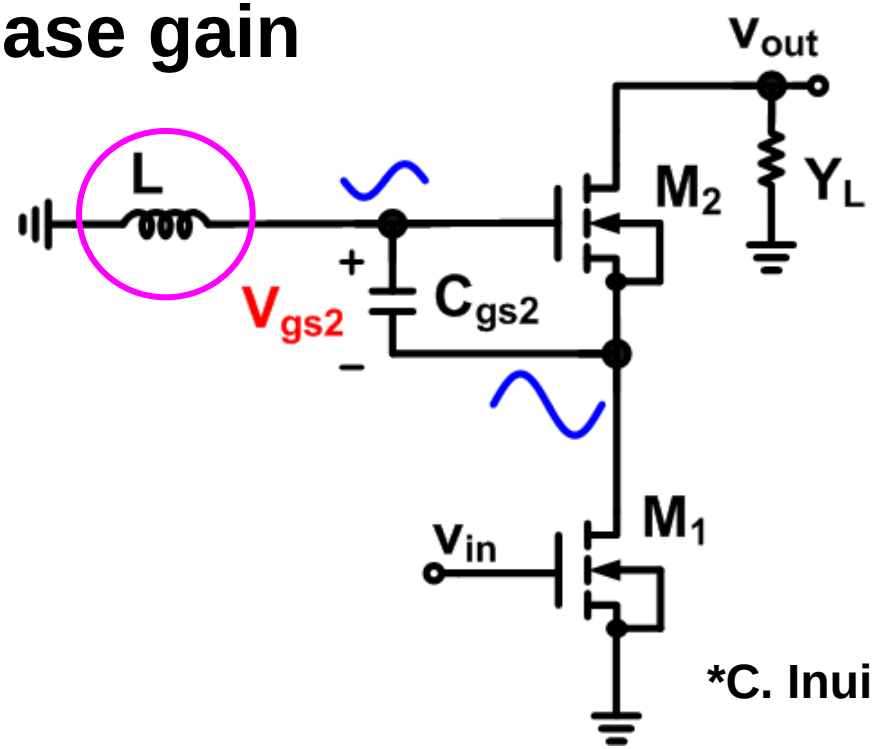
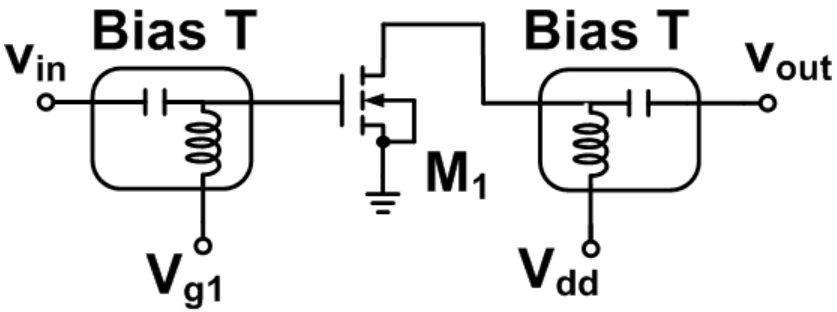
- **Large parasitic capacitance decreases the gain**
  - **Gain-boost technique is utilized to increase gain**



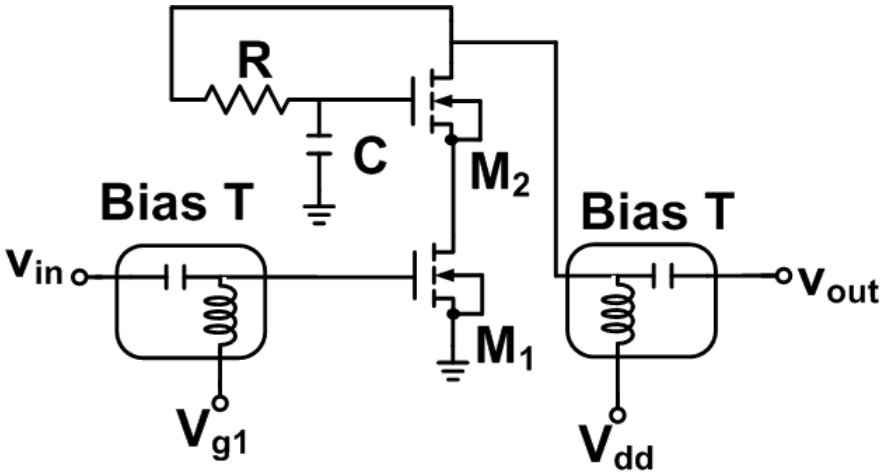
*C. Inui, et al, *APMC*, Dec. 2007

Cascode topology with inductance

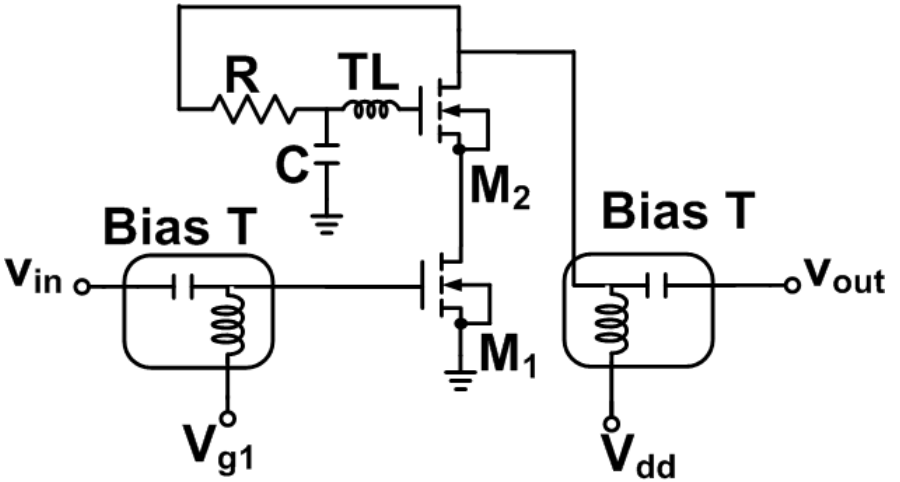
The TEG schematics of the topologies



CS

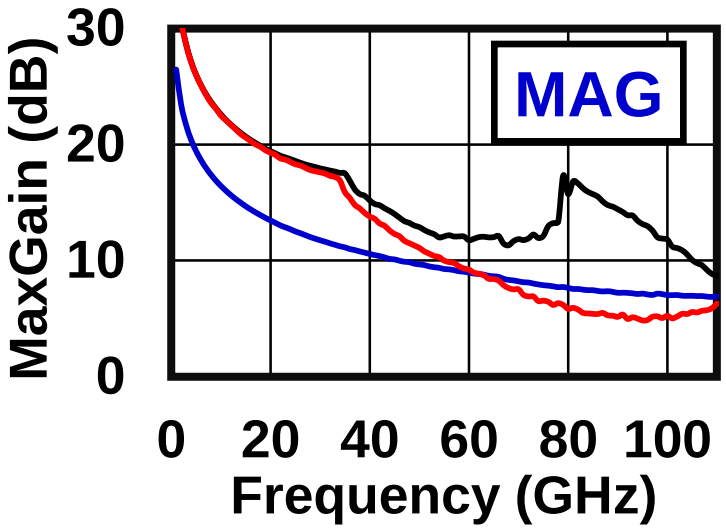


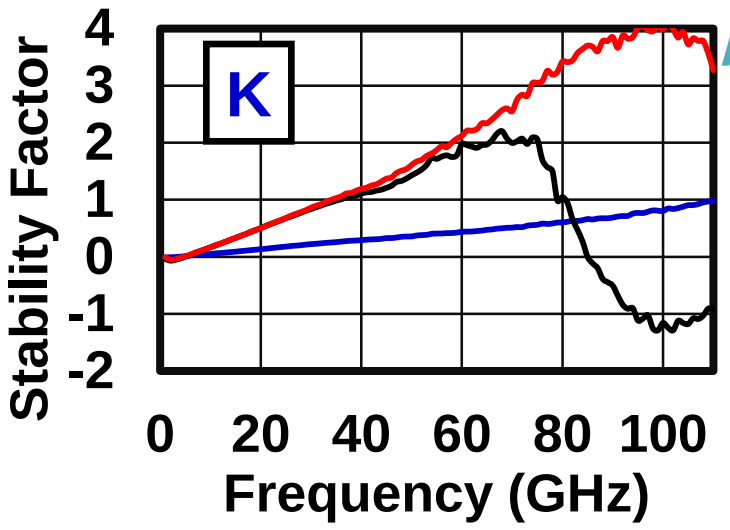
Cas.

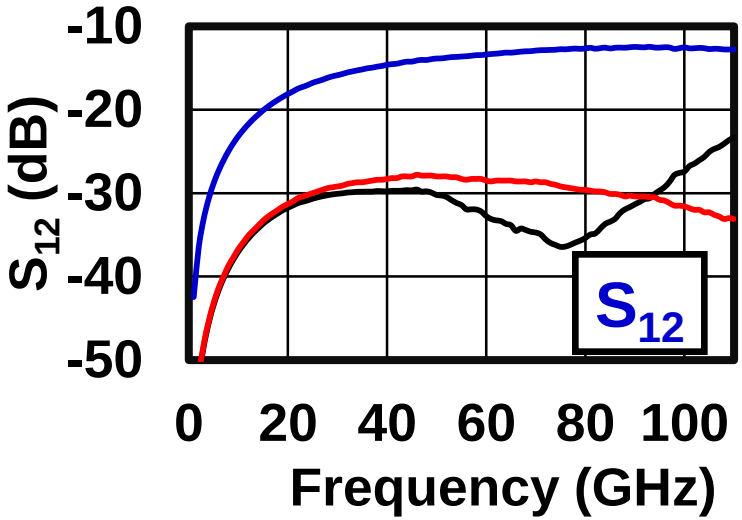


Gain-boost Cas.

Comparison between CS and Cas. TEGs







Line color	No. of finger (CS & CG)	Wf (μm)	TL (μm)	Power (mW)
Blue_CS	20	2	0	8.3
Red_Cas.	20 & 20	2	0	5.8
Black_Cas.	20 & 20	2	80	6.0

V_{dd}=1.2 V, V_{g1}=0.6 V

1-stage amp. using CS topology

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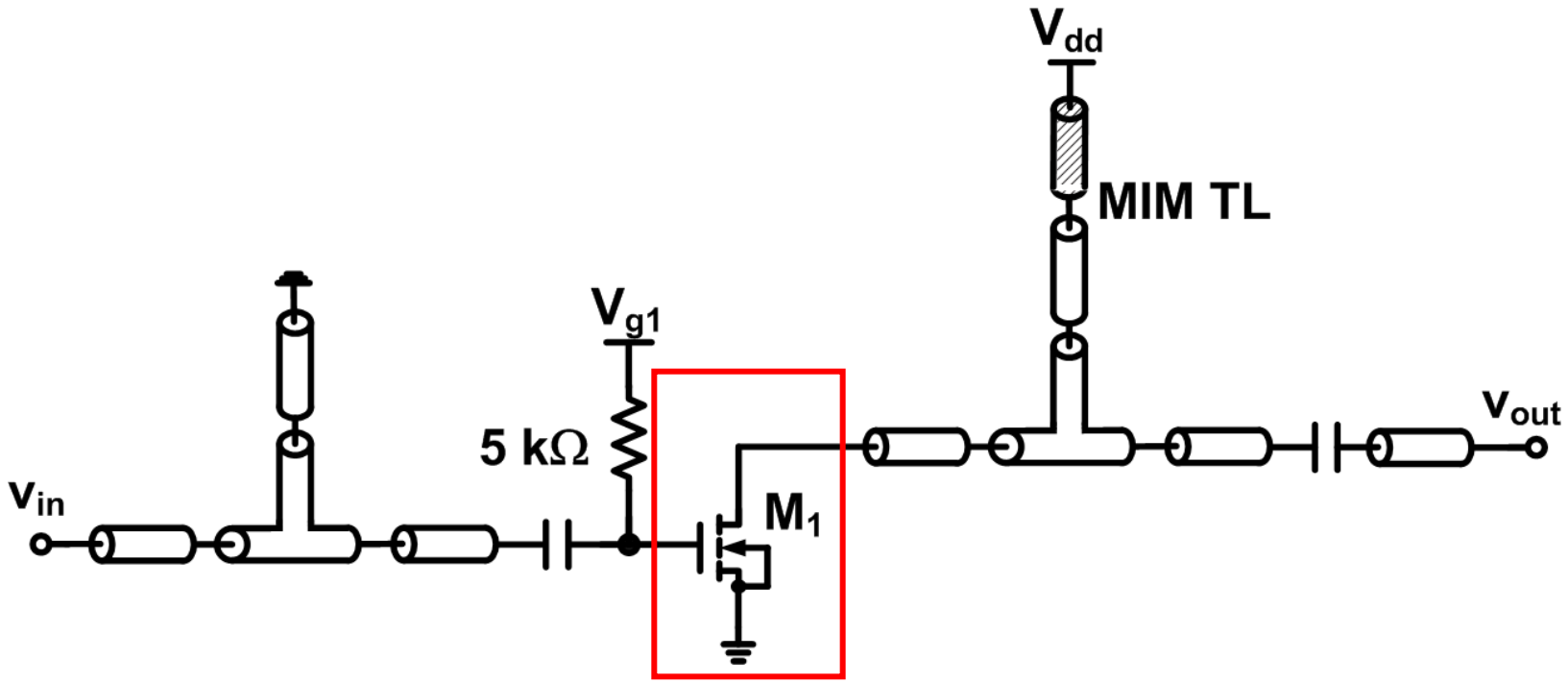
- TL are utilized for impedance matching
- Decoupling MIM transmission line is used for AC ground
- CS transistor size:20×2μm



1-stage amp. using Cas. topology

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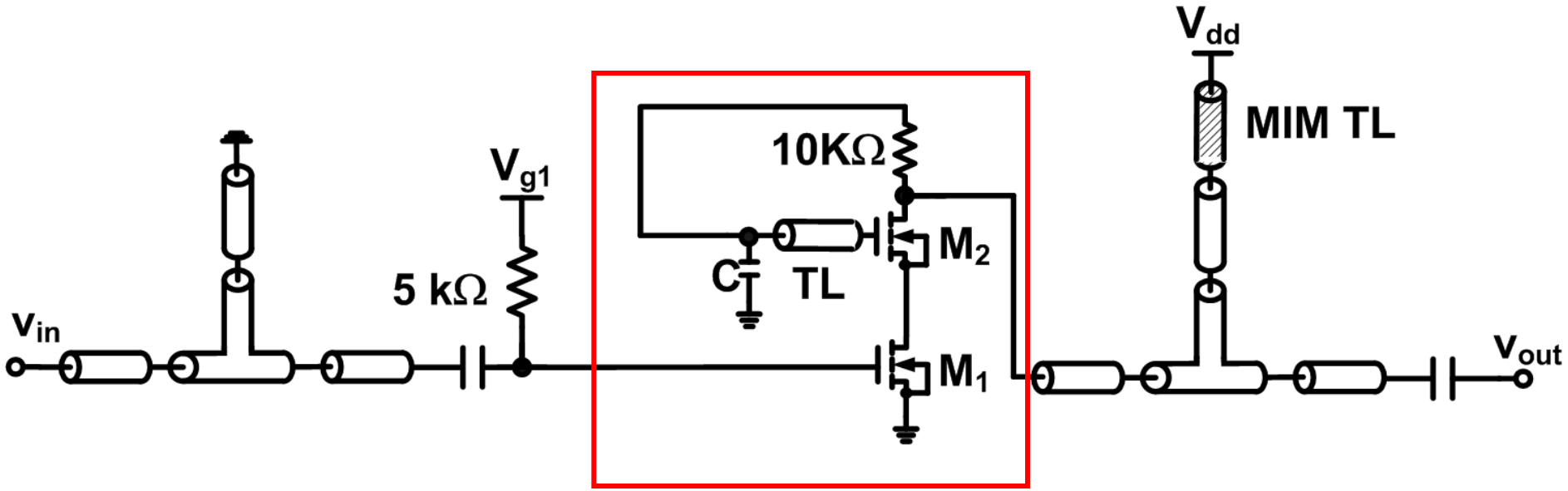
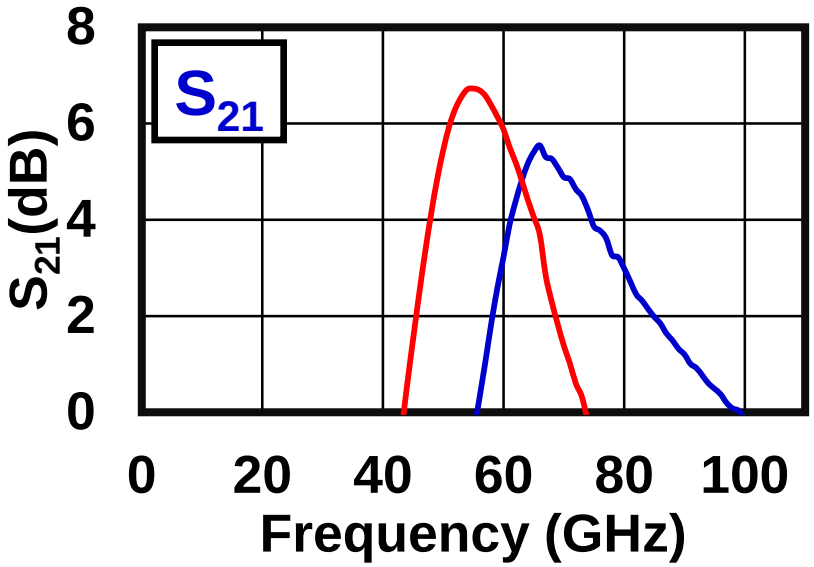
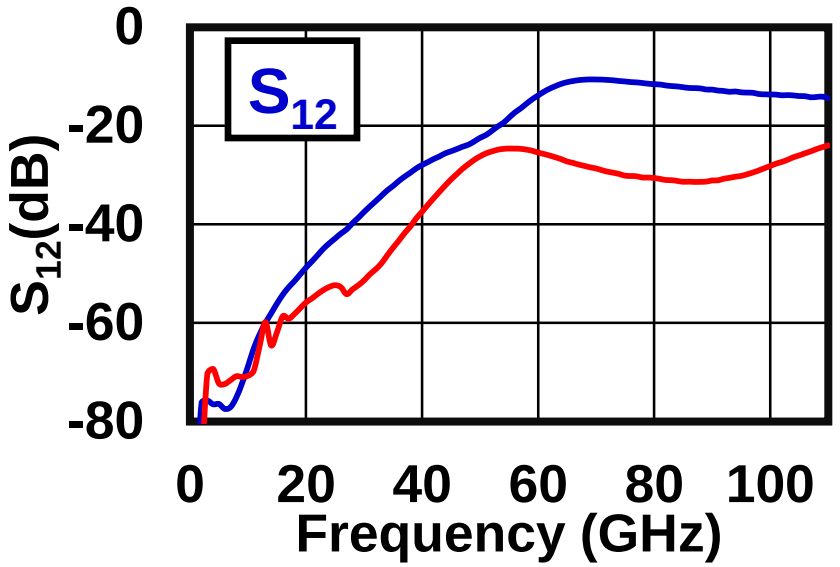
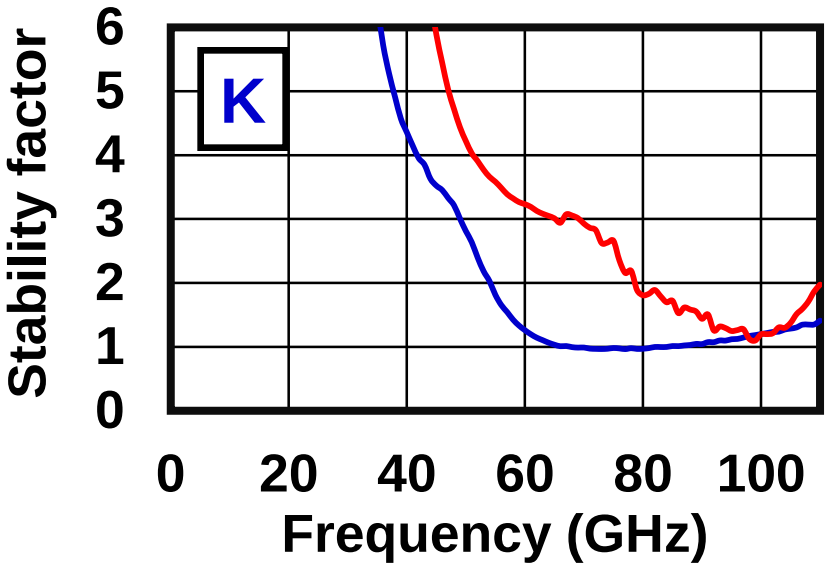
◆Cas. TEG size: CS=20×2μm, CG=20×2μm, TL=80μm.



Measured results of CS and Cas. amps(1)





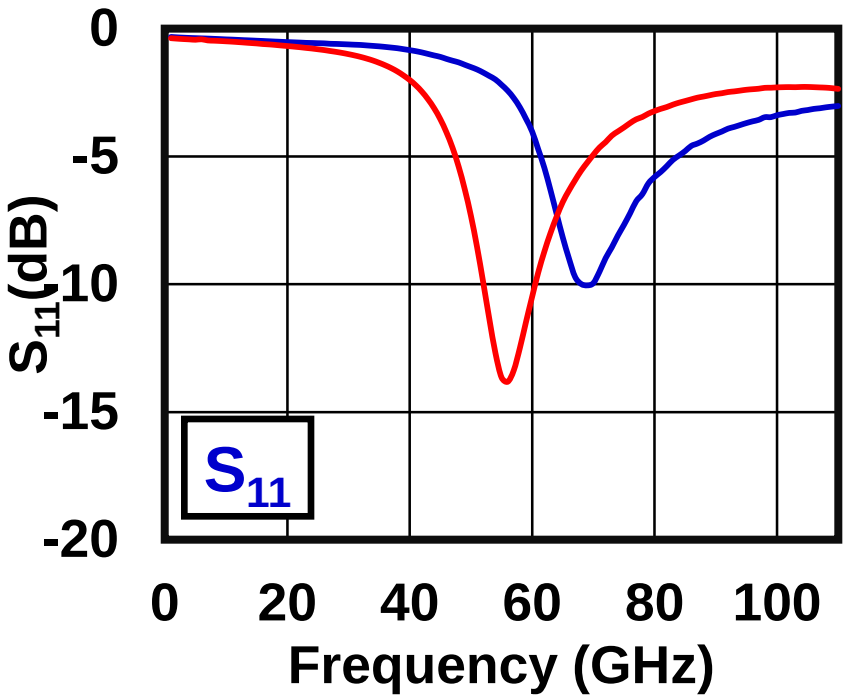


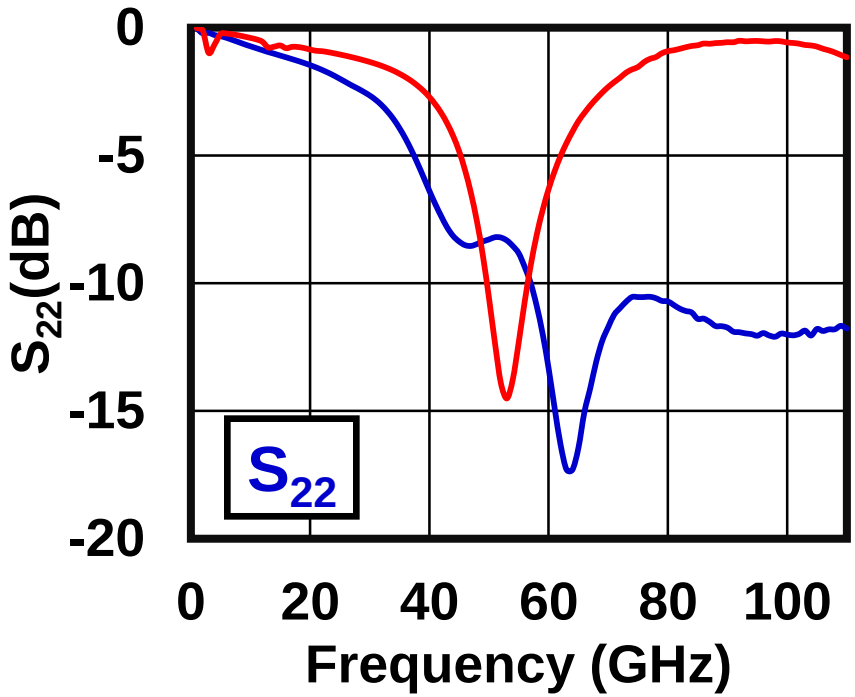
Red: Cas.

Blue: CS

V_{dd}=1.2 V, V_{g1}=0.6 V

Measured results of CS and Cas. amps(2)





V_{dd}=1.2 V, V_{g1}=0.6 V

Red: Cas. , Blue: CS

Summary of the comparison (1)

TEG	MAG (dB) (60GHz)	S_{12}(dB) (60GHz)	K (60GHz)	Power (mW)
CS	9	-13	0.5	8.3
Cas.	9	-28	2.1	5.8
Gain-boost Cas.	12	-33	2.0	6.0

Ampifier	Freq. (GHz)	S_{11} (dB)	S_{22} (dB)	S_{12} (dB)	S_{21} (dB)	K	Power (mW)
CS	66	-9	-15	-11	5.5	1.0	8.3
Gain-boost Cas.	56	-14	-11	-25	6.7	3.5	6.0

V_{dd}=1.2 V, V_{g1}=0.6 V

MaxGain and output power versus power

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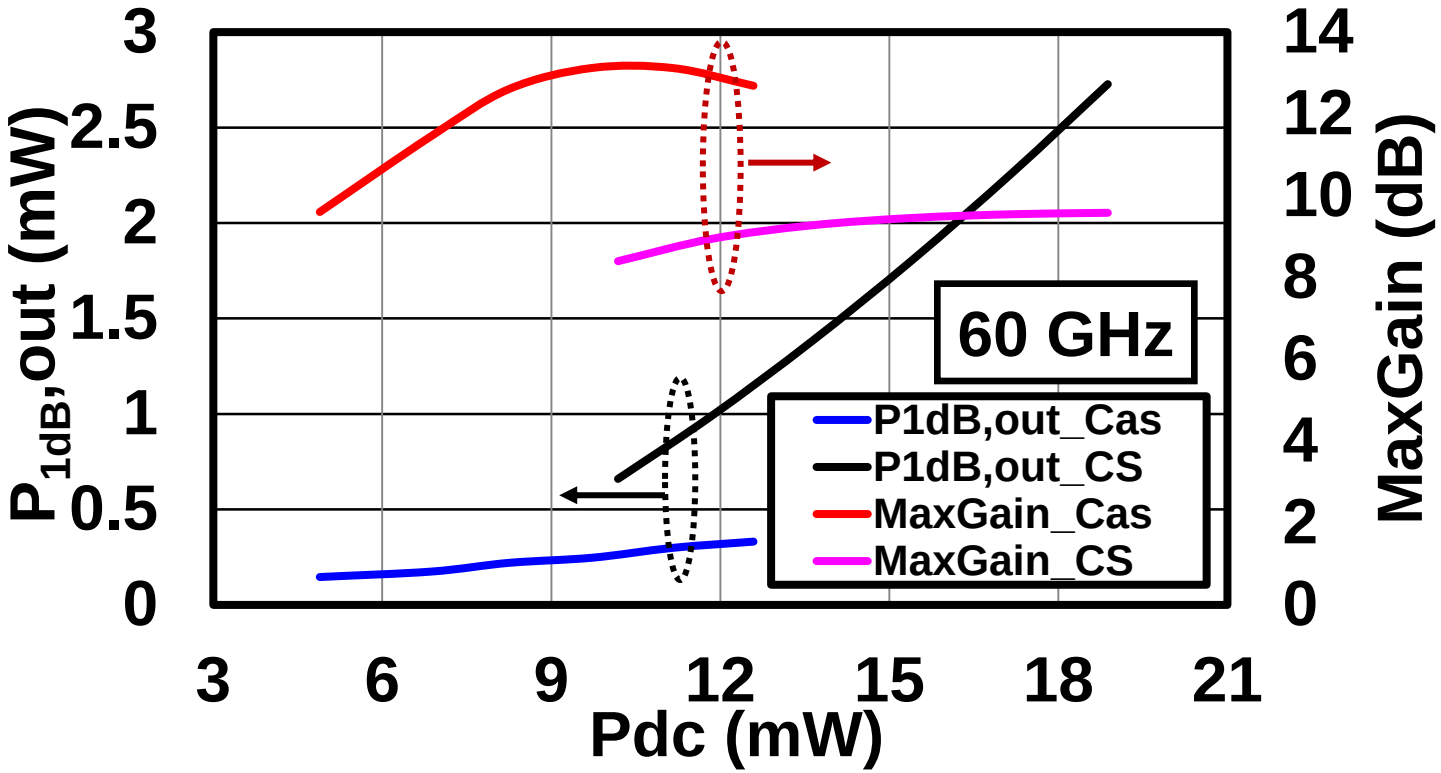
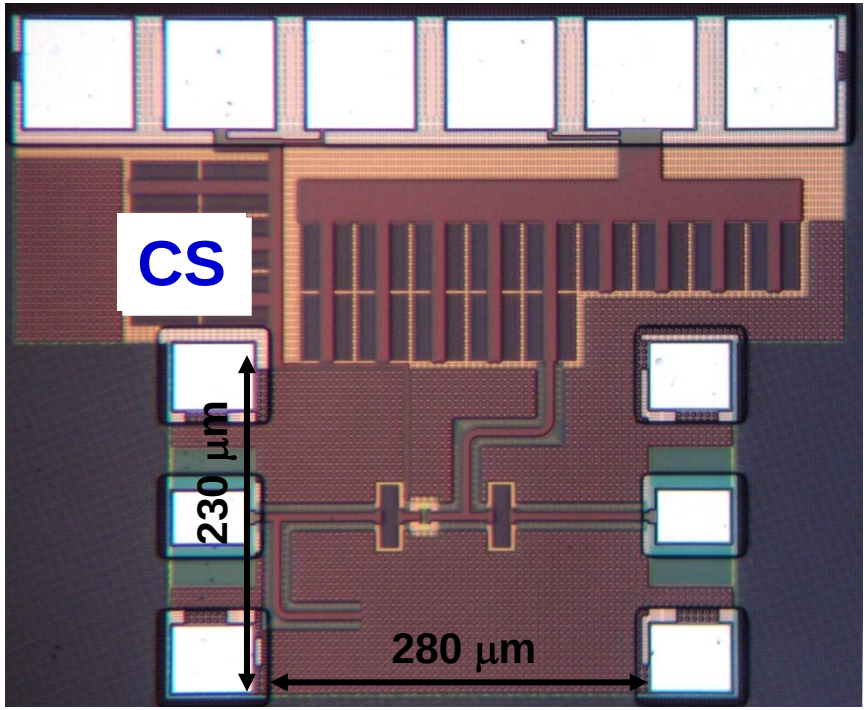
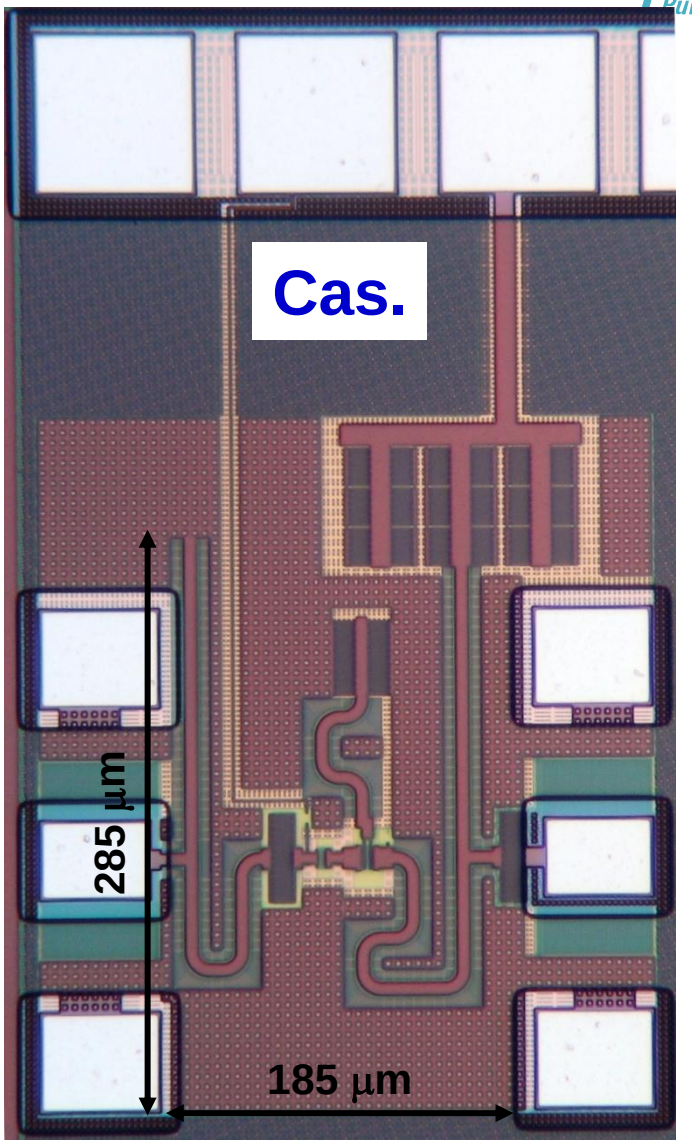
Simulation results



- The maximum gain of the Cas. topology is much larger than CS topology with less power consumption
- The output power at P_{1dB} of the CS topology is larger than the CS topology

Chip photos





65nm CMOS process

CS: 0.064 mm²

Cas.: 0.053 mm²

Conclusion

- The comparison of CS, Cas. and gain-boost Cas. topologies are carried out in 65nm CMOS process.
- Gain-boost technique is studied to increase the gain of cascode topology.
- 1-stage amplifiers are designed utilizing CS and gain-boost Cas. topologies
- The gain-boost Cas. topology have large gain, better isolation and stability factor with less power consumption at 60GHz than the CS topology.
- The 1-stage amplifier utilizing gain-boost Cas. topology achieves smaller output power than that utilizing the CS topology.

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Thank you

Q&A

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