Analog and RF circuits design and future devices interaction

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Abstract

This paper reviews and discusses the recent progress of analog and RF circuits design and the future devices interaction, focusing on the millimeter wave RF circuits and ADCs. With the scaling of CMOS technology, f_T and f_{max} are increased. Using an advanced CMOS process and techniques such as the negative capacitance, the gain flattening, the accurate impedance matching using transmission lines, and the injection locking, a 60 GHz CMOS transceiver is realized. It attains 16 Gbps data transmission with the 16 QAM method. A dynamic comparator using a dynamic pre-amplifier with capacitive digital offset voltage compensation realizes a small mismatch voltage, low noise, low power, and low voltage operation without any static current. Flash ADCs and SAR ADCs using dynamic comparators have progressed. The interpolation method can ease the gain requirement for OpAmp in pipelined ADCs. The interconnection structure should be considered to realize low loss transmission lines and high density and large capacitance ratio MOM capacitors.

RF circuit design

A continuous channel length reduction by the technology scaling has increased the f_T and f_{max} of a MOS transistor (Fig. 1). The current available f_{max} of a MOS transistor reaches 300 GHz, and the high frequency operation of millimeter wave, e.g. 60 GHz [1] and THz range [2], have been attained.

We have realized a CMOS 60 GHz direct-conversion transceiver using 65 nm and 40 nm CMOS devices (Fig. 2) and attained an all-channel 7 Gbps data transmission using the 16 QAM modulation with a small power consumption [1]. The highest data rate of 16 Gbps has been achieved (Fig. 3). The maximum gain, G_{max}, and the minimum noise figure, NF, can be expressed as,

$$G_{\max} \approx \frac{f_{\max}}{f_c} \qquad (1)$$

$$NF\min \approx 1 + \left(\frac{f_c}{f_T}\right)\sqrt{1.3 g_m\left(R_g + R_s\right)} \qquad (2)$$

where f_c is the carrier frequency, g_m is the transconductance, and R_g and R_s are the gate resistance and the source resistance, respectively. An essential RF circuit design method is therefore to draw the ultimate potential from the transistors by accurate and low loss impedance matching. Capacitance compensation by using negative capacitance in a differential circuit is an effective method to increase the amplifier's gain at high frequency operation (Fig. 4). In addition, an accurate device modeling, such as the de-embedding method, and a good decoupling circuit are vital. The 16 QAM modulation can increase the data rate twice compared with a conventional QPSK modulation for the same signal bandwidth. However, any gain fluctuation over the wide frequency range causes interference between the signals and degrades the constellation. This ultimately increases the bit error rate for the QAM signal (Fig. 5). Therefore, the center frequency of each resonator in the cascaded amplifiers should be well controlled by matching the impedance accurately. We use transmission lines for impedance matching due to its accurate parameters and high scalability over the distance.

The other important design point to realize the 16 QAM modulation is to reduce the phase noise of the I/Q VCOs. The QPSK modulation doesn't require low phase noise so much; however, lower phase noise, e.g. less than -90 dBc/Hz at 1 MHz, is required for 16 QAM modulation (Fig. 6). It is quite difficult to realize a low phase noise 60 GHz I/Q VCO due to the low quality factor. Furthermore a wide frequency range of 9 GHz should be realized to address the 4 channel selections. We used 60 GHz I/Q VCOs with an injection locking technique from a 20 GHz PLL [3]. A CMOS VCO exhibits the minimum phase noise at around 20 GHz and it is not so difficult to realize the tuning range of 3 GHz without a serious degradation of phase noise. The phase noise of the injection locked oscillator, PN_{ILO}, is expressed as,

$$PN_{ILO} = PN_{INJ} + 20\log N \qquad (3)$$

where PN_{INJ} is the phase noise of the injection oscillator and N

is the ratio between the frequencies. N is three in this case and a degradation of 9.5 dB is suffered. We have realized a sufficiently low phase noise of -95 dBc at 1 MHz for the 60 GHz I/Q VCOs, which is 20 dB superior than the previous work [4] and opens a new vista to the direct conversion and the use of 16 QAM to increase the data rate twice compared with the conventional QPSK method for 60 GHz transceivers (Fig. 7).

In the future, f_T and f_{max} and the performances of the high frequency circuits, e.g. NF, gain, and phase noise, will progress and the power consumption will be reduced. Furthermore, the total system integration to combine the RF and the baseband circuit will be realized to reduce the total system cost. However the interconnection structure should be addressed to realize a low loss transmission line (Fig. 8). The attenuation factor of the transmission line is,

$$a = \frac{R}{2Z_0} \approx \frac{R_u C_u}{2\sqrt{\varepsilon\mu}} \qquad (4)$$

Therefore, thinner and lower interconnection increases the transmission loss. Also, PMOS devices will be used to form complementary amplifiers to improve the power efficiency. However, the HCI reliability of CMOS transistors will become more serious and the operating voltage should be lowered. This however reduces the RF power and decreases the power efficiency. A future device interaction is strongly required to improve this issue.

ADC design

ADCs have different architectures (Fig. 9) and suitable performance areas [5] (Fig. 10) and can be classified into the comparator-based ADCs and the OpAmp-based ADCs. The flash ADC and the SAR (Successive Approximation Register) ADC are the comparator-based ADCs that do not require OpAmps and are suitable for low resolution conversion. The flash ADC realizes an ultra-high speed conversion and the SAR ADC realizes an ultra-low power conversion. The pipelined ADC and the sigma-delta ADC are the OpAmp-based ADCs that require OpAmps. The pipelined ADC is suitable for a moderate resolution and high speed conversion and the sigma-delta ADC is suitable for low speed yet very high resolution conversion. The technology scaling decreases the operating voltage and the amplifier gain. This makes the OpAmp design more difficult. Therefore, the comparator-based ADCs are more suitable for the scaled CMOS technology.

A dynamic comparator that does not consume any static power is currently used (Fig. 11) [6]. An offset voltage mismatch between the comparators determines the effective resolution of the flash ADCs. Transistors M_1 and M_2 determine the mismatch and a larger gate size is required to reduce the mismatch; however, this results in an increase of power consumption. Hence, the digital mismatch compensation is used. The mismatch voltage change is described by the following,

$$\Delta V_{os} \approx \frac{V_{eff}}{2}\left(\frac{\Delta C_L}{C_L} - \frac{\Delta I_D}{I_D}\right) \qquad (5)$$

where V_{eff} is the effective gate voltage ($=V_{GS}-V_T$), C_L is the load capacitance, and I_D is the drain current of M_1 and M_2. The compensation techniques generally fall into two categories: the change of the drain current using extra transistors or the change of the load capacitance. We used a small size CDAC with an up-down counter to reduce the mismatch from about 70 mV_{pp} to 6 mV_{pp} (Fig. 12). Very small MOM (Metal Oxide Metal) capacitor (~0.1 fF) is very useful. Fig. 13 shows a 5 bit, 2.3 GSps flash ADC for the analog baseband of the 60 GHz transceiver [7]. It consumes only 12 mW and occupies 0.06 mm^2 in a 40 nm CMOS. This proposed comparator can operate at 0.5 V with a forward body bias technique because of the small number of transistor stacks. A 0.5 V, 5 bit flash ADC has been developed in 90nm CMOS and exhibits a very low power consumption of 1.2 mW (160 fJ) at 600 MSps [8].

The pipelined ADCs and the sigma-delta ADCs conventionally require small mismatch and large capacitance (>1pF) and a MIM capacitor has been developed to address this requirements. In contrast, SAR ADCs require a large capacitor ratio ($> 2^{N-2}$: N=# of bits) for the capacitors and very small capacitance (<1 fF) is needed. The MOM capacitor is suitable since the capacitance can be adjusted by adjusting the length of the finger. Furthermore, the density of the MOM capacitor increases with technology scaling. On the other hand, the MIM capacitor's density cannot be increased (Fig. 14). The mismatch of the MOM capacitor is larger; however it can be corrected by using small capacitance with digital calibration circuits. The comparator noise should be suppressed for SAR ADC to increase the SNR. A conventional latch circuit generates large noise and this limits the SNR. Thus, we introduced a dynamic amplifier followed by a CMOS amplifier to reduce the thermal noise [6]. As a result, the noise voltage and the noise power become 1/3 and 1/9, respectively (Fig. 15). The input referred noise voltage is,

$$\overline{v_{n\_i}^2} = 2\gamma \frac{kT}{C_L}\frac{V_{eff}}{V_{DD}} \qquad (6)$$

where gamma is the noise factor, V_{DD} is the supply voltage [9].

A larger load capacitance is required to suppress the noise and the lower V_{DD} increases the noise.

A high gain OpAmp (>80 dB), which is required for the pipelined ADC, is not promising with the technology scaling. Therefore, the interpolated pipeline ADC (Fig. 16), which does not require any high gain OpAmps has been proposed [10], [11]. An accurate voltage pair can be composed by the interpolation method from the amplified signals by a pair of low gain (~4x) amplifiers. No accurate absolute gain is required; only a small relative gain mismatch is required to satisfy the linearity of the ADC. The small relative gain mismatch is not so difficult to obtain in IC technology and can be suppressed by a digital error correction.

The sigma-delta ADCs require medium gain (>40 dB) OpAmps to form the integrators. The situation is not so serious compared with the pipelined ADCs; however, it is becoming more challenging due to supply voltage lowering. A VCO (Voltage Controlled Oscillator) exhibits a perfect 1st order integrator, thus the sigma-delta ADCs using VCOs have been developed [12].

References

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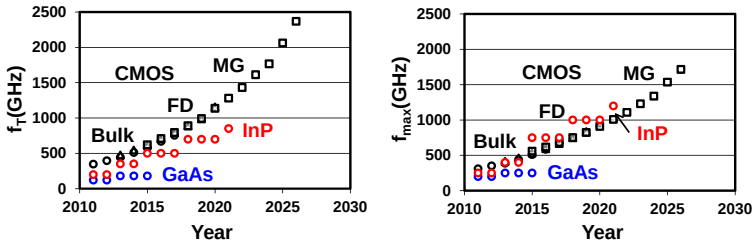

Fig. 1. Expectations of f_T and f_{max}.

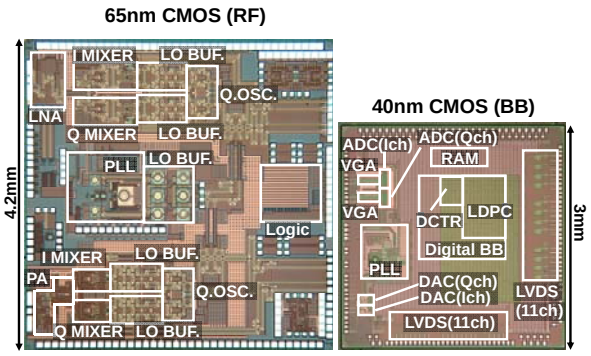

Fig. 2. 60 GHz CMOS transceiver LSIs.
RF LSI (Left) and mixed signal baseband LSI (Right).

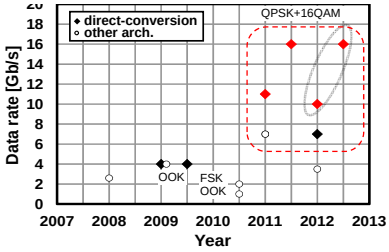

Fig. 3. Data rate in 60 GHz transceivers.

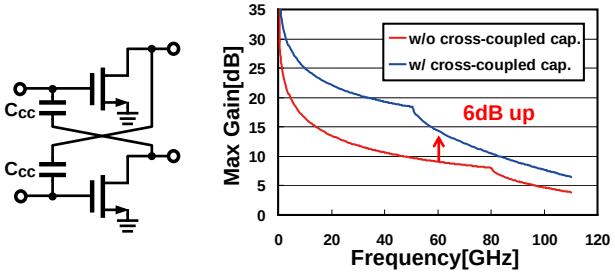

Fig. 4. Negative capacitance and the maximum gain.

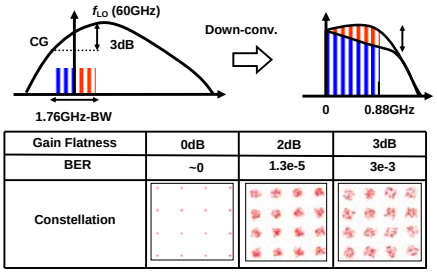

Fig. 5. Gain flatness and the constellation for the 16 QAM.

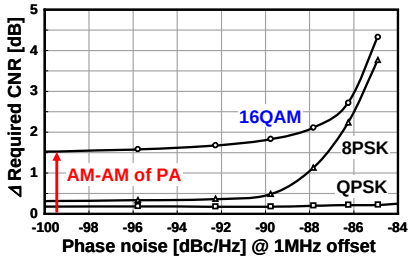

Fig. 6. Requirements for the phase noise.

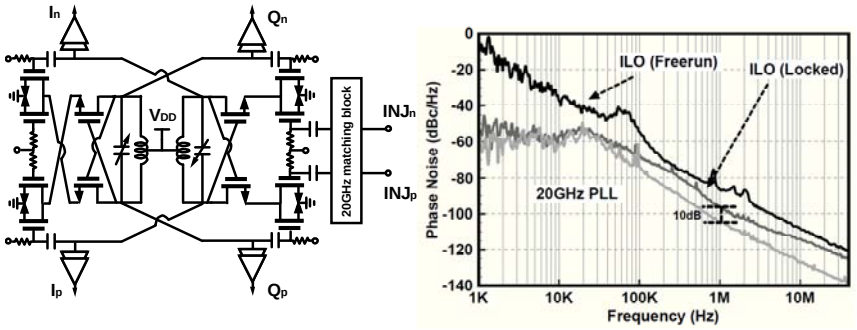

Fig. 7. Injection locked 60 GHz I/Q VCO and phase noise.

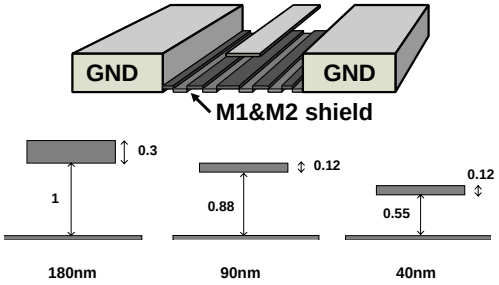

Fig. 8. Transmission line and interconnection structure. (Normalized by the 180 nm technology)

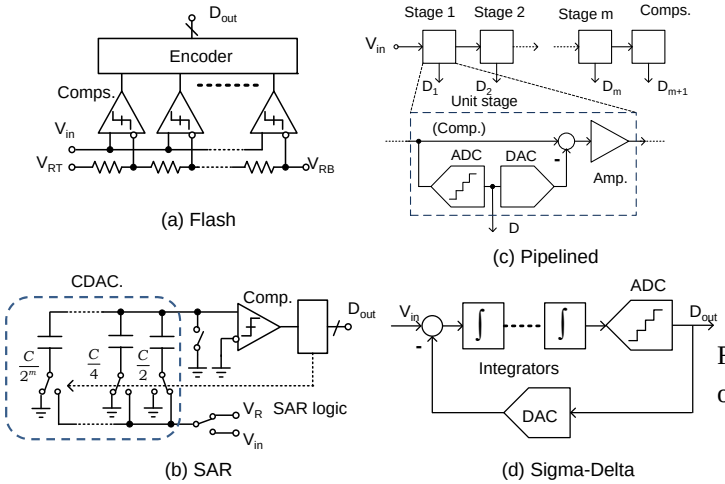

Fig. 9. Major ADC architectures.

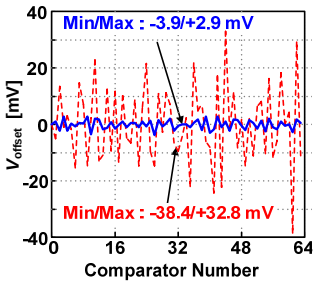

Fig. 12. Native and compensated offset voltages in comparators

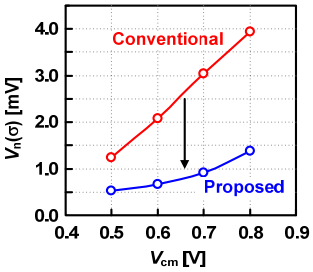

Fig. 15. Noise reduction.

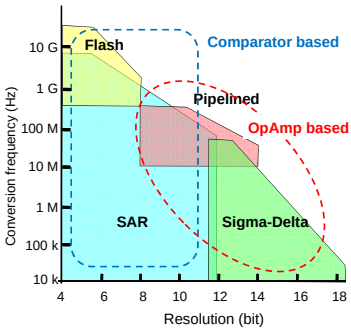

Fig. 10. Performance and the ADC architectures.

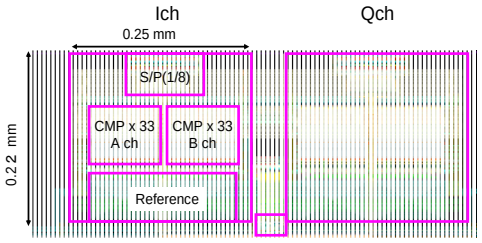

Fig. 13. 5 bit, 2.3 GSps, 12mW, flash ADC

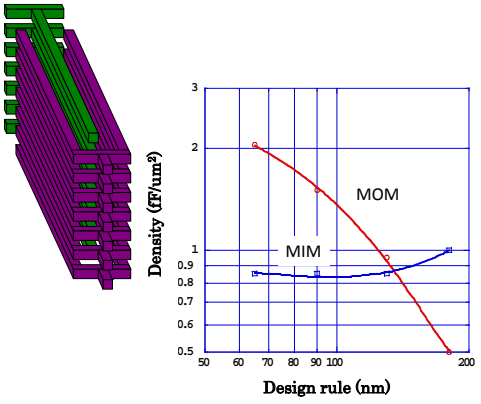

Fig. 14. MOM capacitance and capacitance density.

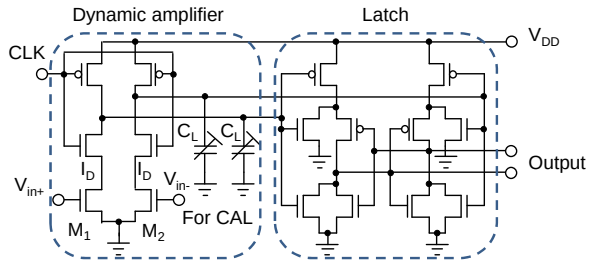

Fig. 11. Dynamic comparator using dynamic amplifier with offset voltage compensation.

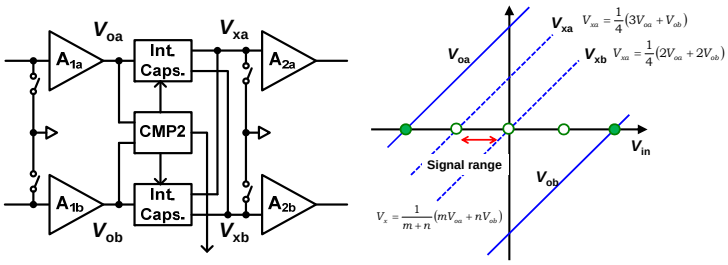

Fig. 16. Interpolated pipeline ADC and voltage diagram.