A 58.1-to-65.0GHz Frequency Synthesizer with Background Calibration for Millimeter-wave TDD Transceivers

Wei Deng, Teerachot Siriburanon, Ahmed Musa, Kenichi Okada, and Akira Matsuzawa
Department of Physical Electronics, Tokyo Institute of Technology
2-12-1-S3-27, Ookayama, Meguro-ku, Tokyo 152-8552, Japan
E-mail: deng@ssc.pe.titech.ac.jp

Abstract— This paper presents a 58.1-to-65.0GHz frequency synthesizer for millimeter-wave TDD transceivers. The proposed synthesizer is capable of supporting all 60GHz channels including channel-bonding defined by IEEE 802.15.3c, wirelessHD, IEEE 802.11ad, and ECMA-387. A background calibration scheme is proposed to automatically correct frequency drift caused by environmental variations. This synthesizer is implemented in a 65nm CMOS process.

I. Introduction

The unlicensed bandwidth between 57 and 66 GHz is released for multi-Gb/s and broadband communications. Current standards governing wireless communication at 60GHz are IEEE 802.15.3c, wirelessHD, IEEE 802.11ad, and ECMA-387. These standards define 4 bands centered at 58.32GHz/60.48GHz/62.64GHz/64.8GHz, and ECMA-387 additionally defines channel-bonding bands centered at 59.4GHz/61.56GHz/63.72GHz for higher data rates and more efficient constellations. In order to compliant with these standards, mm-wave frequency synthesizers that can generate each of these carrier frequencies are required. Moreover, mm-wave frequency synthesizers with quadrature output for direct-conversion architecture, and TDD-supporting capability for more efficient spectrum/lower cost, become increasingly critical and challenging.

Recently, a few PLLs are designed for 60-GHz wireless communication system. Authors in [1] propose a 60GHz PLL using a QVCO oscillating at the fundamental frequency. Later, a PLL with push-push VCO followed by a hybrid coupler [2] is published. In [3], a PLL with a sub-harmonic VCO which is used to inject a super-harmonics quadrature Injection Locked Oscillator (ILO) [4] is reported. Among these publications, PLL using super-harmonics quadrature ILO is preferred due to the best phase noise performance at 60GHz. However, due to inaccurate active/passive device modeling at mm-wave frequency band, it is difficult to guarantee the proper operation of the 60GHz ILO, especially including process-voltage-temperature (PVT) variations. A conventional foreground calibration technique [1][5], which is operated only at start-up, cannot track ILO frequency drift as temperature varies, thus, a background method, which would automatically correct frequency drift by frequency feedback, is needed inevitably. For TDD transceivers, one possible background calibration method is to calibrate the ILO for RX (TX) during TX (RX) time slots. According to IEEE 802.11ad, Short Inter-Frame Spaces (SIFS) length is 3μs, and ACK length including preamble is 1.2μs, then the maximum available duration for ILO calibration is limited to 7.2μs. Conventional mm-wave calibration method [1][5], as shown in Fig. 1 (a), is infeasible for calibrating ILO, since two calibration procedures (Step1: calibrate ILFD, step2: calibrate ILO) are required to carry out sequentially, which is time-consuming.

In this paper, a 60GHz frequency synthesizer with background calibration is proposed for mm-wave TDD transceivers. Only one calibration procedure is required, which significantly reduces calibration time cost. The proposed frequency synthesizer operates for a wide frequency range from 58.1 to 65.0 GHz, which supports all 60GHz channels including channel-bonding defined by IEEE 802.15.3c, wirelessHD, IEEE 802.11ad, and ECMA-387. This paper is organized as

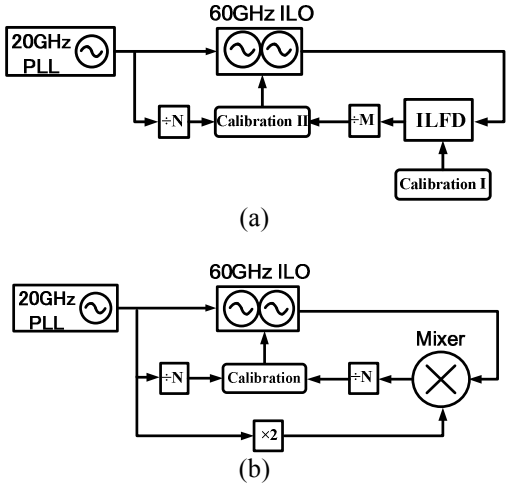

Fig.1.Conceptual diagram of 60GHz frequency synthesizer with (a) conventional calibration method, and (b) proposed calibration method.

follows: In section II, the proposed architecture is discussed. The following section describes the circuit implements in details. Section IV demonstrates experimental results of proposed 60GHz frequency synthesizer. Finally, conclusion is summarized in section V.

II. Proposed Architecture

The basic approach adopted in this paper is using a 20GHz PLL to inject a 60GHz ILO, which is operated as a frequency tripler. As mentioned previously, the correct operation of the 60GHz ILO cannot be ensured due to inaccurate active/passive device modeling and PVT variations. Therefore, in order to guarantee that the 60GHz ILO can acquire the injection locking to the 20GHz PLL properly, it is necessary to automatically calibrate the free-running frequency of 60GHz ILO to 3 times than the output frequency of the 20GHz PLL

During calibration, comparison between the derivative signal of 60GHz ILO free-running frequency and 20GHz PLL output frequency is involved. Fig. 1 (a) and (b) shows a conceptual diagram of the 60GHz frequency synthesizer with digital calibration using Injection Locked Frequency Divider (ILFD), and a mixer for frequency reduction, respectively. Each one has its merits in terms of power dissipation, chip area, PVT-tolerance, and calibration time. For TDD systems, transmitter (TX) and receiver (RX) operate in different time slots. Thus, the calibration of 60GHz ILO for TX can be performed during RX time slots, and the calibration of 60GHz ILO for RX can be performed during TX time slots. However, the time duration is limited to 7.2 μs only for each TX and RX slot according to IEEE 802.11ad, imposing a strict requirement for the calibration time of the 60GHz ILO. In Fig. 1(a), the ILFD for frequency reduction would be calibrated first to ensure its functionality, before the performing of 60GHz ILO calibration. Then the total calibration time is significantly increased, which demonstrates the infeasibility of calibration using ILFD for frequency down-conversion.

In order to reduce the calibration time, frequency down-conversion using mixer is employed as shown in Fig.1 (b). The process of calibration is carried out when the 20GHz PLL is locked. At the initial state or during TX time slots, the ILO for RX outputs its free-running frequency, and the output of ILO for RX is down-converted to a frequency around 20 GHz by a mixer, through doubling of the 20GHz PLL injection signal. After two separate divider chains, the frequency coming from the output of mixer and the 20GHz PLL are compared using digital calibration circuits. The output of digital calibration circuit directly controls the digital code for a digital-to-analog converter, giving rise to adjust the ILO free running frequency. After several reference cycles, the 60GHz ILO free-running frequency is closed to the 3 times of the 20GHz PLL output. Considering the calibration of ILO for RX (TX) is performed at TX (RX) time slots, the calibration method can run as a background calibration to monitor the 60GHz ILO frequency over temperature drift.

III. Circuit Descriptions

The proposed 60GHz frequency synthesizer mainly consists of a 20GHz PLL, a 60GHz Quadrature ILO, a frequency down-converting circuit, and a digital calibration circuit. The block diagram of proposed 60GHz synthesizer is depicted in Fig. 2.

A. 20GHz PLL

The 20GHz PLL consists of a phase-frequency detector (PFD), a current-steering charge pump, a 2nd-order on-chip low pass filter, an LC-VCO with a tuning range of 17.9-to-21.7 GHz, followed by a divide-by-2 CML divider, an divide-by-3 E-TSPC divider, a digital divide-by-5 divider, and a digital multi-modulus divider. The whole divide ratio can be controlled from 1620 to 1800 in steps of 30. This divide ratio combing with a 12 MHz frequency resulting from a halved off-chip 24MHz reference enables synthesis of the required tones.

B. 60GHz ILO [8]

The circuit schematic of 60GHz ILO is shown in Fig. 3. A quadrature 60GHz LO signal can be obtained due to a quadrature I/Q configuration. The free-running frequency can be

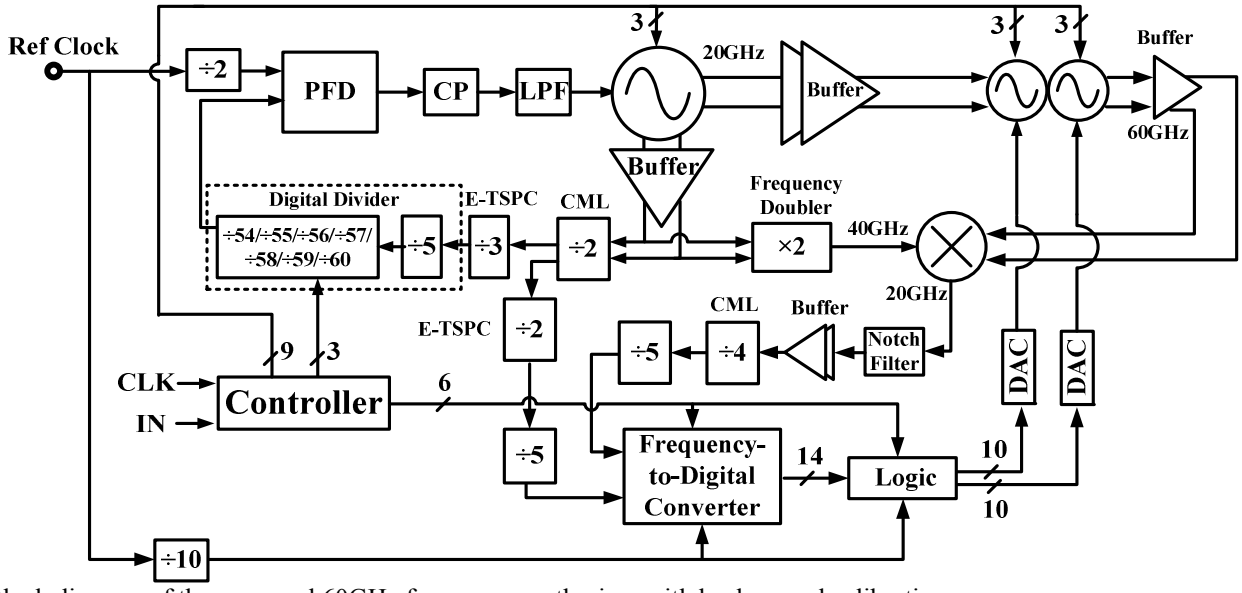

Fig.2. Block diagram of the proposed 60GHz frequency synthesizer with background calibration.

adjusted by a switched capacitor bank for coarse tuning, and a varactor which is controlled by the calibration circuit for fine tuning. The 20GHz PLL signal is injected through tail transistor of I oscillator.

C. Down-converting Circuit

The down-converting circuit is composed of a frequency doubler, a mixer, and two notch filters as shown in Fig. 4. The frequency doubler is utilized for generating a second harmonic of the input signal from the 20GHz PLL. The mixer is designed using a single-balanced topology which mixes the single-ended RF output from the frequency doubler at frequency around 40GHz, with differential LO output signal from ILO at frequency around 60GHz. Output signal of the mixer carries 20GHz output signal and undesirable signals caused by strong LO input power. Therefore, notch filters are implemented to suppress LO feedthrough from the input stage of the mixer at frequency around 60GHz. Finally, output signal goes through 20GHz buffers and divider chain before performing digital calibration. Additionally, in order to save chip area, all inductors employed in this circuit are custom-designed, which composed of three 15μm × 15μm stacked-spiral inductors used for shunt peaking and impedance matching, and two 70μm × 80μm inductors utilized for notch-filtering, as shown in Fig. 4.

D. Digital calibration circuit

The digital calibration circuit consists of a frequency-to-digital converter, and digital logics. In order to increase the frequency resolution, digital calibration circuits are triggered at 1/10 of the reference clock. Derivative frequency signals coming from the 60GHz ILO and 20GHz PLL are measured using digital counters, respectively. Outputs of the digital counters, in the form of binary numbers, are compared in the following logic circuit during each reference cycle for digital circuits. The output of logic circuit directly controls the code for DAC, giving rise to adjust the ILO free-running frequency. If the derivative frequency coming from the 60GHz ILO is greater (less) than that coming from the 20GHz PLL, the output code of digital logic circuit is decremented (incremented) to speed down (up) the 60GHz ILO free-running frequency, as illustrated in Fig.5. The calibration system allows intermittent operation to reduce extra power consumption for calibration.

IV. Experimental Results

The proposed 60GHz frequency synthesizer is implemented in a standard 65nm CMOS process. The microphotograph of the fabricated synthesizer is shown in Fig. 6. The total chip area is 1.9mm × 2 mm. PLL spectrum is measured with an Agilent E4448A PSA spectrum analyzer and a 50-to-75 GHz external mixer. The phase noise is evaluated using an Agilent E5052B SSA signal source analyzer and a 50-to-75 GHz external mixer.

When the frequency of input reference clock is 24MHz, the synthesizer can generate all 60GHz channel bands: 58.32GHz, 59.4GHz, 60.48GHz, 61.56GHz, 62.64GHz, 63.72GHz, and 64.8GHz, which are defined by IEEE 802.15.3c, wirelessHD, IEEE 802.11ad, and ECMA-387. The frequency synthesizer consumes 72mW from a 1.2V power supply. If the intermittent operation is disabled, the calibration circuits including down-converting circuits and digital circuits consume 65mW additionally.

The measured output spectrum of the 20GHz synthesizer is shown in Fig.7. The reference spur level of the 20GHz PLL varies from -54 to -70dBc. The phase noise of the 60GHz synthesizer is less than -114 dBc/Hz @ 10MHz offset across the

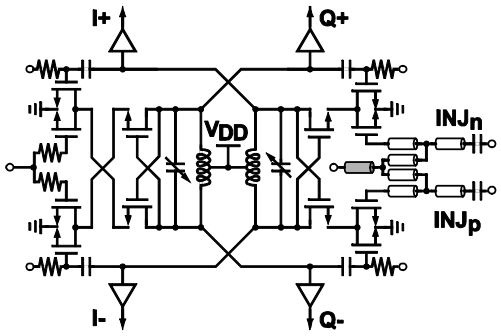

Fig.3.Circuit schematic of the quadrature ILO.

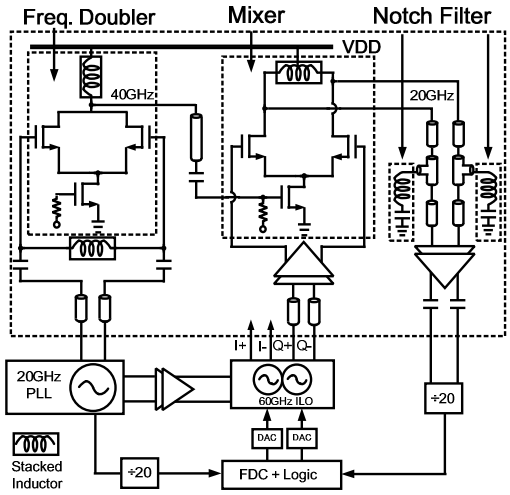

Fig.4. Schematic of down-converting circuits, along with other building blocks.

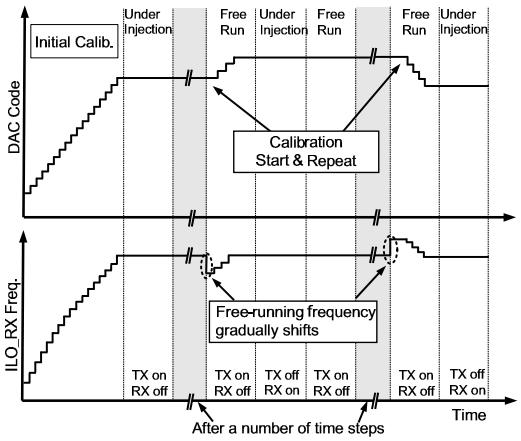

Fig.5. DAC code and output frequency of ILO for RX against time.

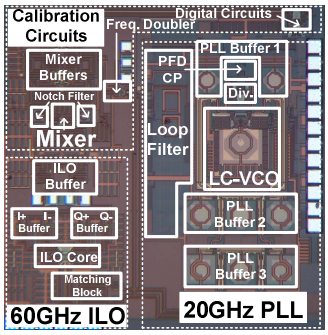

Fig.6. Chip micrograph.

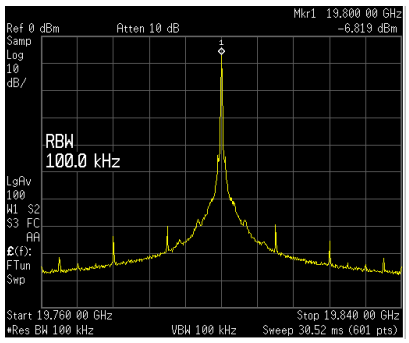

Fig.7. Measure spectrum@19.8GHz.

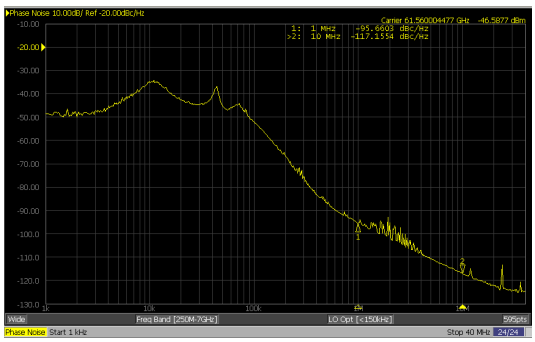

Fig.8. Measured phase noise @ 61.56GHz.

entire band. The typical measured phase noise is -117 dBc/Hz @10MHz offset, from a carrier frequency of 61.56 GHz, as shown in Fig. 8. It is noted that the output power indicated in Fig. 8 does not account for losses from cables and an external 50-to-75 GHz down-conversion mixer. The calibrated output power is -8dBm.

Table I compares the present 60GHz frequency synthesizer with the state-of-art publications [1-3][6][7]. To the best knowledge of authors', it is the first 60GHz frequency synthesizer with background calibration for TDD transceivers.

V. Conclusion

A 60GHz frequency synthesizer with background calibration which can support IEEE 802.15.3c, wirelessHD, IEEE 802.11ad, and ECMA-387 TX/RX front end is reported. With carful design, the proposed synthesizer can be suited for millimeter-wave TDD systems.

Acknowledgment

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Table I Performance comparison with other state-of-the-art 60GHz PLLs

	Features	CMOS Tech [nm]	f_{ref} [MHz]	Frequency [GHz]	Phase Noise [dBc/MHz]	Power [mW]	Output type	Background Calibration
[1]	QVCO@60GHz + Foreground Calibration	45	100	57 - 66	-75@1	78	Quad.	No
[2]	Push-push VCO@30GHz + Hybrid Coupler	90	203.2	59.6 - 64	-73@1 -112@10	76	Quad.	-
[3]	Super-harmonic Injection	65	36	58 - 63	-96@1 -113@10	80	Quad.	No
[6]	Diff. VCO @60GHz	90	234	58 - 60.4	-85@1	80	Diff.	No
[7]	Diff. VCO @60GHz	90	60	61 - 63	-80@1 -110@10	78	Diff.	No
This work	Super-harmonic Injection + Background Calibration	65	24	58.1 – 65.0	-96@1 -117@10	72	Quad.	Yes