A 0.5 V, 420 MSps, 7-bit Flash ADC Using All-Digital Time-Domain Delay Interpolation

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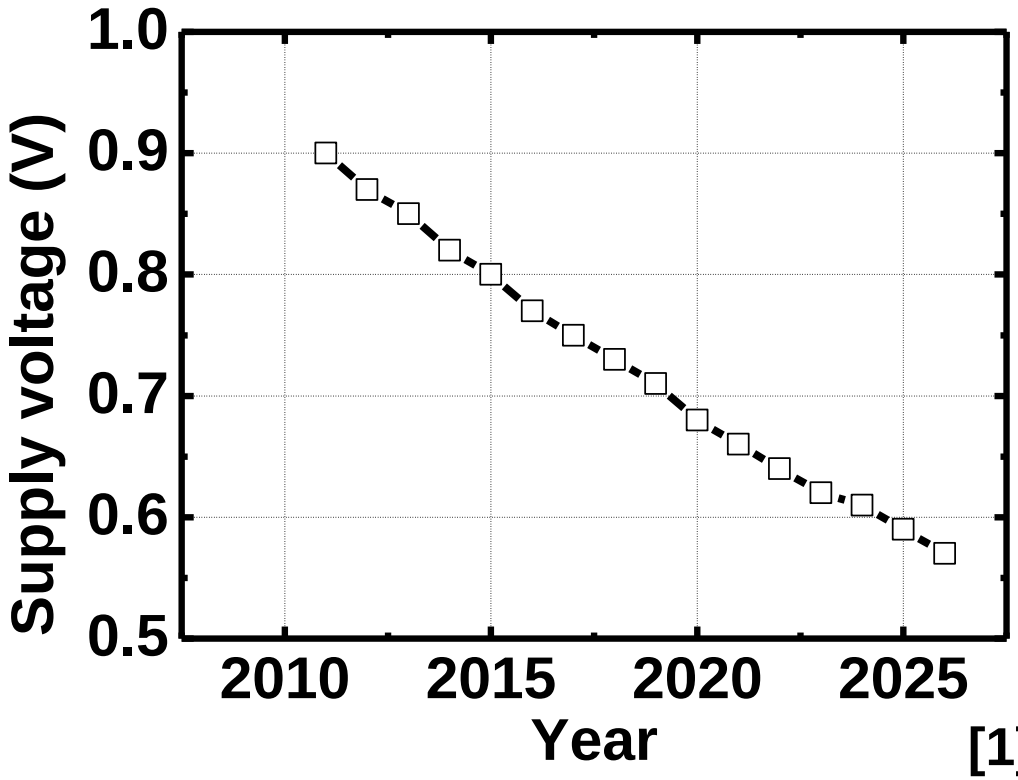
Outline

- **Motivation**
- **Background**
- **Circuit Design**
- **Experimental Results**
- **Conclusion**

Motivation

- **Ultra-low-voltage operation**
  - **Immediate power saving potential**
  - **Explore new circuit techniques for future technology**



[1] ITRS, 2011.

Background

- **Flash ADC's advantages**
  - **Shortest latency**

  →Attractive for systems with feedback loops: clock data recovery (CDR), decision feedback equalizer (DFE)
- **Disadvantages**
  - **With increasing resolution**

  →Exponential increase

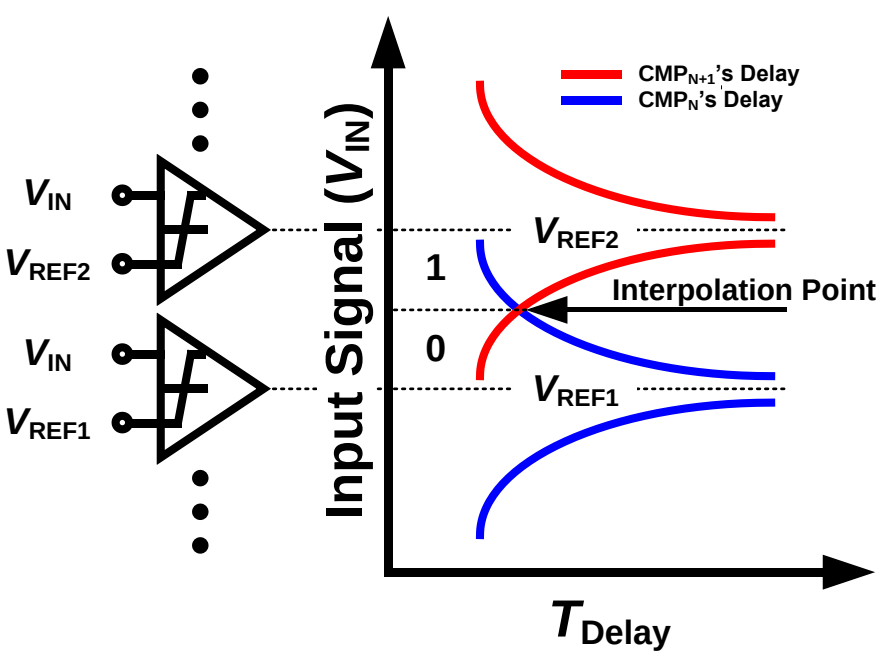
  →Power consumption

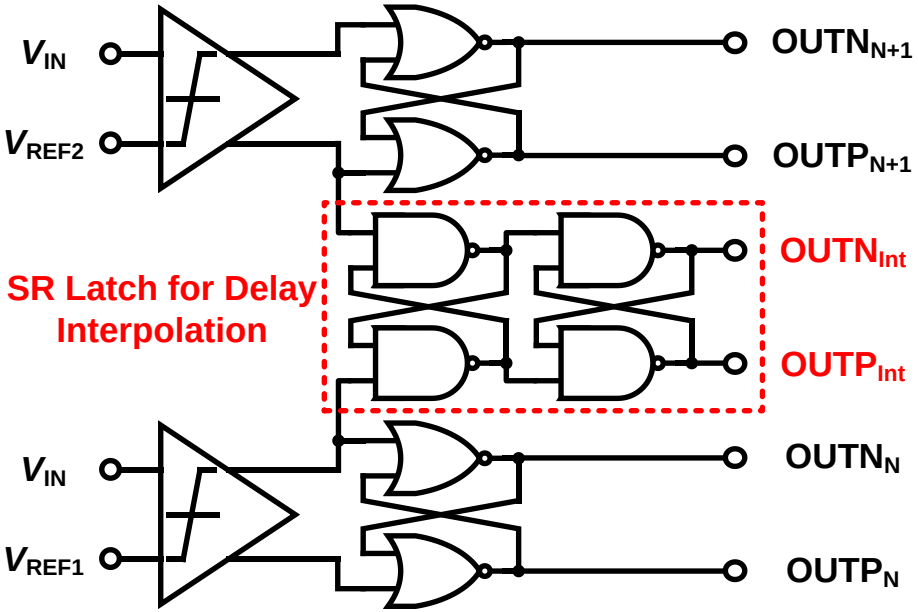
  →Area

  →Input capacitance

Time-Domain Delay Interpolation

- **Time-domain interpolation can enhance the resolution of a flash ADC without the severe trade-offs [2]**

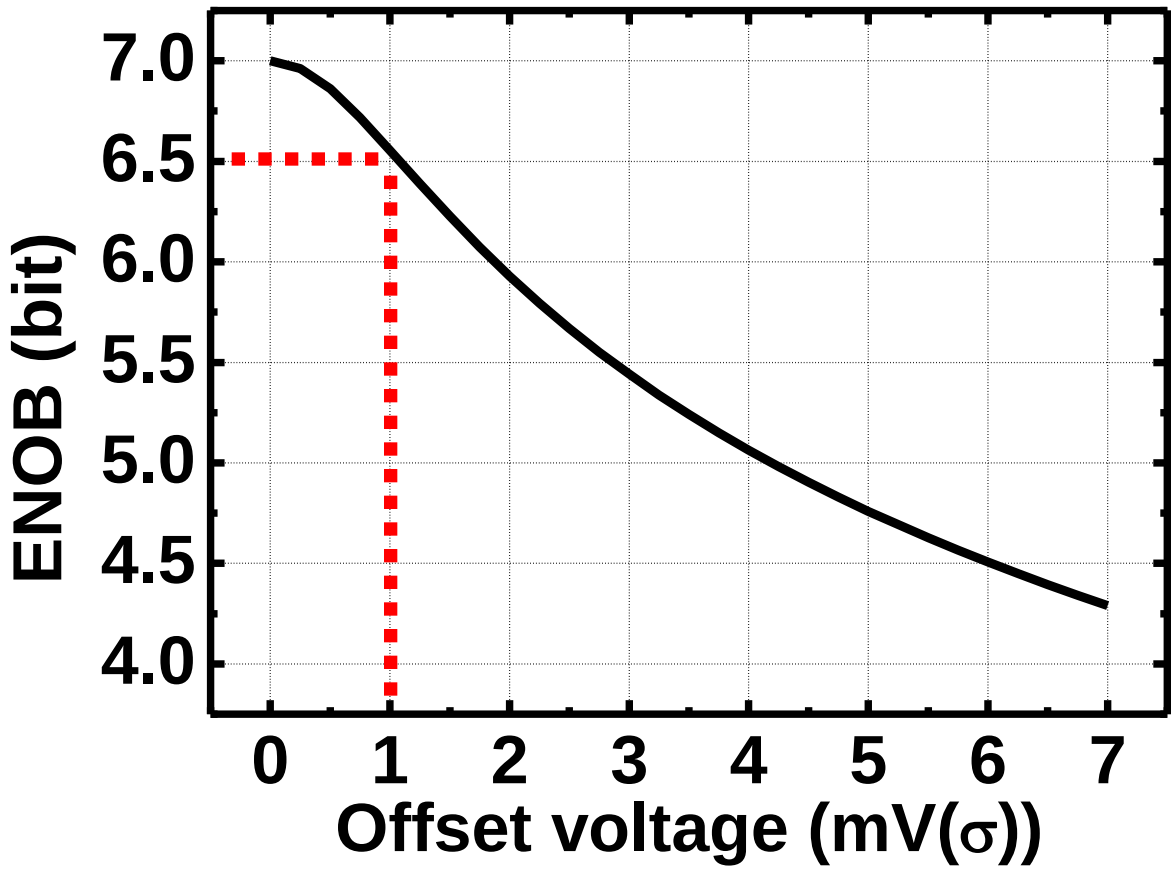




[2] Y. S. Shu, VLSI Circuits 2012.

Offset voltage vs. ENOB

- **To limit the ENOB degradation to less than 0.5 bit → < 1 mV(σ) offset voltage is required**



Mismatch Calibration at ULV

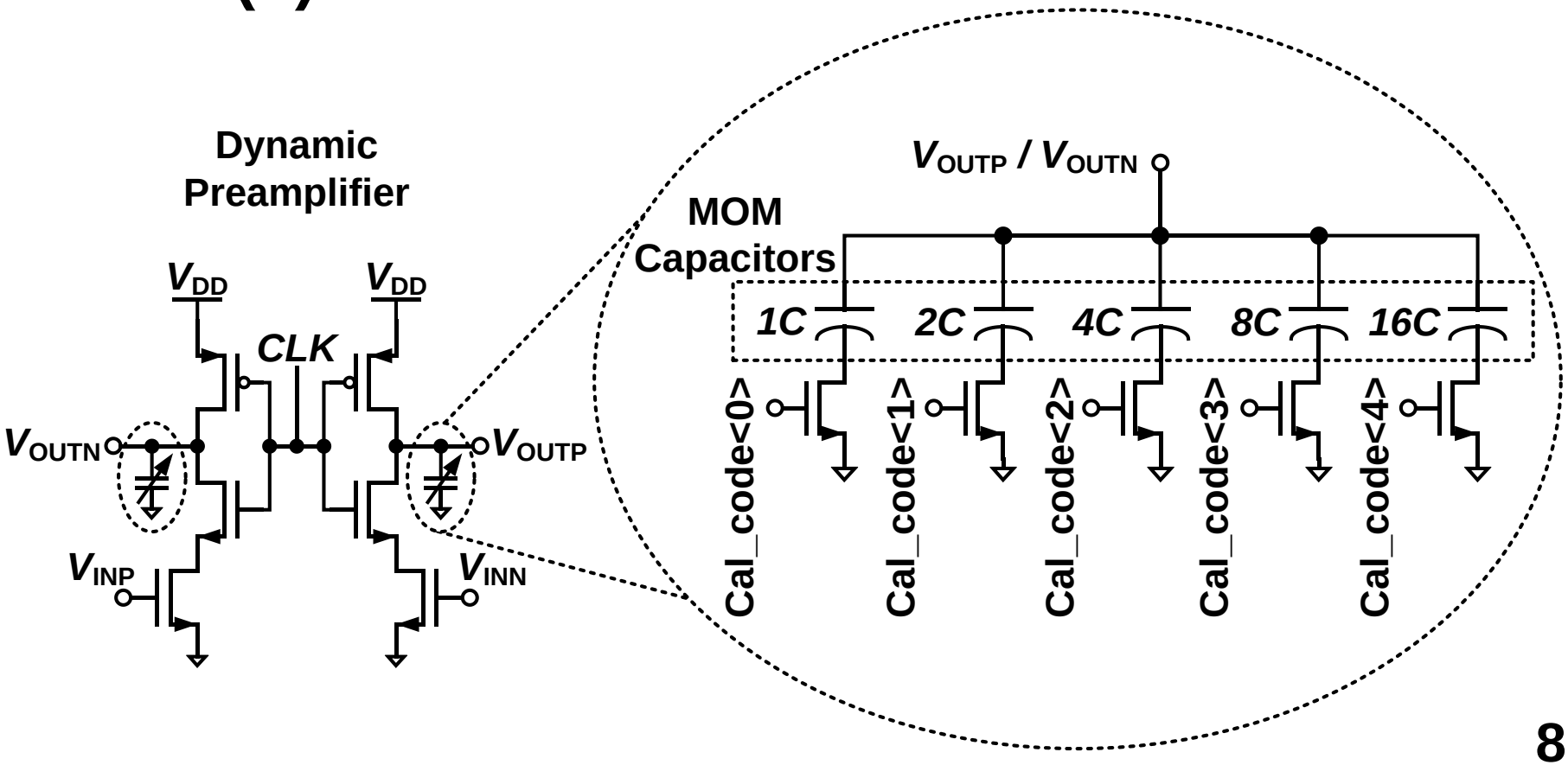
- **Conventional varactor [3] calibration degrades with supply voltage lowering**
- **The mismatch of the comparator can be problematic at the ultra-low supply voltage**

Calibration Methods	None	Current	Varactor	Time	MOM
Offset [mV(σ)]	10.1	1.32	5.79	1.77	0.85
Power @ 500 MHz [mW]	14.5	41.3	21.4	24.5	17
Delay [ps]	365	450	756	556	625

[3] V. Giannini, *et al.*, ISSCC 2008.

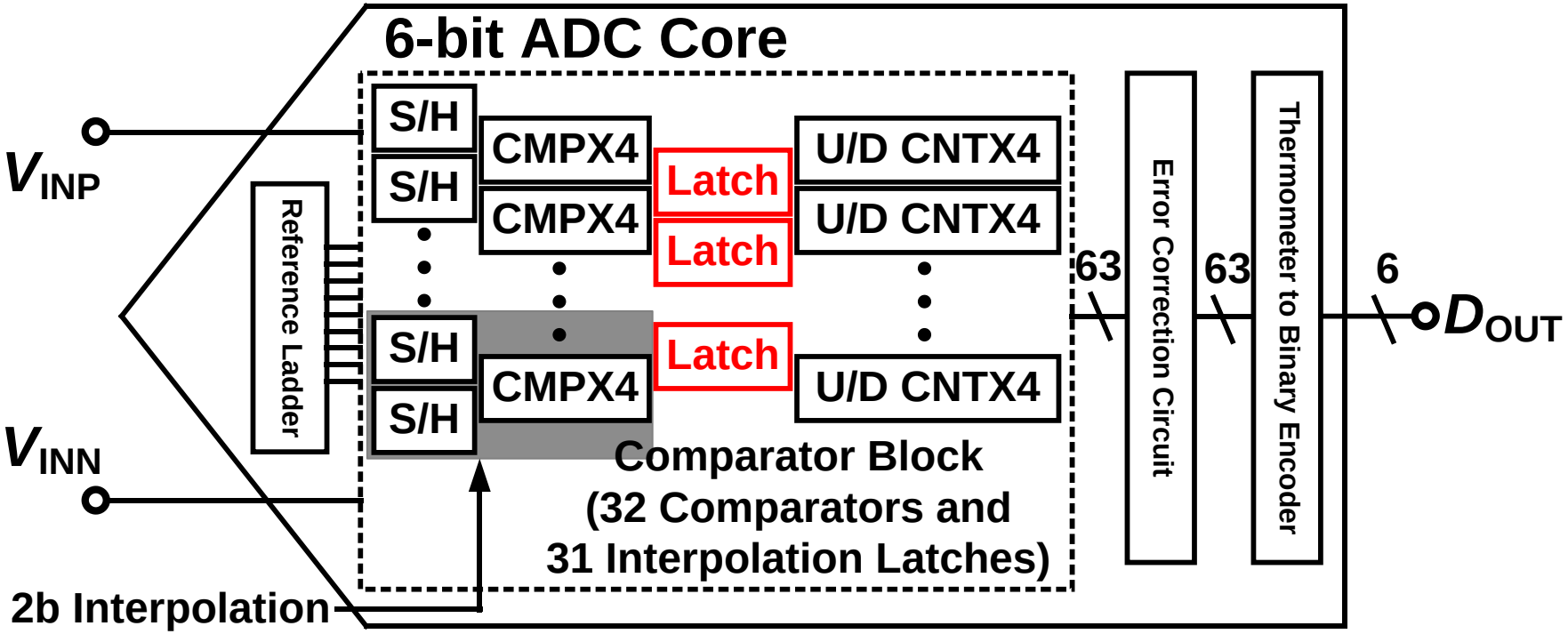
MOM Calibration

- **Using MOM capacitors and switches, the offset voltage can be suppressed to less than 1 mV(σ)**



6-bit ADC Core

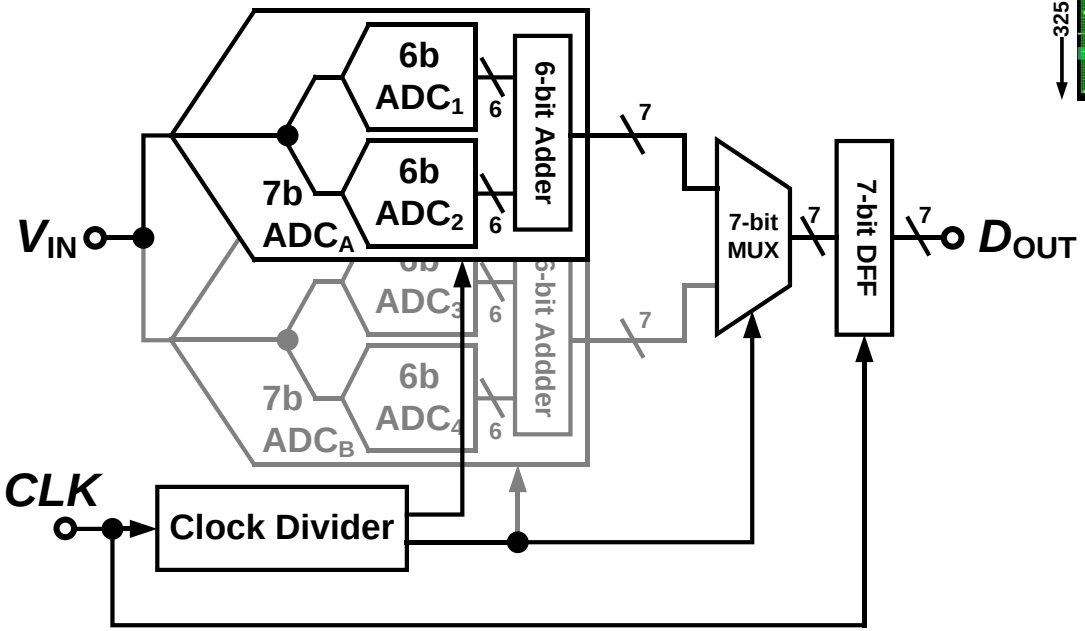
- **6-bit ADC core with delay interpolation using a modified 5-bit core from [4]**

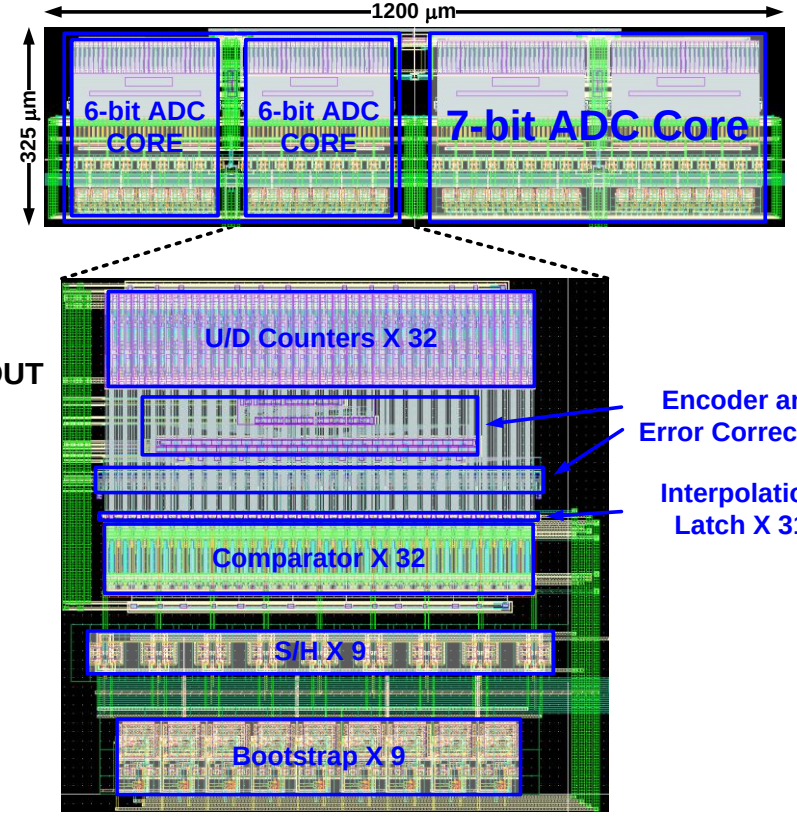


[4] M. Miyahara, A-SSCC 2010.

ADC Structure

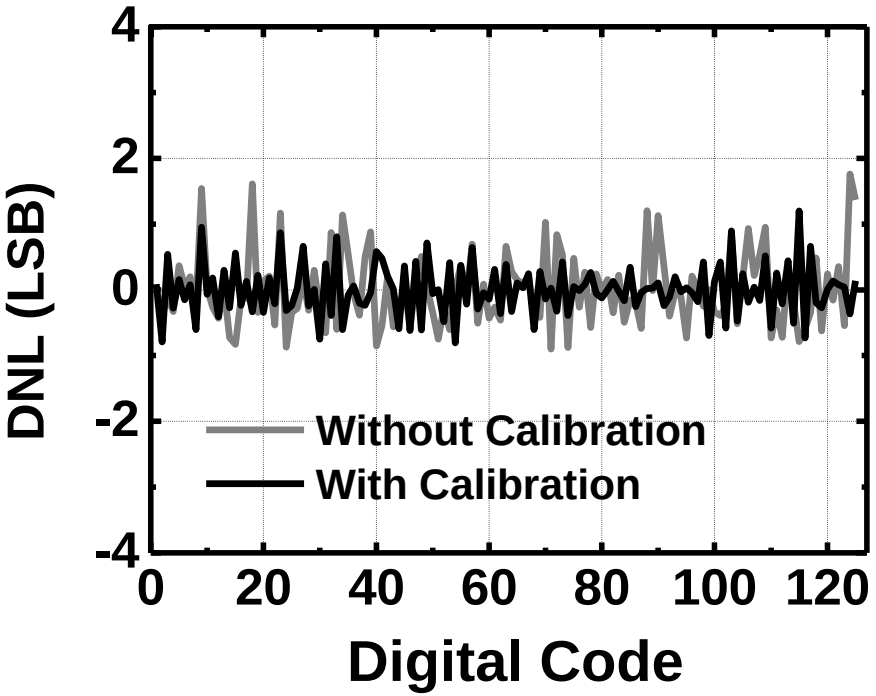
- 7-bit ADC block diagram consists of 4×6-bit cores



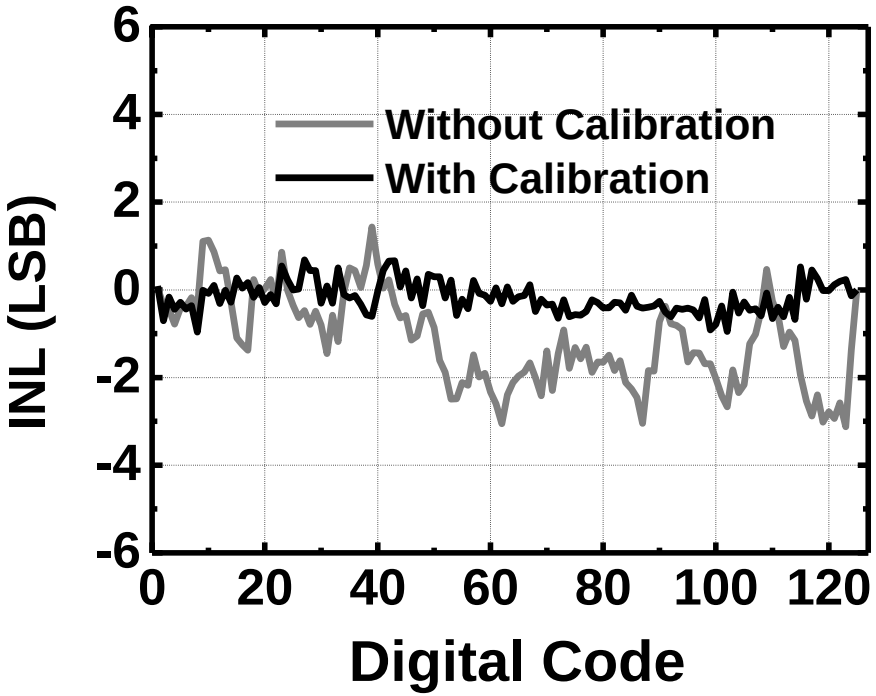


Measured DNL and INL

DNL
±1.6 LSB → ±0.95 LSB



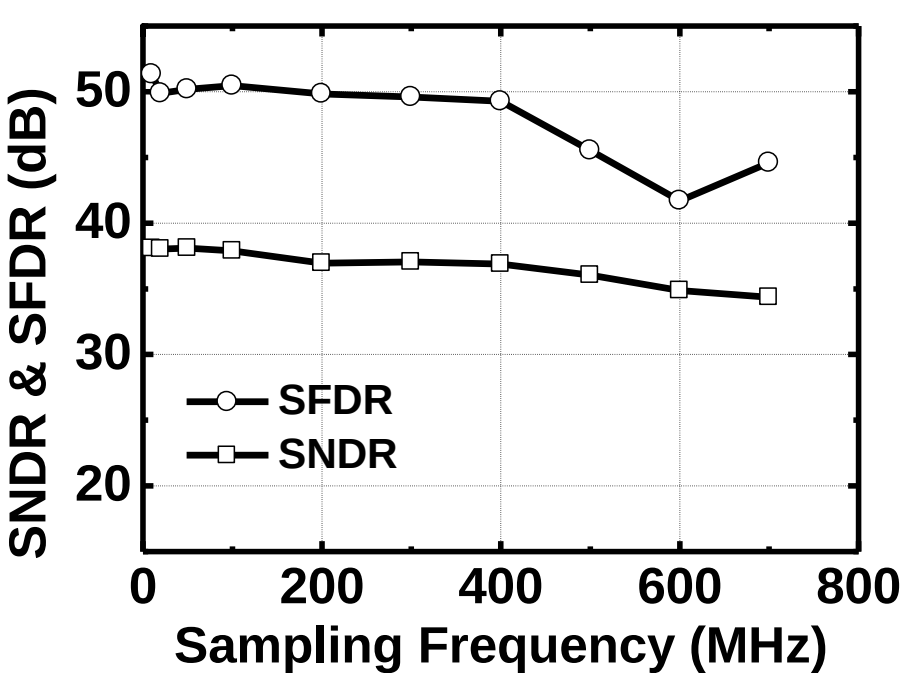
INL
±1.4 LSB → ±0.68 LSB



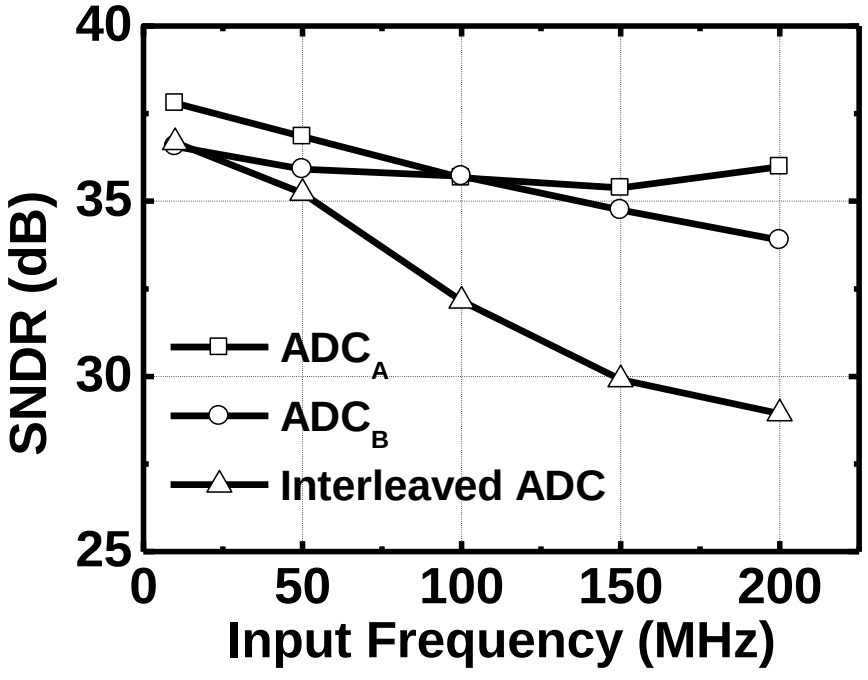
(Operating at 100 MSps with a 0.5 V supply)

Measured SFDR and SNDR

- SFDR and SNDR vs. sampling frequency
- SNDR vs. input frequency



(a)



(b)

Performance Comparison

	[5]	[6]	[7]	This Work	
Architecture	Subrange	Subrange	Pipeline	Flash	
Resolution [bit]	7	7	10	7	
f_s [MSps]	2200 (4 ch)	300 (1 ch)	10 (1 ch)	420 (2 ch)	210 (1 ch)
Process [nm]	65	65	90	90	
Supply [V]	1	1.2	0.5	0.5 (V_{BS} = 0.5)	
SNDR [dB]	36.1	40.5	48.1	35	36
Power [mW]	40	2.3	2.4	4.1	2.1
FoM [fJ/c.-s.]	280	88	940	906	195

[5] I. N. Ku, *et al*., CICC 2011.

[6] U. F. Chio, *et al*., ESSCIRC 2011.

[7] J. Shen, *et al*., JSSC 2008.

Conclusion

- **All-digital time-domain delay interpolation enhances the resolution of a flash ADC without the undesirable trade-offs**
- **MOM calibration is effective for ultra-low-voltage circuits**
- **Ultra-low-voltage proves to be a promising method to reduce power consumption**

Thank you for your interest!

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