TOKYO TECH
Pursuing Excellence

Current status and future prospect of analog and RF VLSI design

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Outline

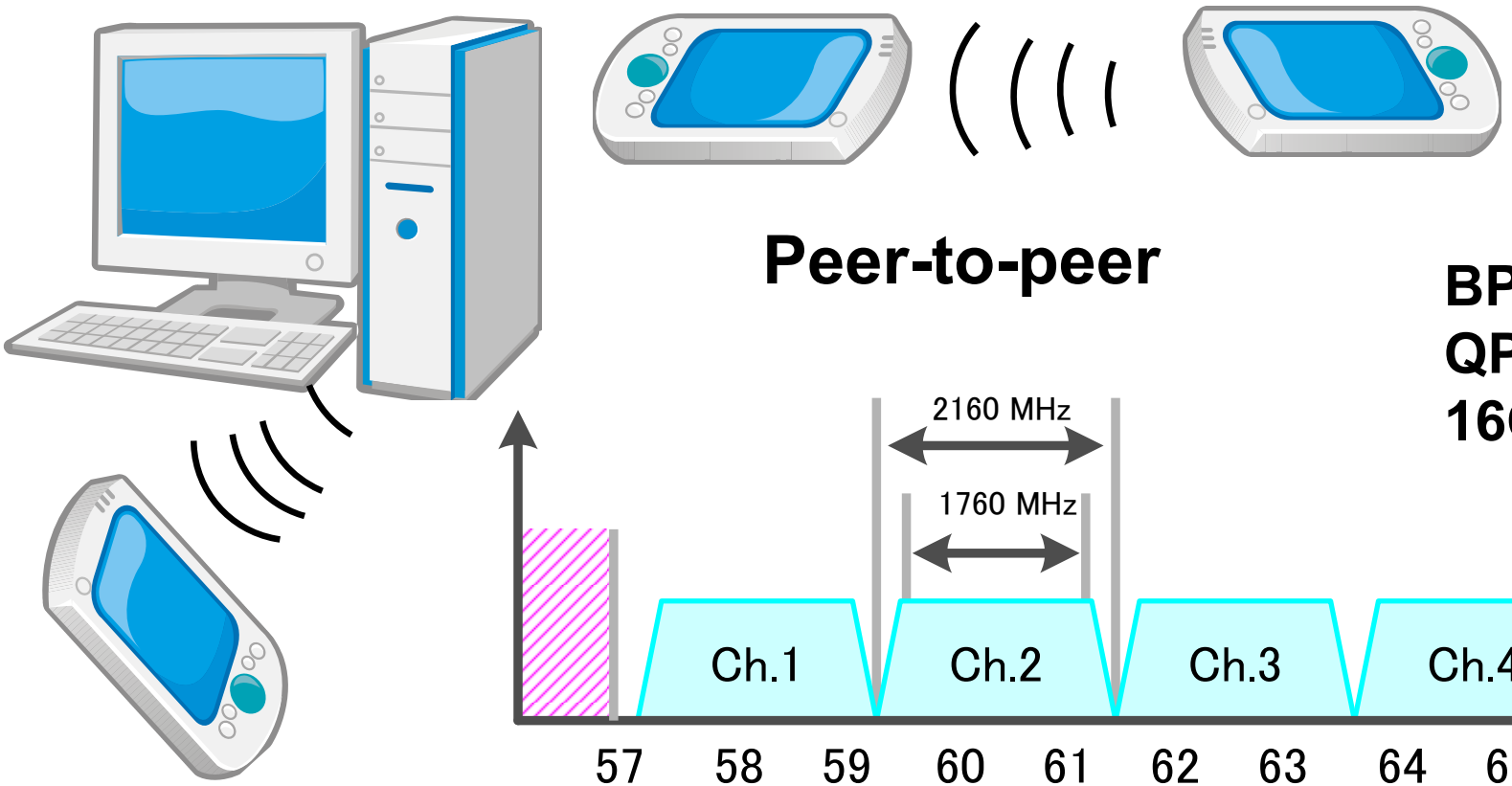
- **RF IC design**
  - 60GHz CMOS transceiver
  - Essence of millimeter wave IC design
- **ADC design**
  - Flash ADC with dynamic comparator
  - SAR ADC with dynamic comparator
  - Interpolated pipeline ADC
- **Discussion and summary**

RF IC design

60GHz CMOS transceiver

Usage model

Giga bit ultra-fast data transfer systems around 60GHz.
4 ch. 1.8GHz BW provides 3.5—7.0 Gbps data transfer.
Low power and small size are required



Peer-to-peer

BPSK: 1.7 Gbps
QPSK: 3.5 Gbps
16QAM: 7 Gbps

Kiosk download

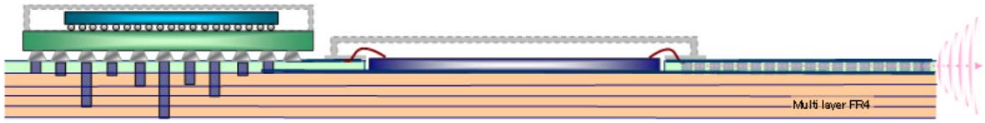
BW: 1.8GHz, 4 channels

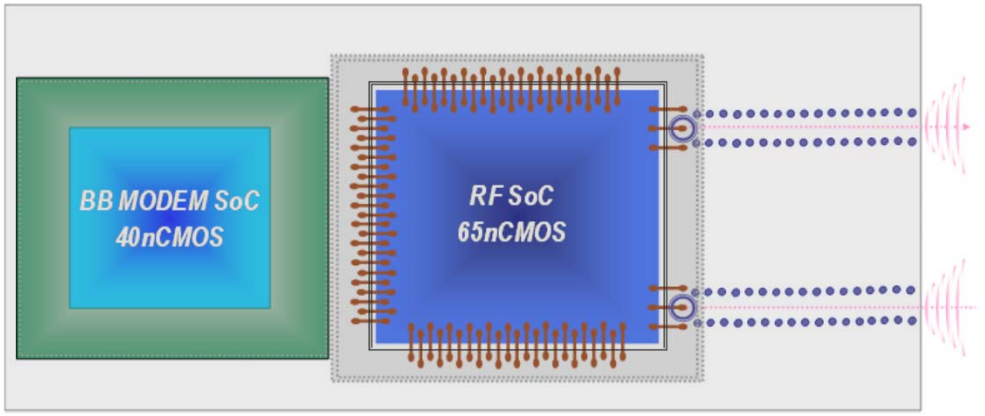
IEEE 802.15.3c

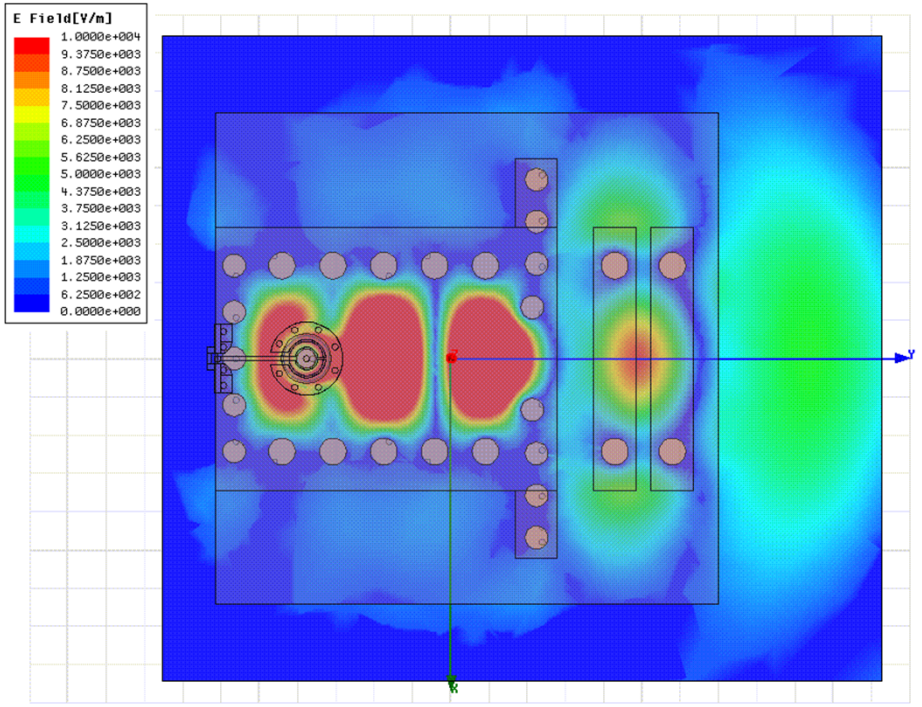
Equipment image

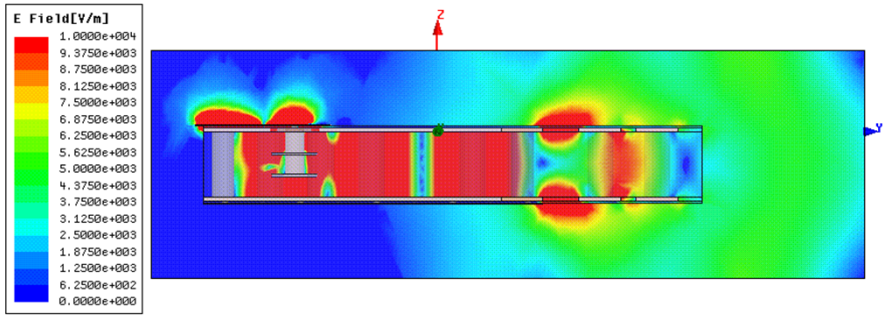
Two chips solution on one PCB with antenna

Low cost system



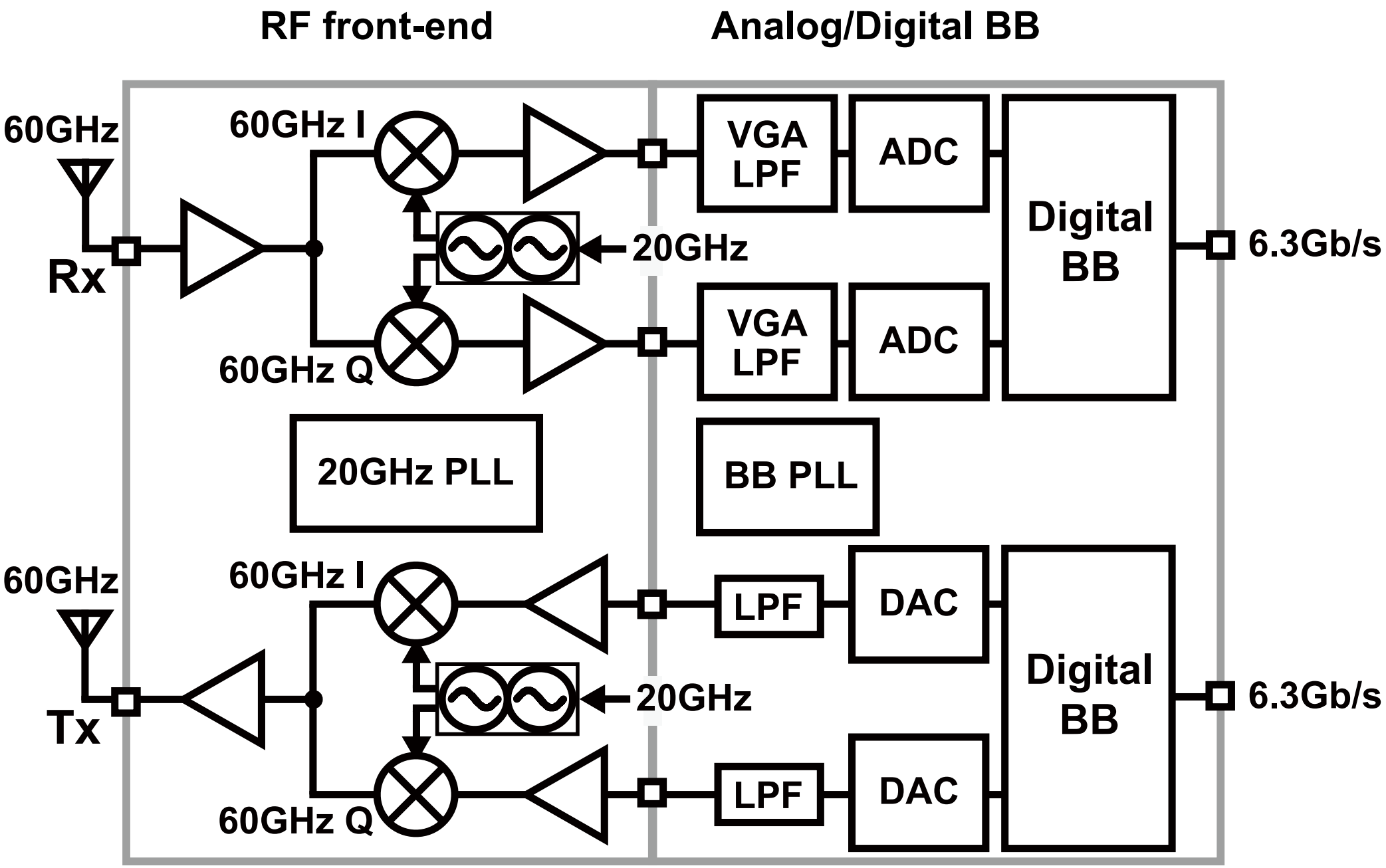






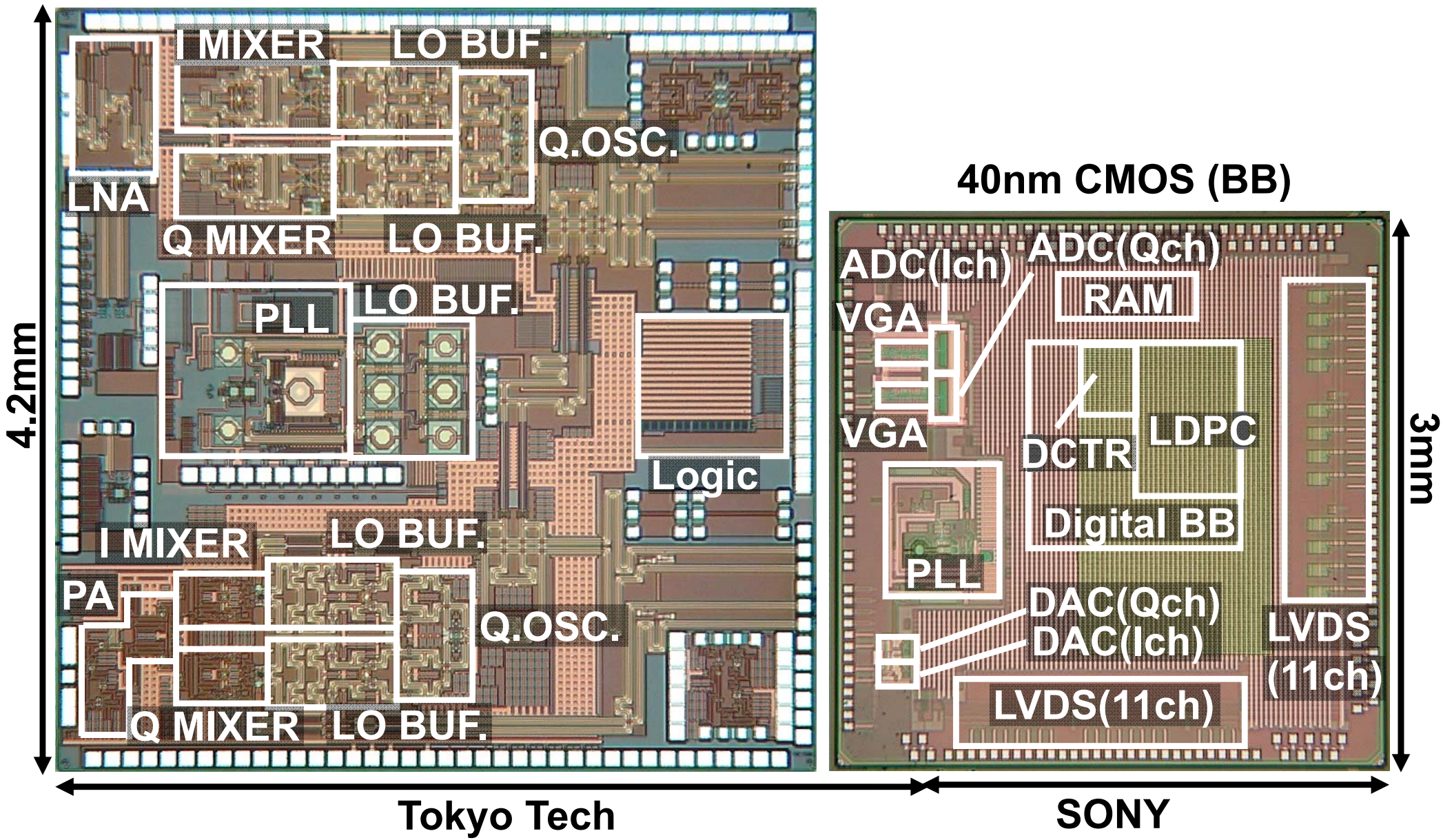
Gain: 5.6 dBi

60GHz Transceiver: Block Diagram



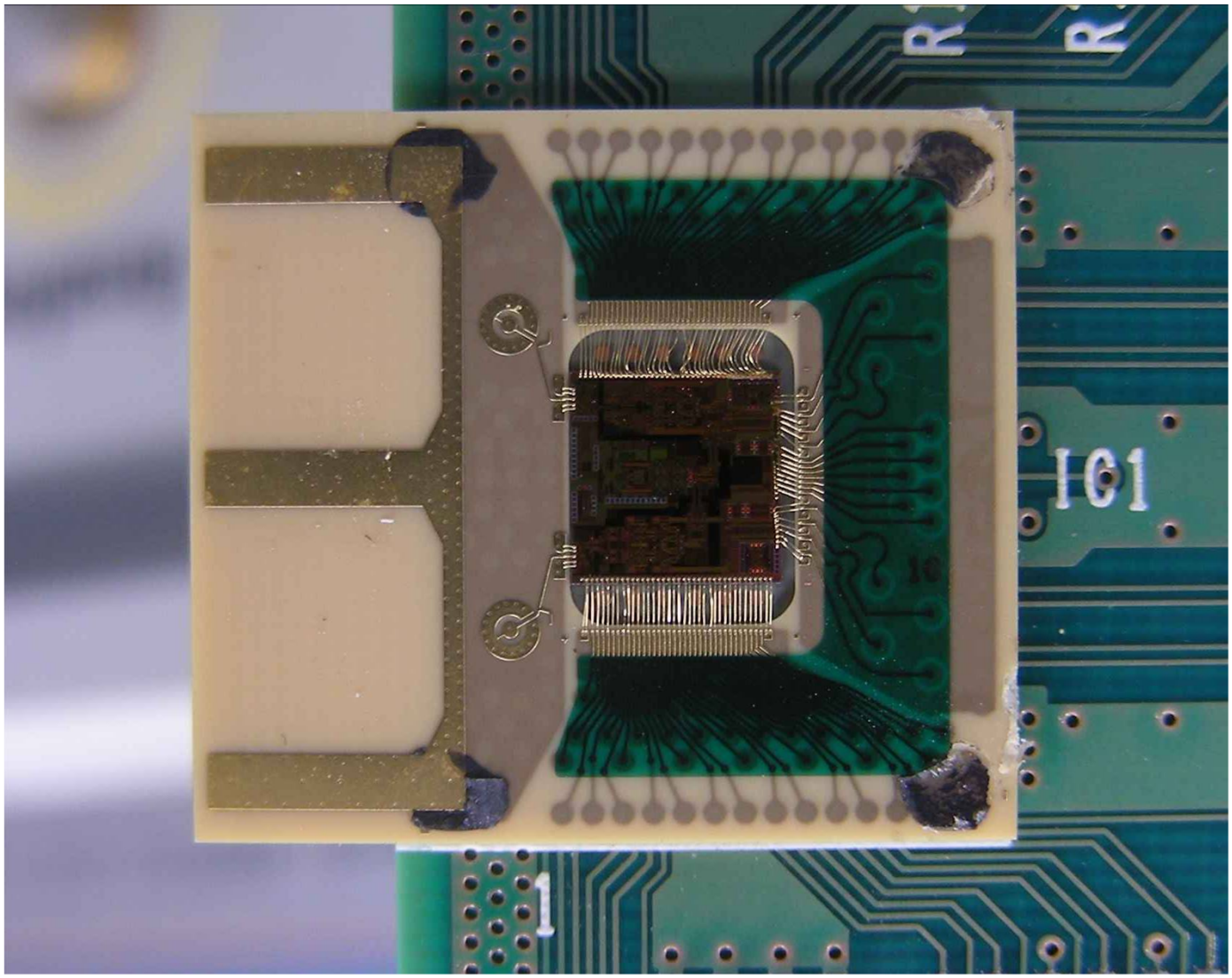
Die Photo

K. Okada and A. Matsuzawa, et al., ISSCC 2012

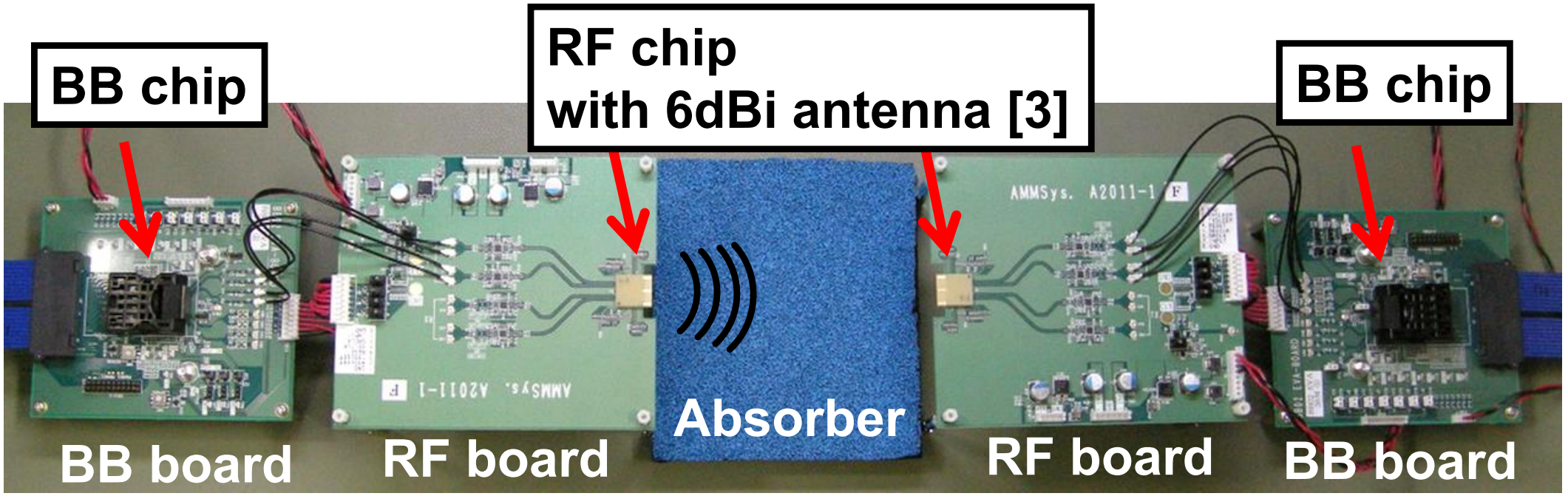


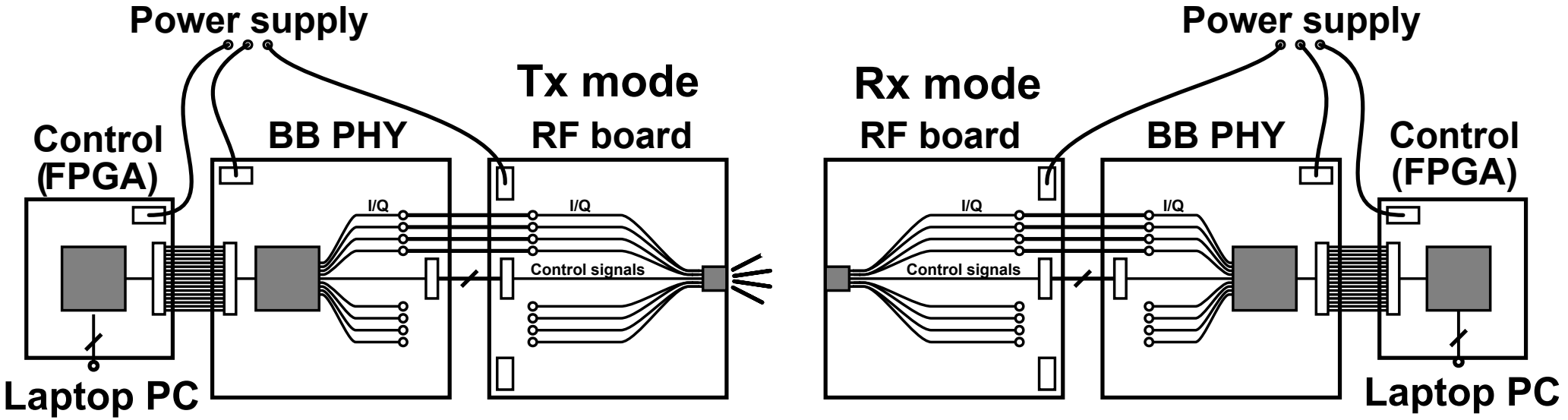
Chip with antenna in package

The 60GHz RF chip are mounted on the antenna in package



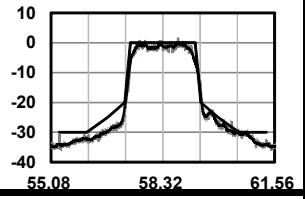
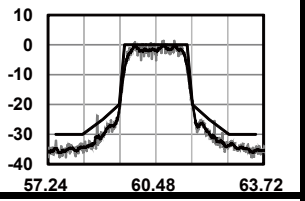
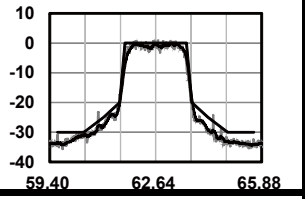
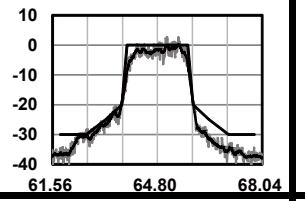
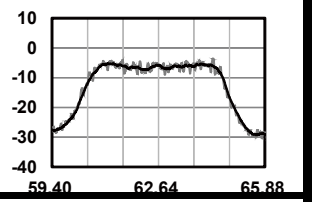
RF+BB Measurement Setup





R. Suga, *et al*., *EuMC* 2011

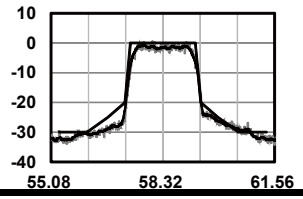
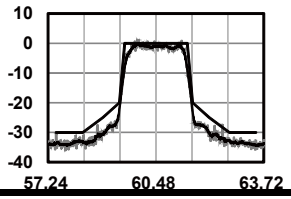
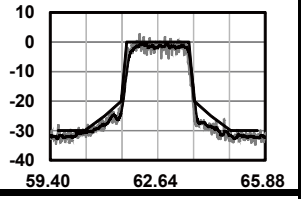
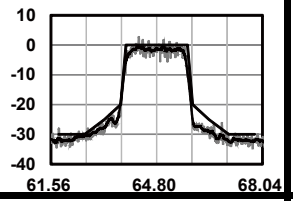
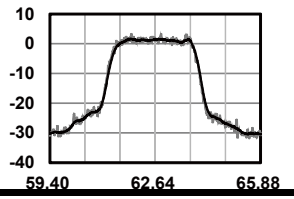
3.5Gb/s QPSK (max 8Gb/s)

Channel	ch.1	ch.2	ch.3	ch.4	Max rate
Constellation					
Spectrum					
Back-off	3.8dB	3.9dB	4.4dB	5.0dB	4.4dB (ch.3)
Data rate*	3.5Gb/s	3.5Gb/s	3.5Gb/s	3.5Gb/s	8.0Gb/s (ch.1-ch.4)
EVM	-21.2dB	-21.6dB	-21.4dB	-20.1dB	-17.3dB (ch.3)
Distance**	1.3m	1.4m	1.6m	1.6m	>0.01m (ch.3)

*The roll-off factor is 0.25. The bandwidth is 2.16GHz except for Max rate.

**Maximum distance within a BER of 10^{-3}. The 6-dBi antenna in the package is used.

7.0Gb/s 16QAM (max 10Gb/s)

Channel	ch.1	ch.2	ch.3	ch.4	Max rate
Constellation					
Spectrum					
Back-off	4.4dB	4.6dB	5.0dB	5.7dB	5.0dB (ch.3)
Data rate*	7.0Gb/s	7.0Gb/s	7.0Gb/s	7.0Gb/s	10.0Gb/s (ch.3)
EVM	-23.0dB	-23.0dB	-23.3dB	-22.8dB	-23.0dB (ch.3)
Distance**	0.3m	0.5m	0.5m	0.3m	>0.01m (ch.3)

*The roll-off factor is 0.25. The bandwidth is 2.16GHz except for Max rate.

**Maximum distance within a BER of 10^{-3}. The 6-dBi antenna in the package is used.

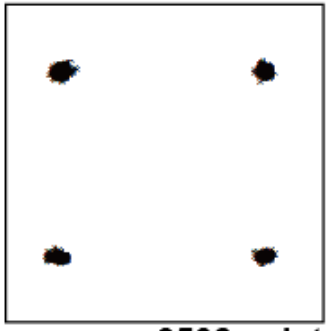
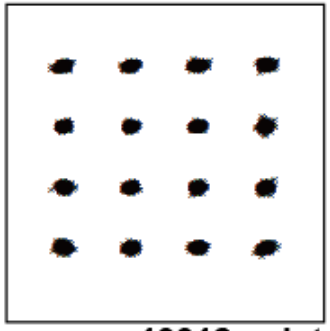
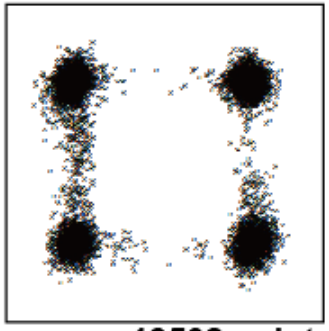
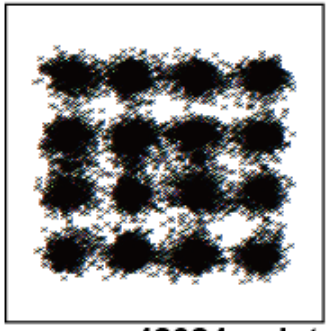
Performance Comparison

	Integration	#ch.	Data rate (16QAM)	P_{DC} (Tx/Rx)
Tokyo Tech [1]	RF (Direct)	2	11Gb/s [1] 16Gb/s [4]	252mW / 172mW
CEA-LETI [5]	RF (Hetero)	4	3.8Gb/s	1,357mW / 454mW
SiBeam [6]	RF (Hetero)	2	3.8Gb/s	1,820mW / 1,250mW
Tokyo Tech (This work)	RF (Direct) + analog /digital BB	4	RF: w/ wider-BW 10Gb/s RF+BB: 6.3Gb/s	RF: 319mW / 223mW BB: 196mW / 398mW

[1] K. Okada, *et al*., *ISSCC* 2011 [4] H. Asada, *et al*., *A-SSCC* 2011 [5] A. Siligaris, *et al*., *ISSCC* 2011 [6] S. Emami, *et al*., *ISSCC* 2011

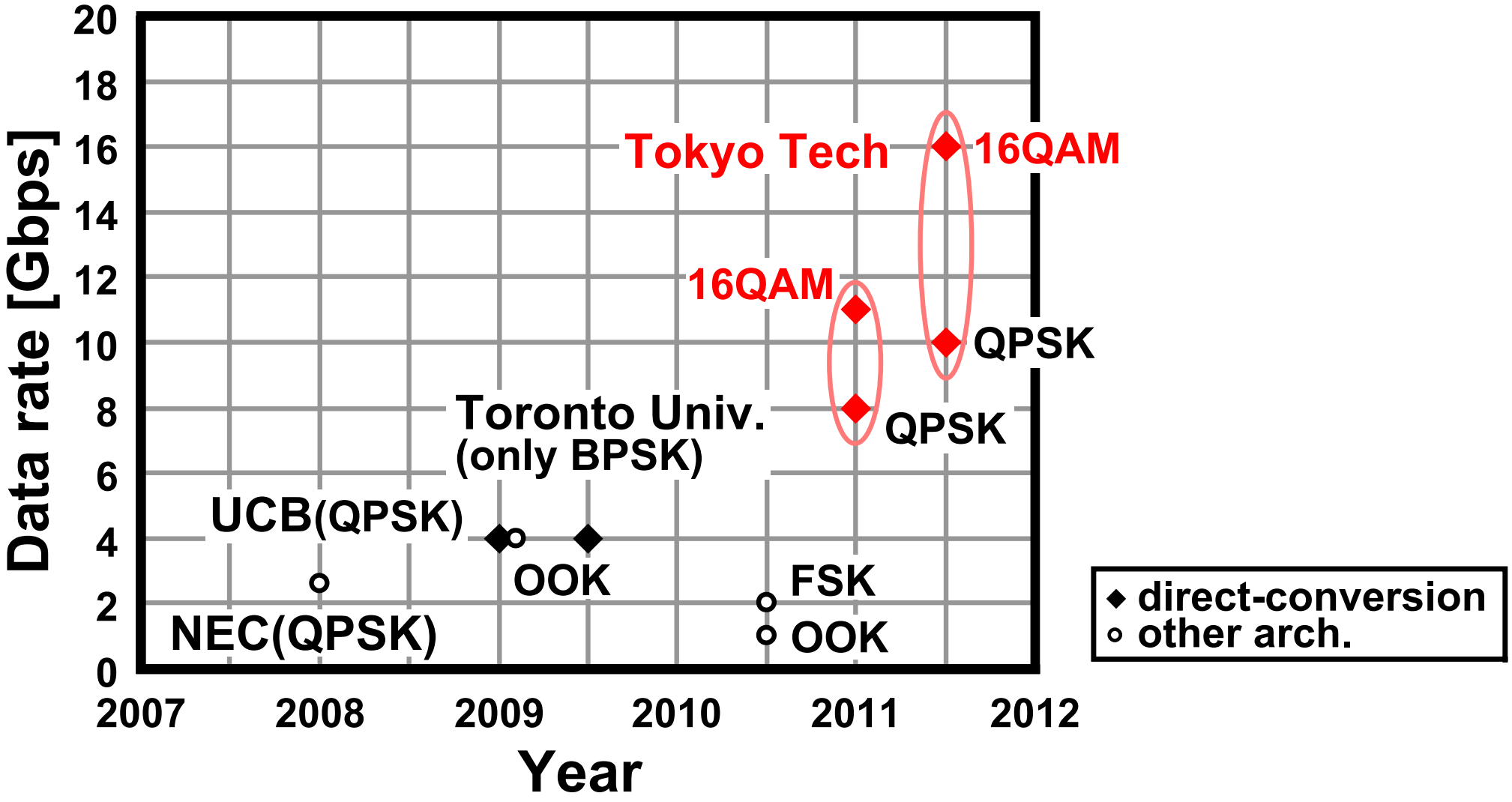
Recent measurement results

Attains the world fastest data rate of 16Gbps in wireless systems

Constellation	 9506 points	 19912 points	 13502 points	 42024 points
Modulation	QPSK	16QAM	QPSK	16QAM
Symbol rate	1.76GS/s	1.76GS/s	5.0GS/s	4.0GS/s
Data rate	3.52Gb/s	7.04Gb/s	10.0Gb/s	16.0Gb/s
EVM (withDFE)	-30.5dB	-28.2dB	-15.2dB	-16.1dB

Performance Comparison

Attains the world fastest data rate of 16Gbps in wireless systems

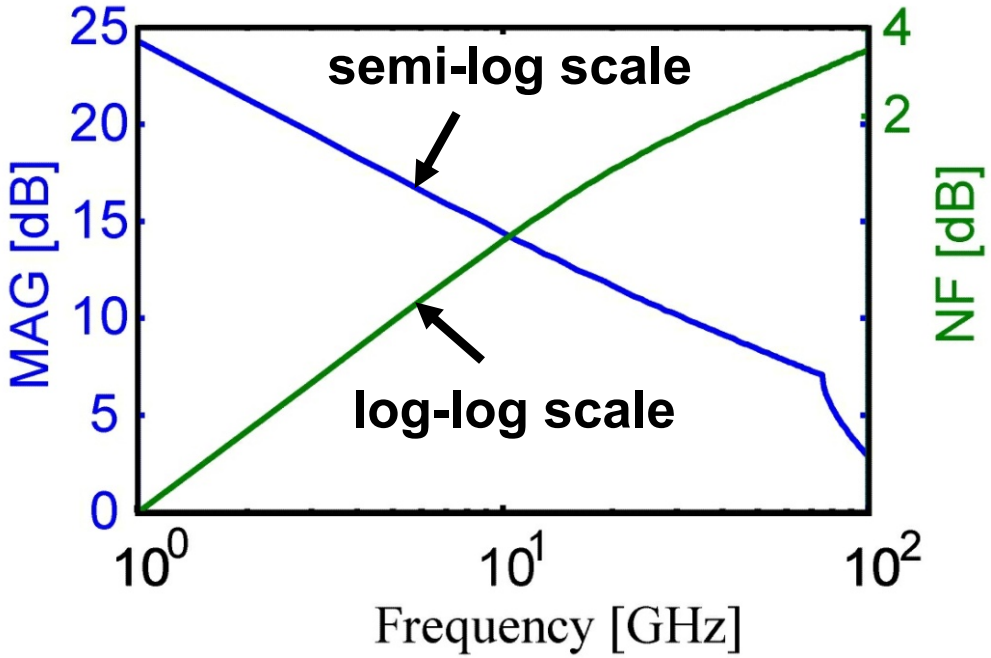


Essence of millimeter wave IC design

Gain and Noise; f_{max} and f_T

Gain and noise are mainly determined by f_{max} and f_T of Transistor

- ☹ Lower gain
  - ☹ MAG is inversely proportional to the logarithm of the operating frequency f_c.
- ☹ Higher noise
  - ☹ NF_{min} is proportional to the operating frequency f_c.



65nm NMOS

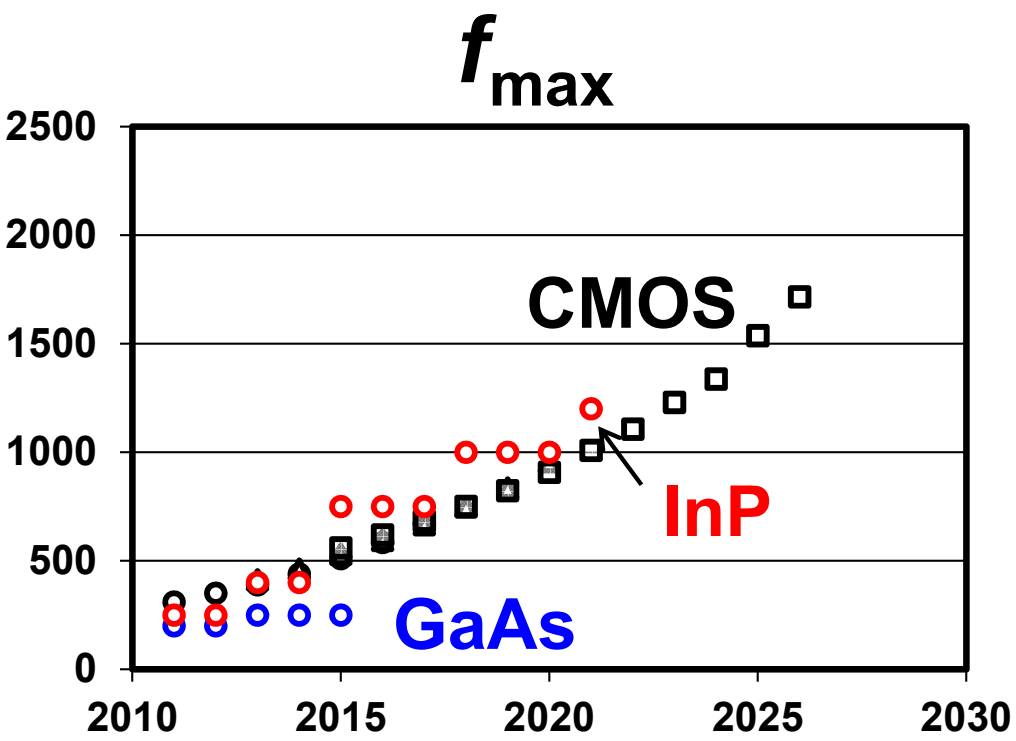
W_f=2.5μm, N_f=32, V_{gs}=0.8V and V_{ds}=0.8V.

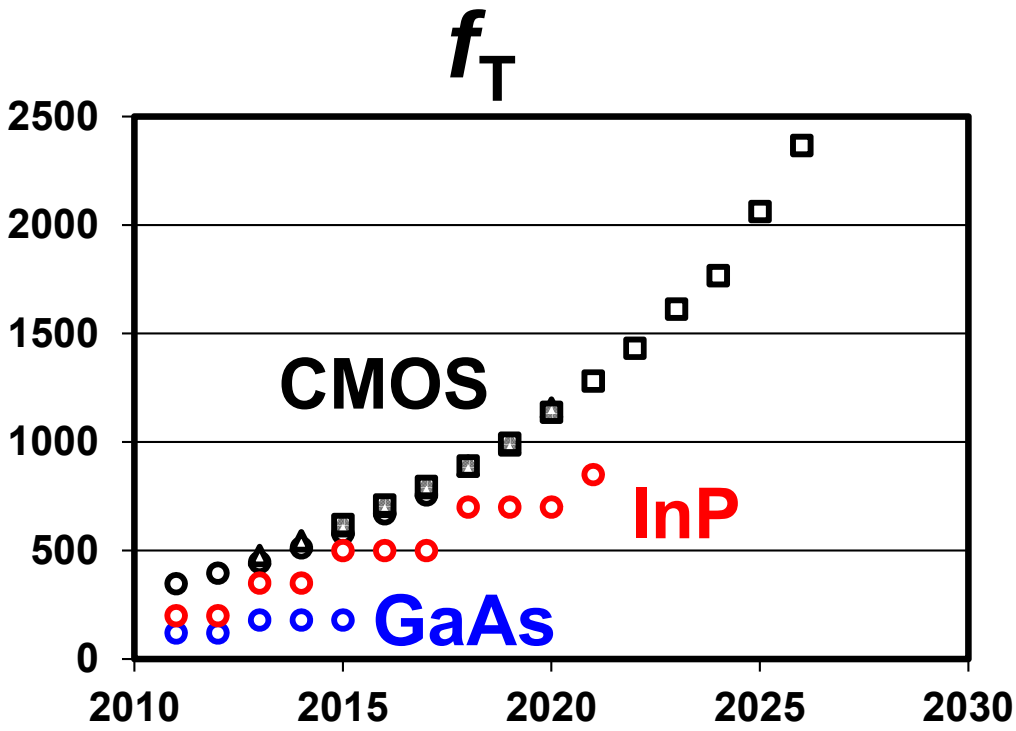
$$G_{\max} \approx \frac{f_{\max}}{f_c}$$

$$NF_{\min} \approx 1 + \left(\frac{f_c}{f_T}\right)\sqrt{1.3 g_m \left(R_g + R_s\right)}$$

Expected f_{max} and f_T

f_{max} and f_T of MOS transistor are expected to increase continuously



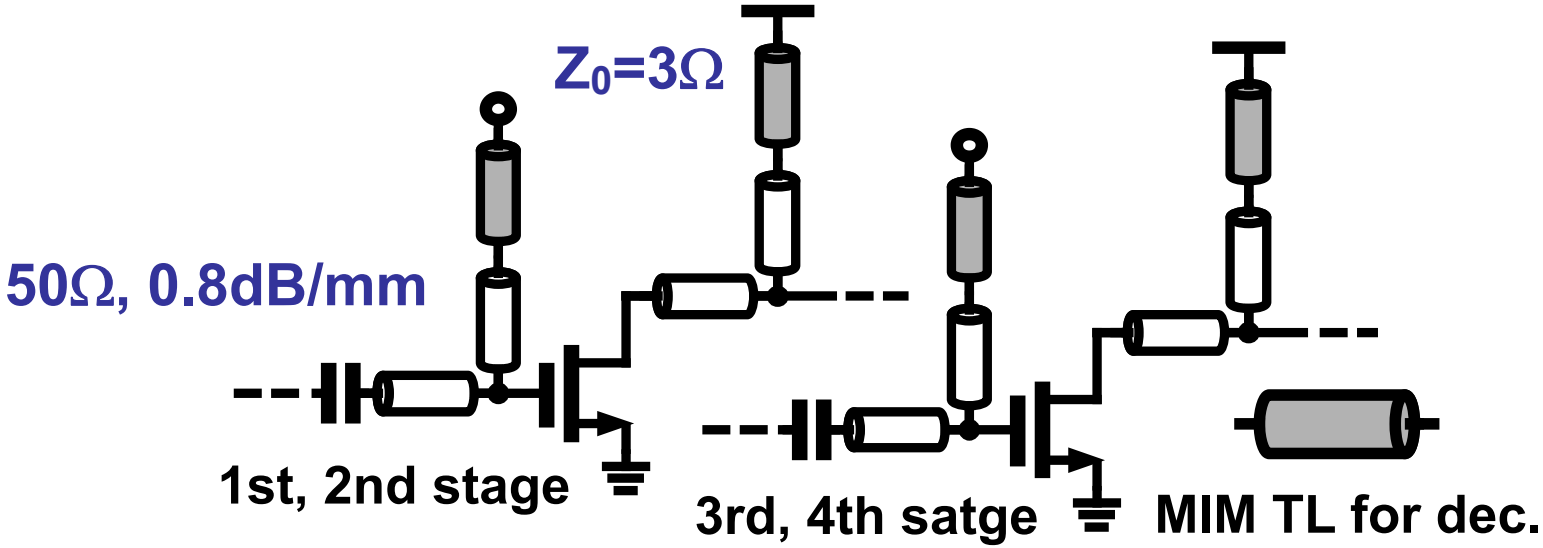


- ○ Bulk CMOS
- △ Ultra-Thin-Body Fully-Depleted (UTB FD) SOI
- □ Multi-Gate MOSFETs

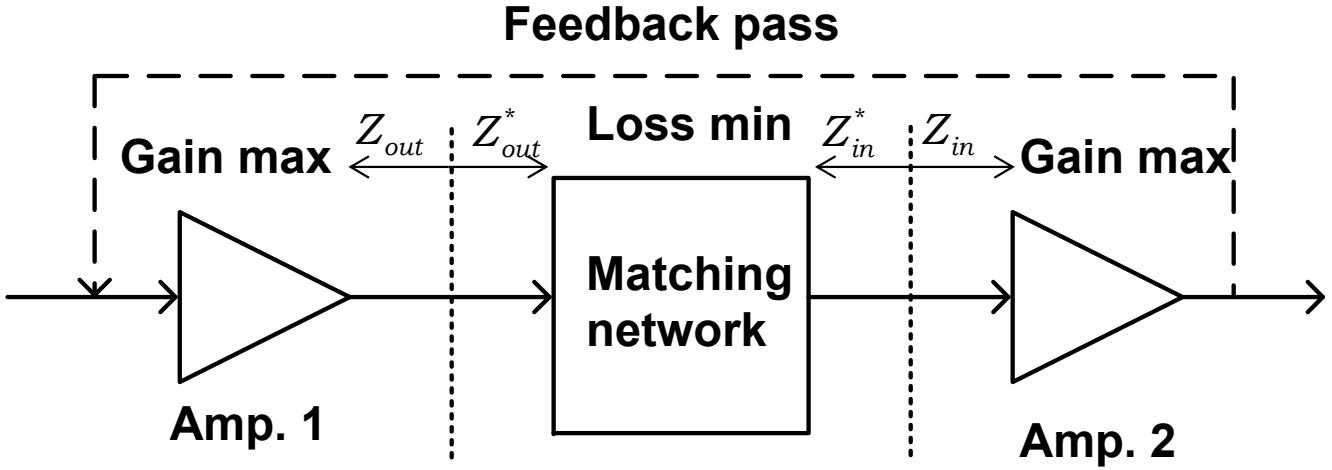
ITRS RFAMS 2011.

Amplifier design

Amplifier design;
accurate sizing, biasing, impedance matching and decoupling.



A several GHz oscillation will occur, if the feedback passes are made.

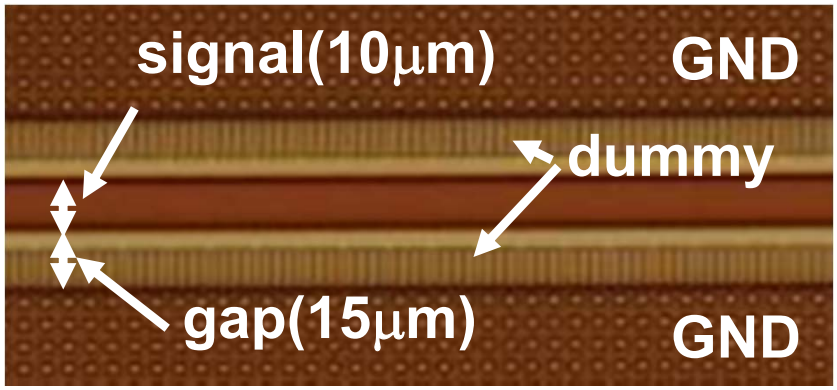


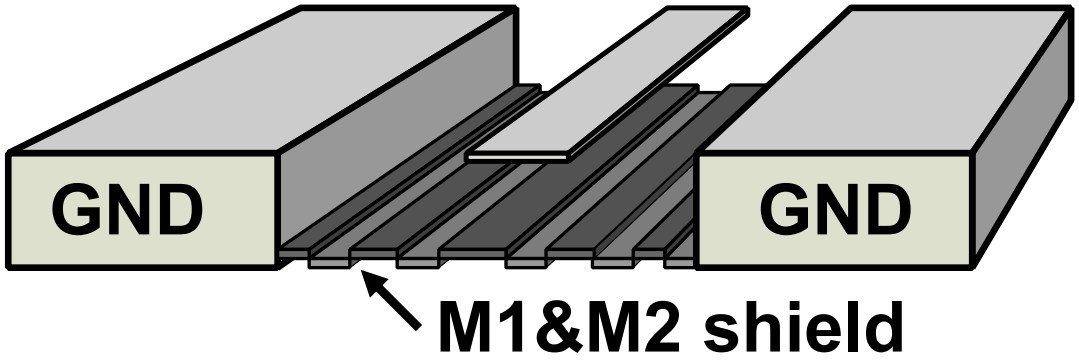
Low loss TR line

Transmission line, transformer, and decoupling capacitor are developed.

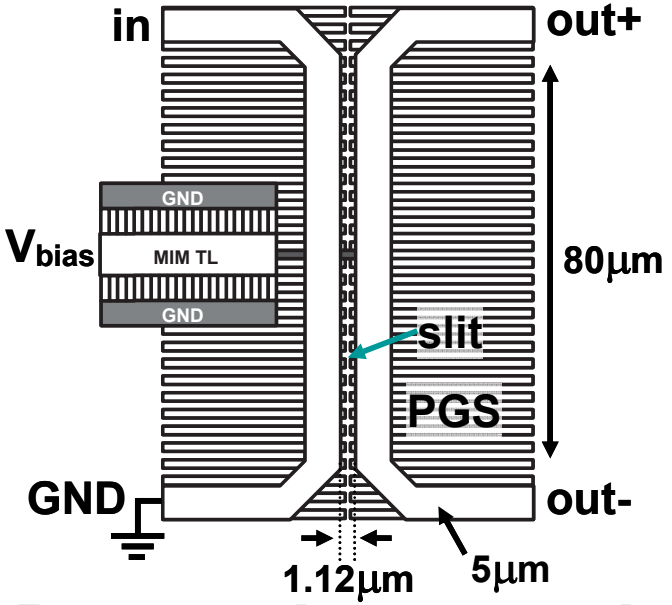
Transmission line

0.8dB/mm
Manually-placed dummy metal

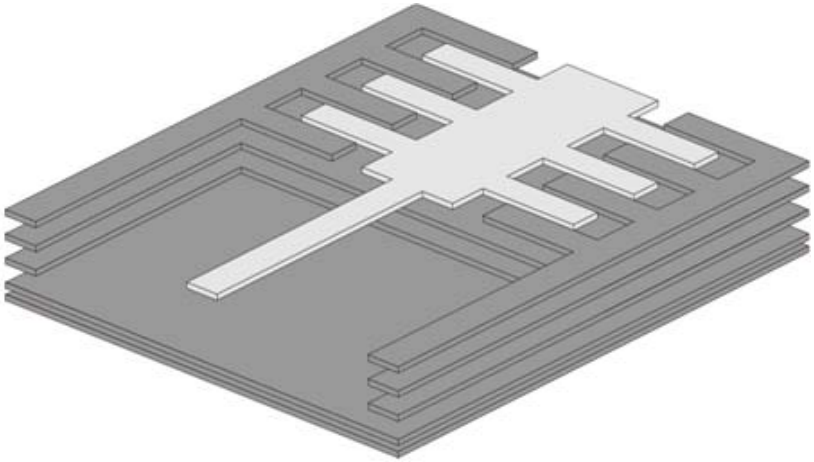




Transformer

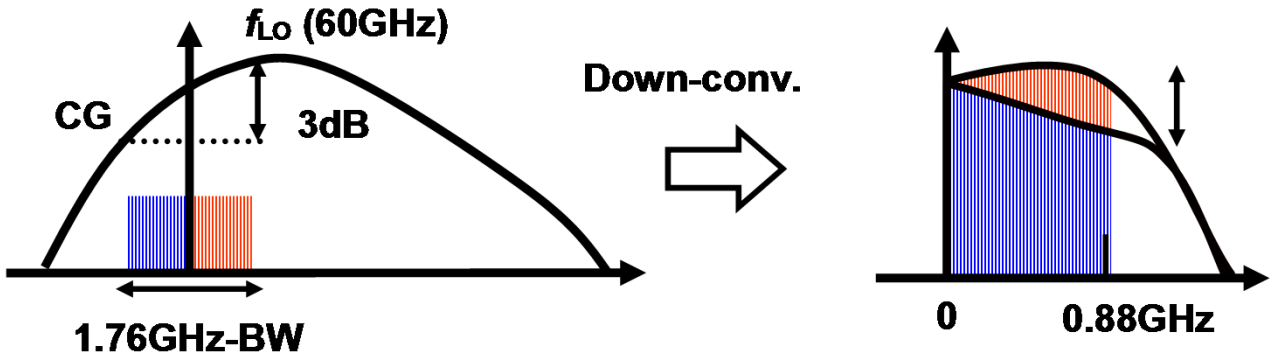


Decoupling capacitor

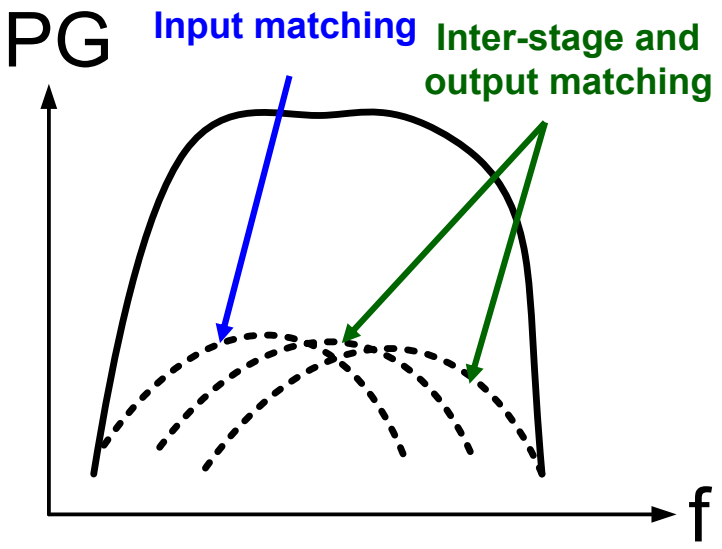


Gain flatness

A gain flatness causes ISI for QAM signal and results in increase of BER. Adjusting the impedance matching to reduce the gain flatness.



Gain Flatness	0dB	2dB	3dB
BER	~0	1.3e-5	3e-3
Constellation			

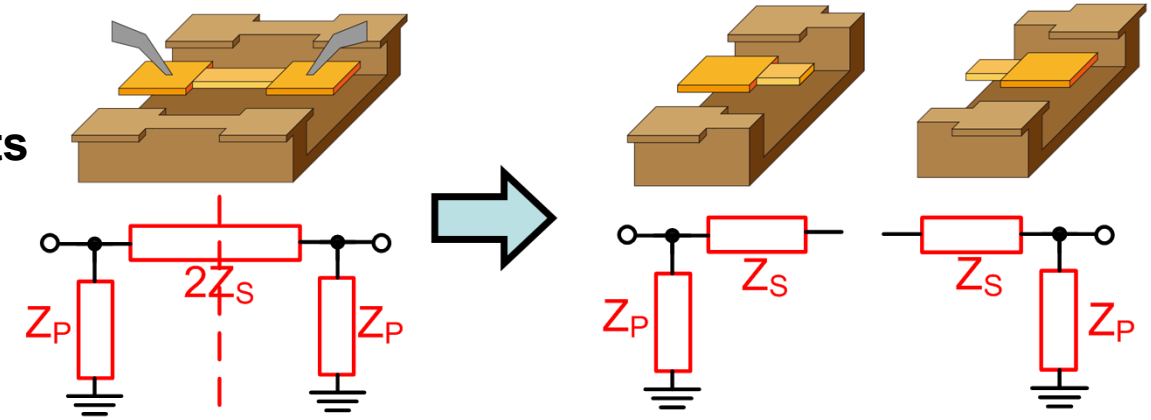


Modeling (De-embedding) tequnique

Through only method

Inaccurate due to interference between PADs

Measure the PAD and lead parts



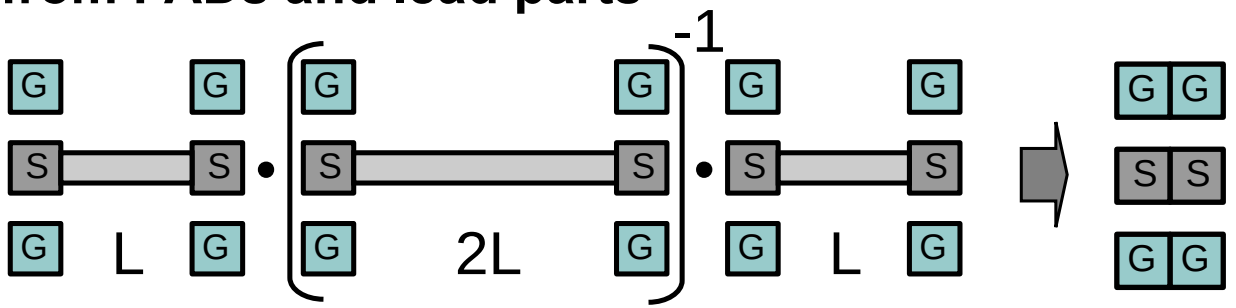
Thru (short line) structure

Pad model

L-2L Method

Measure with L (200um) and 2L (400um) transmission lines

No affect of interference from PADs and lead parts



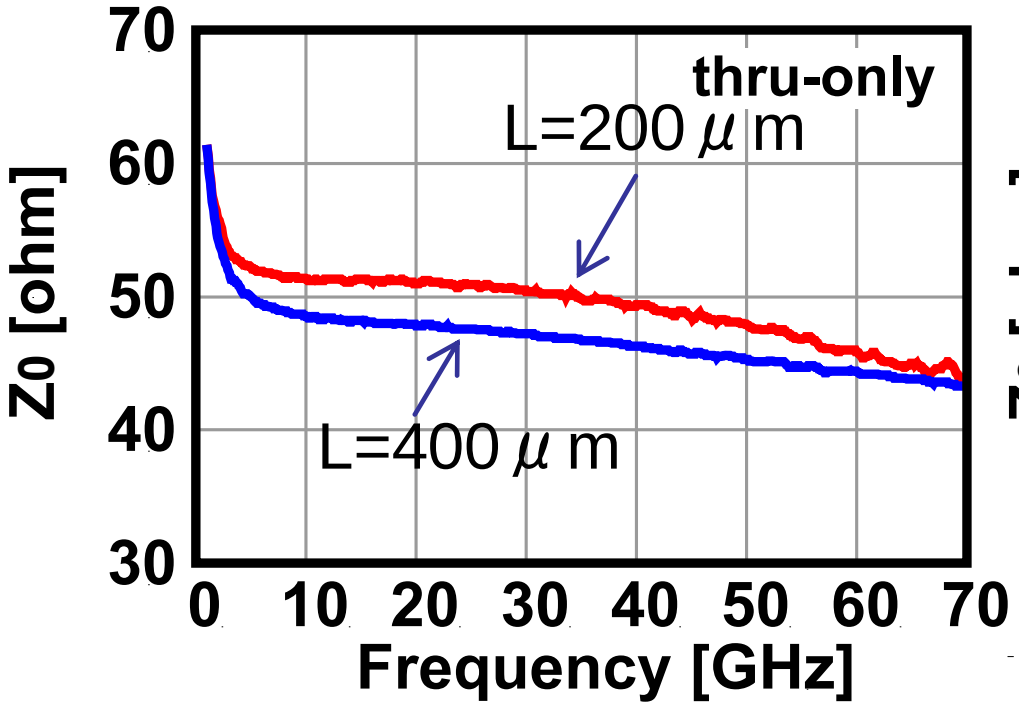
$$\mathbf{T}_{lpad} \cdot \mathbf{T}_{TL} \cdot \mathbf{T}_{rpad} \cdot \left(\mathbf{T}_{lpad} \cdot \mathbf{T}_{TL} \cdot \mathbf{T}_{TL} \cdot \mathbf{T}_{rpad}\right)^{-1} \cdot \mathbf{T}_{lpad} \cdot \mathbf{T}_{TL} \cdot \mathbf{T}_{rpad} = \mathbf{T}_{lpad} \cdot \mathbf{T}_{rpad}$$

A. M. Mangan, et al., IEEE Trans. on Electron Devices, vol. 53, no. 2, pp.235-241, Feb. 2006
N. Takayama, K. Okada, and A. Matsuzawa, et al., IEEE Asia-Pacific Microwave Conference (APMC), Singapore, Dec. 2009.

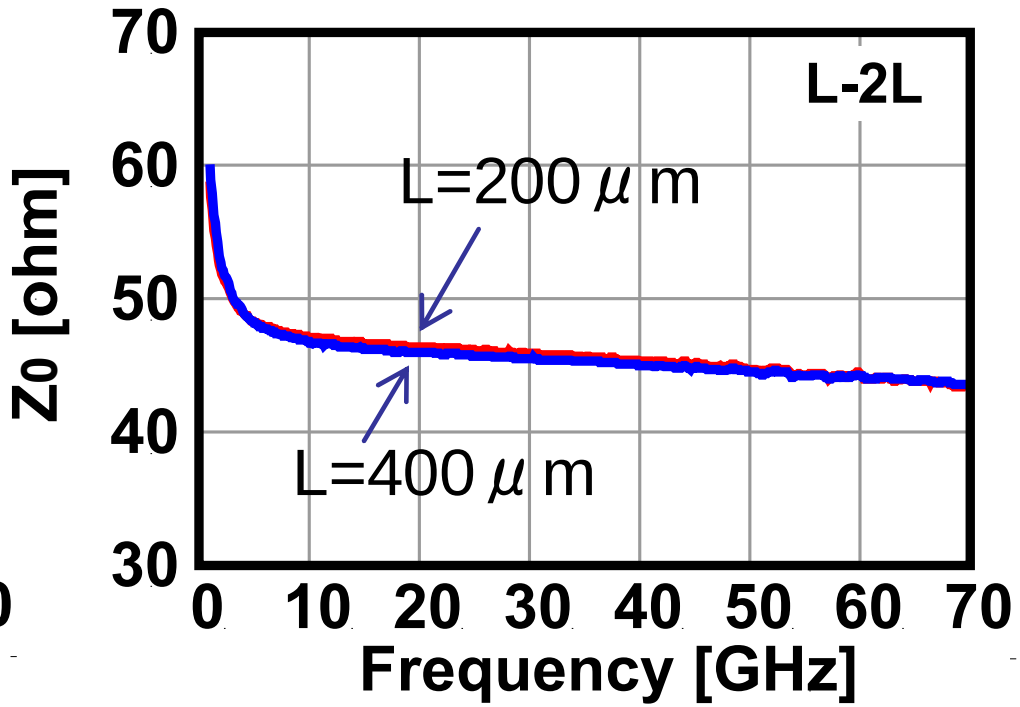
Measurement results

An accurate device modeling with proper measurement method is vitally important for very high frequency circuit design. The performance of millimeter wave circuits is mostly determined by The accuracy of modeling for passive and active devices.

Through only method

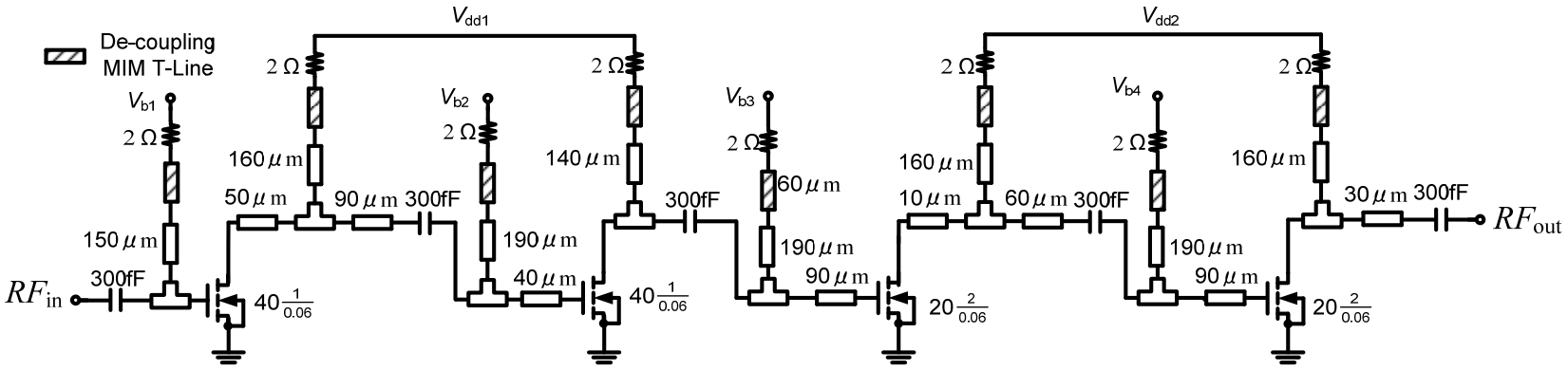


L-2L Method

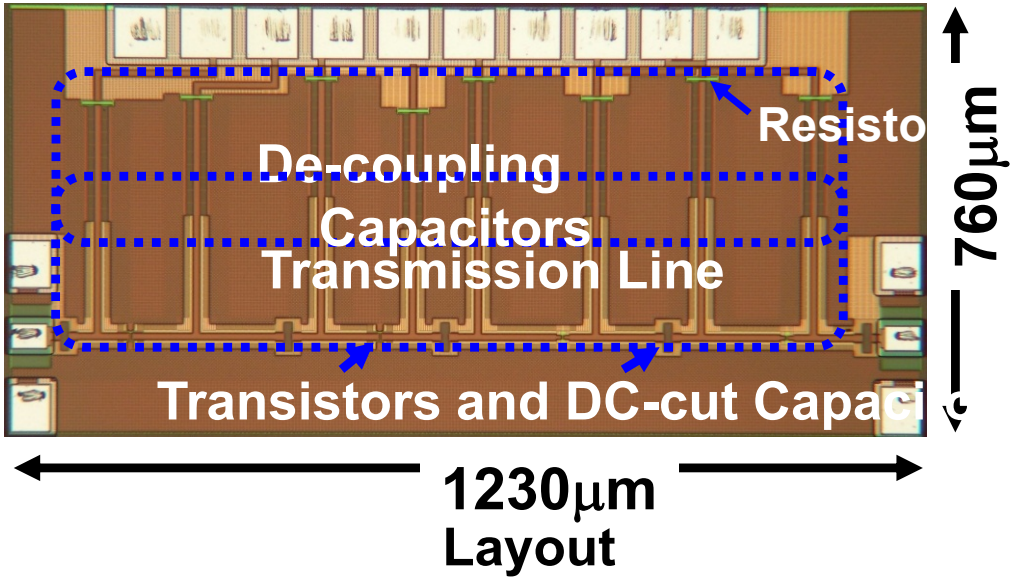


60GHz CMOS LNA

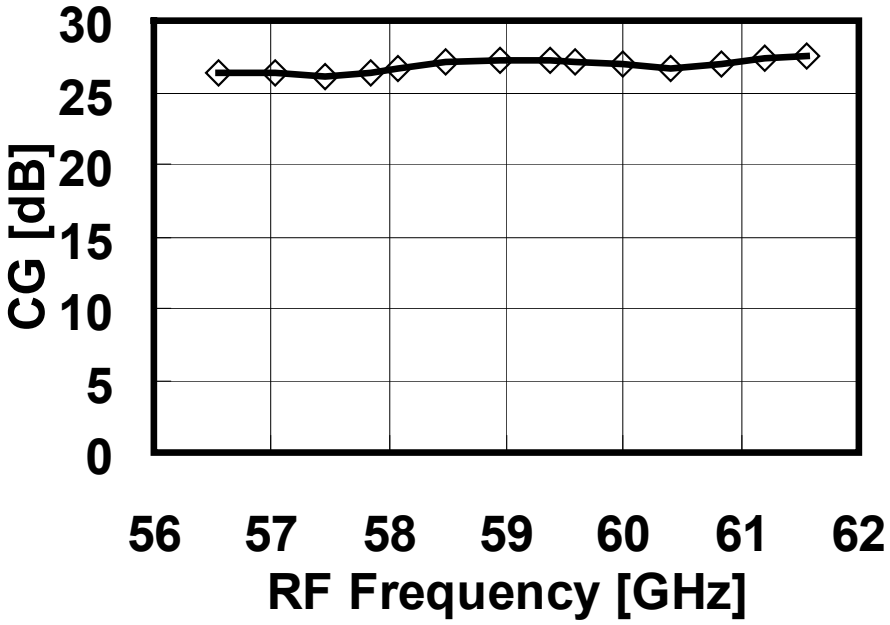
A multi stage non-cascode CMOS LNA realizes wide gain flatness.



Four gain stages without cascodes



Gain flatness



Comparison in LNA

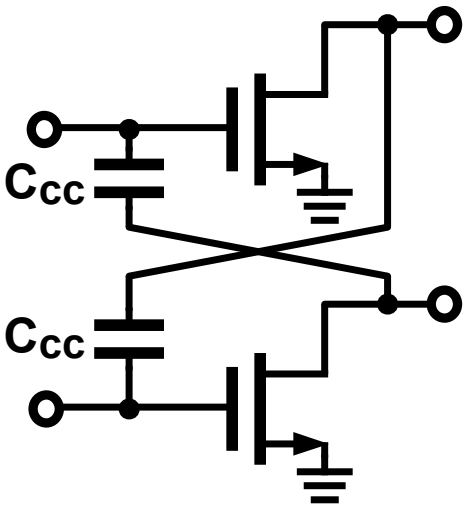
	[1]	[2]	[3]	[4]	[5]	[6]	This work
Tech.	90nm	90nm	90nm	90nm	65nm	90nm	65nm
Topology	CS	Cas.	Cas.	CS	Diff. Cas.	Cas.	CS-CS
#Stage	3	2	2	2	3	3	4
BW [GHz]	5	6	8	-	7.7	14	17
Gain [dB]	15.0	14.6	15.5	12.2	19.3	20.0	24
NF [dB]	4.4	5.5	6.5	6.5	6.1	6.8	4.0-7.6
Power [mW]	3.9	24	86	10.5	35	36	30

[1] E. Cohen, *et al*., *RFIC* 2008 [2] T. Yao, *et al*., *JSSC* 2007 [3] S. Pellerano, *et al*., *JSSC* 2008 [4] B. Heydari, *et al*., *JSSC* 2007 [5] C. Weyers, *et al*., *ISSCC* 2008
[6] Y. Natsukari, *et al*., *VLSI Circuits* 2009

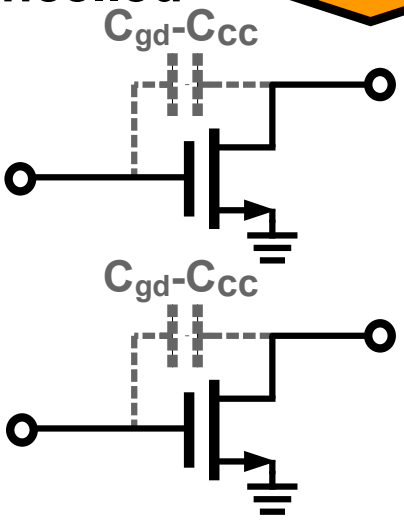
Ning Li, K. Okada, and A. Matsuzawa et al., ESSCIRC, Seville, Spain, pp.342-345, Sep. 2010.

Cross coupled feedback capacitors

Differential circuit



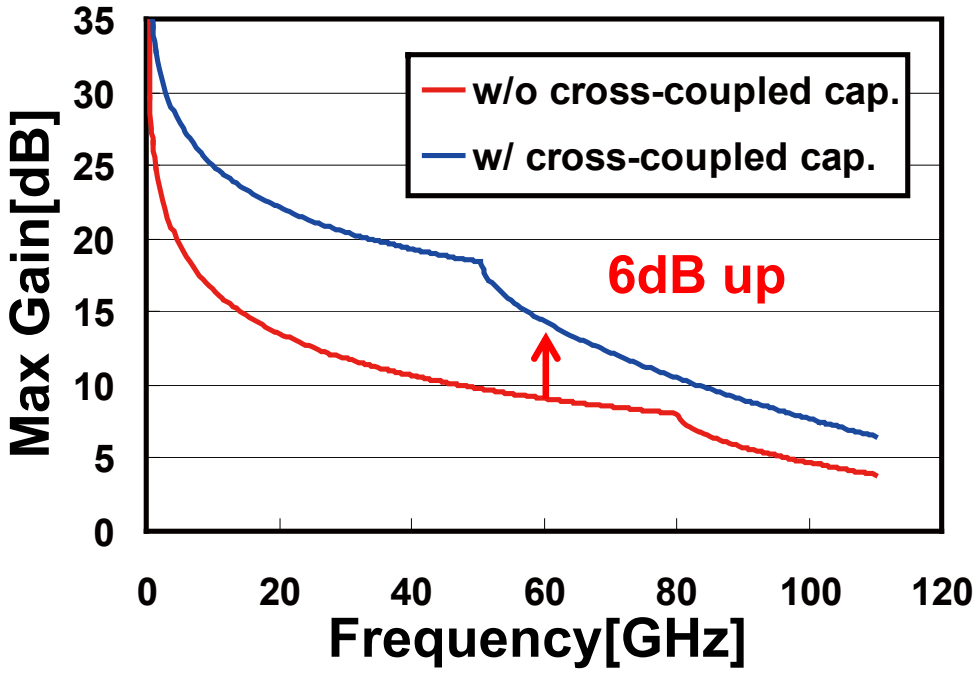
Capacitance is cancelled



Cross coupled feedback capacitors in a differential circuit can reduce the effective capacitance to increase the gain of 6dB at 60GHz.

$$f_{\max} = \frac{f_T}{2\sqrt{R_g g_m C_{gd} / (C_{gs} + C_{gd}) + (R_g + r_{ch} + R_s) g_{ds}}}$$

This term is reduced

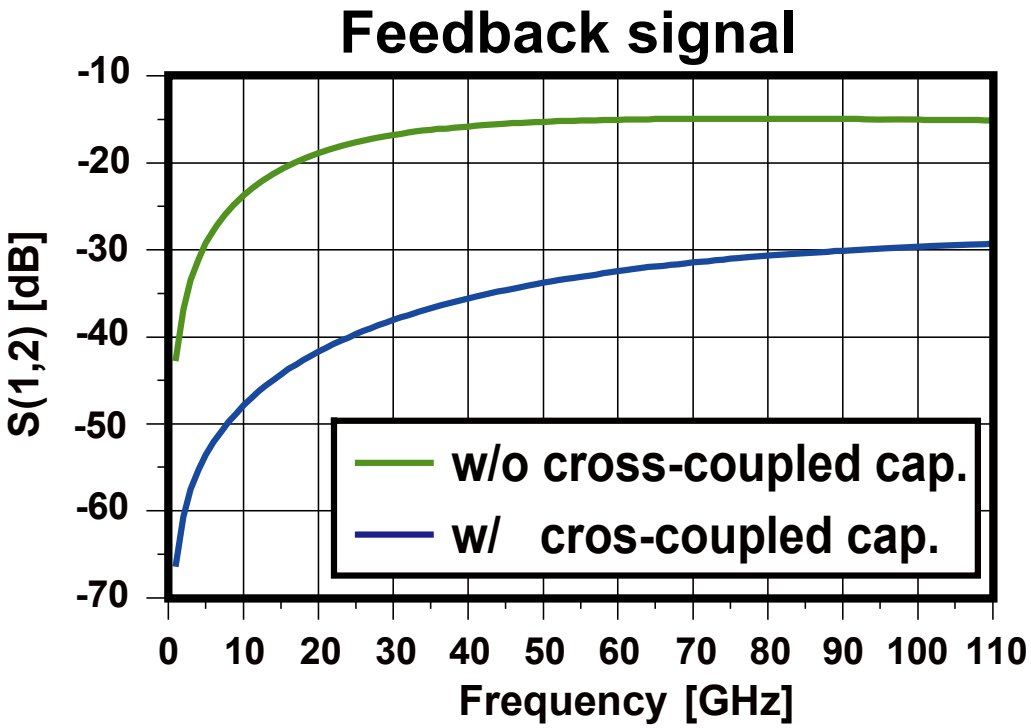


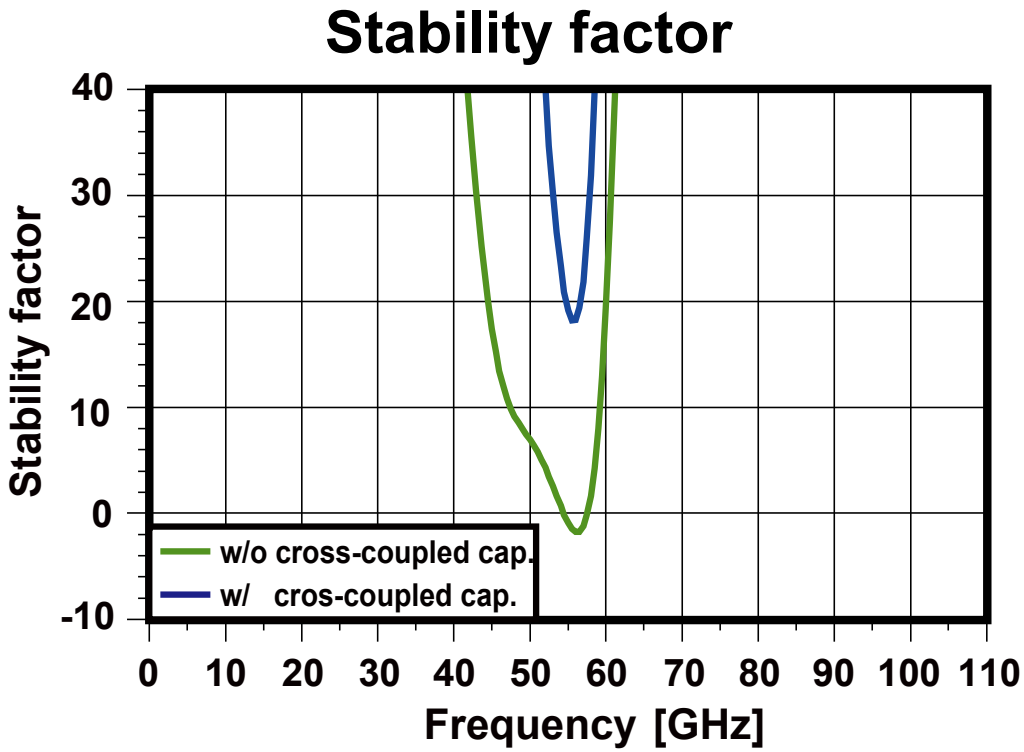
Y. Natsukari, et al., VLSI Circuits, Dig. Tech. Papers, pp. 252–253, June 2009.

W. L. Chan, et al., ISSCC. Tech. Dig., pp. 380–381, Feb. 2009.

Feedback signal and stability

Feedback signal is suppressed by the cross coupled capacitors and this increase the stability of amplifier.



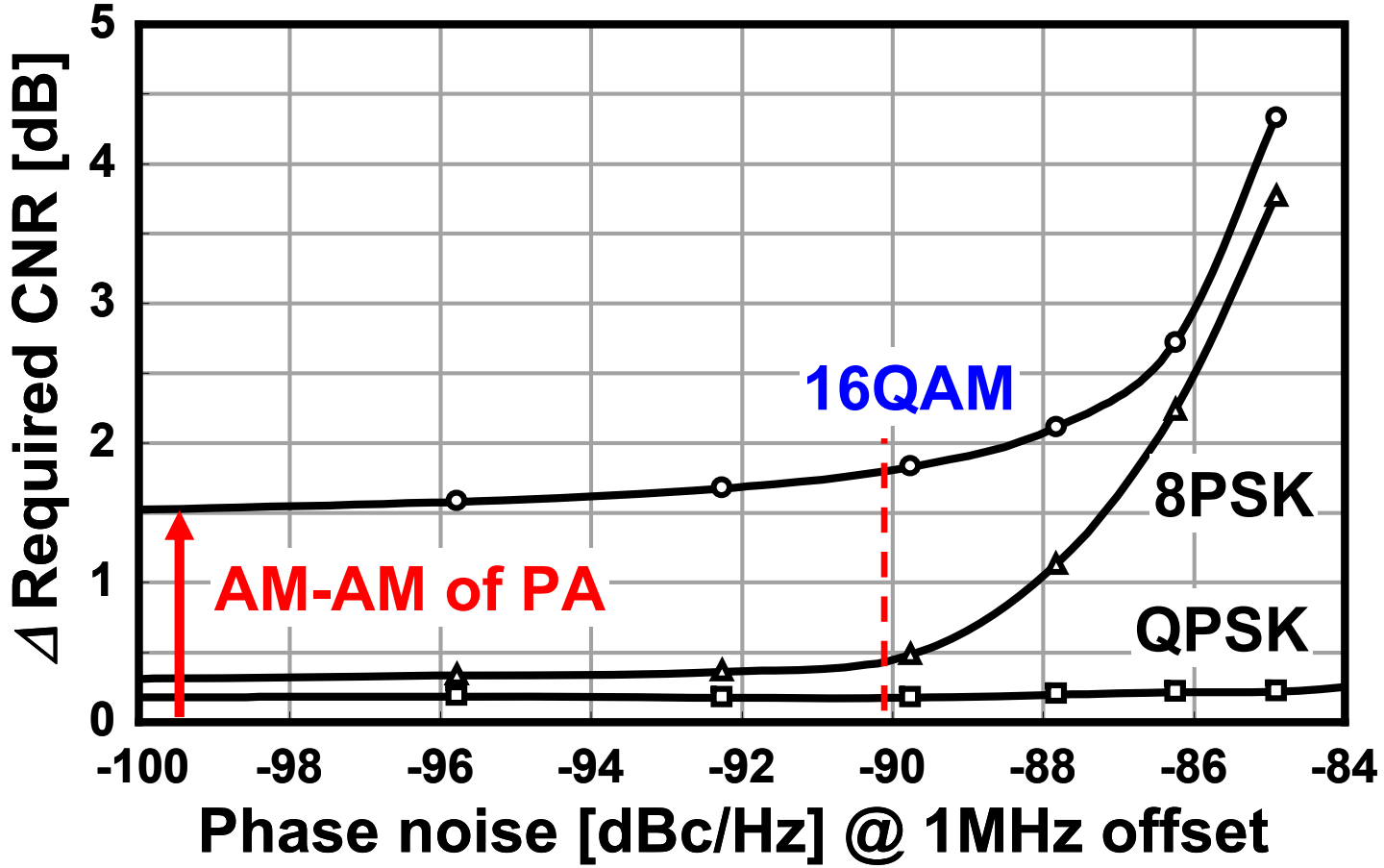


Required phase noise of IQ-VCO for 16QAM

A phase noise of LT. -90dBc/Hz@1MHz is required for 16QAM systems

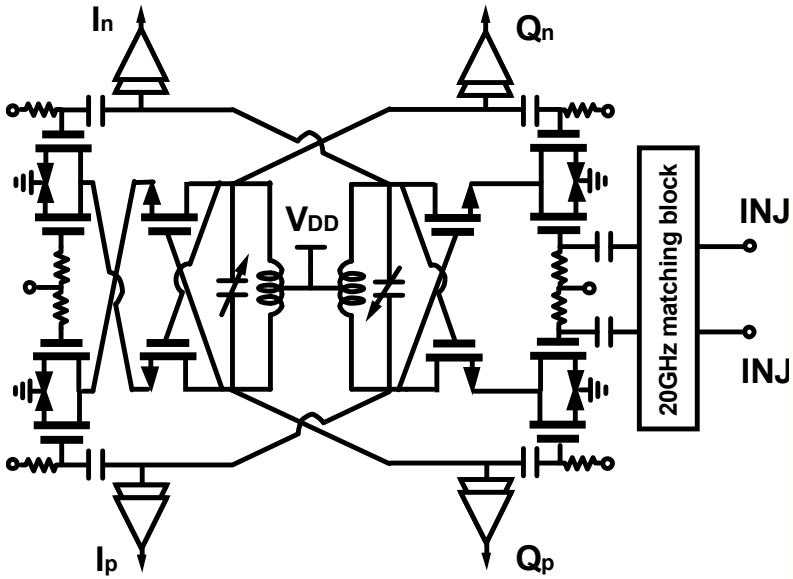
A reported phase noise of 60GHz IQ VCO is -76dBc/Hz @1MHz at most

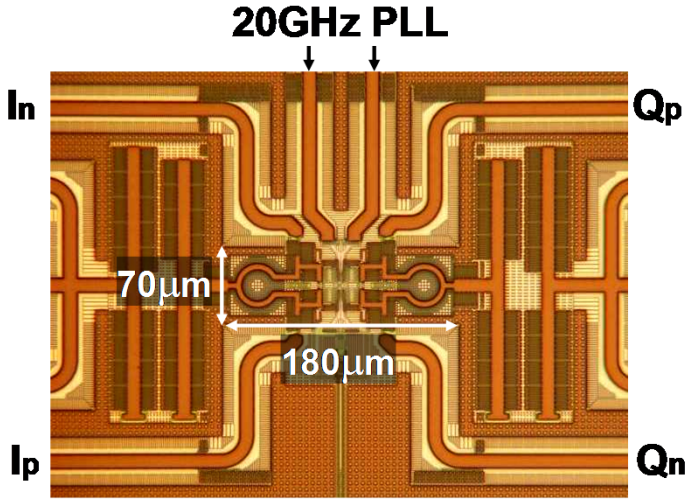
K. Scheir, et al., ISSCC, pp. 494-495,Feb. 2009.



Key technology: Quadrature ILO

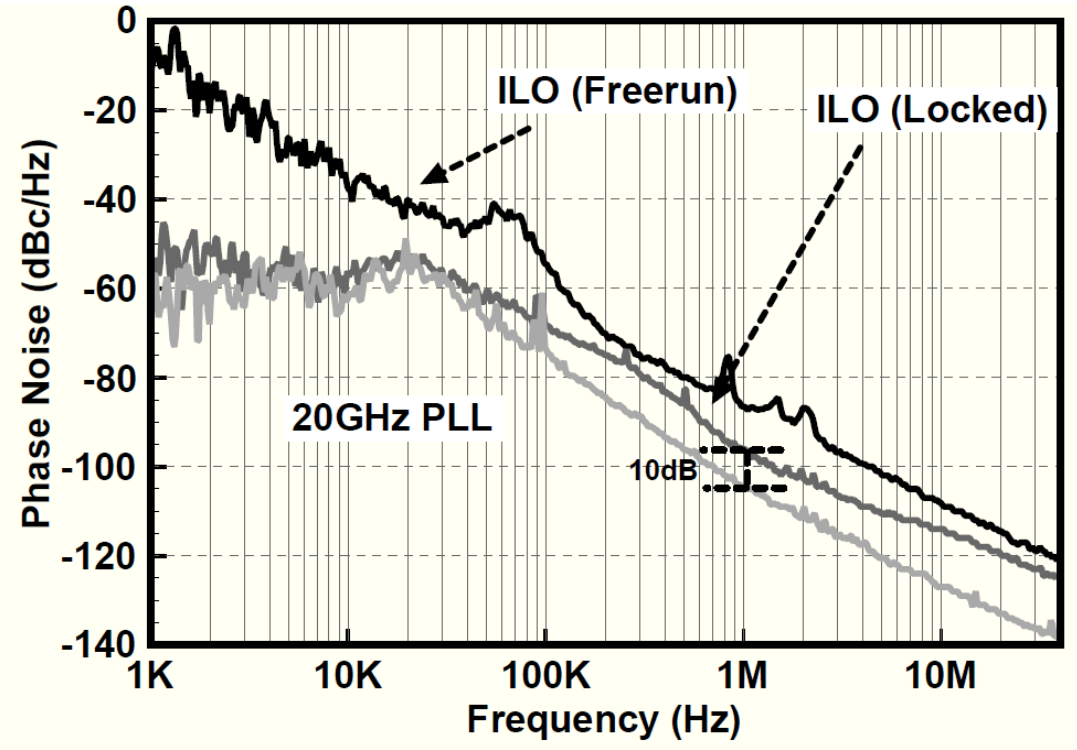
Quadrature injection locked 60GHz oscillator with 20GHz PLL
Low phase noise of -96dBc/Hz @1MHz.





Best phase noise is achieved.

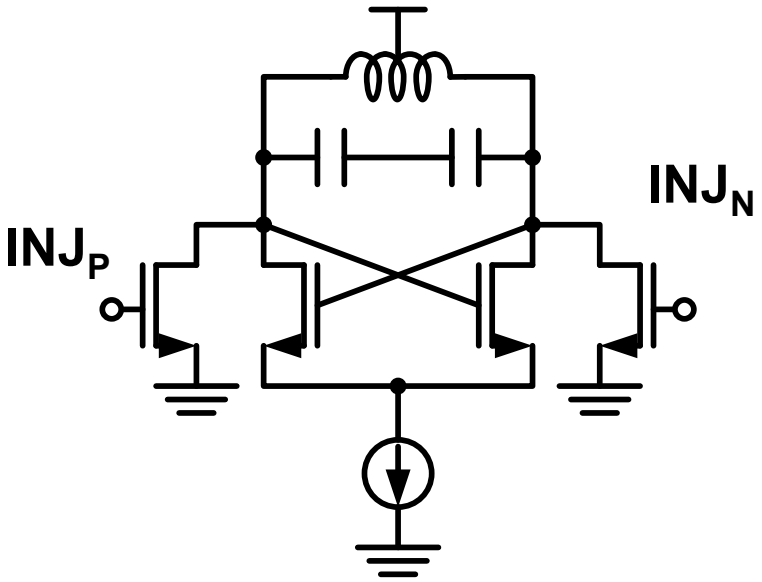
58-63GHz, -96dBc/Hz-1MHz offset



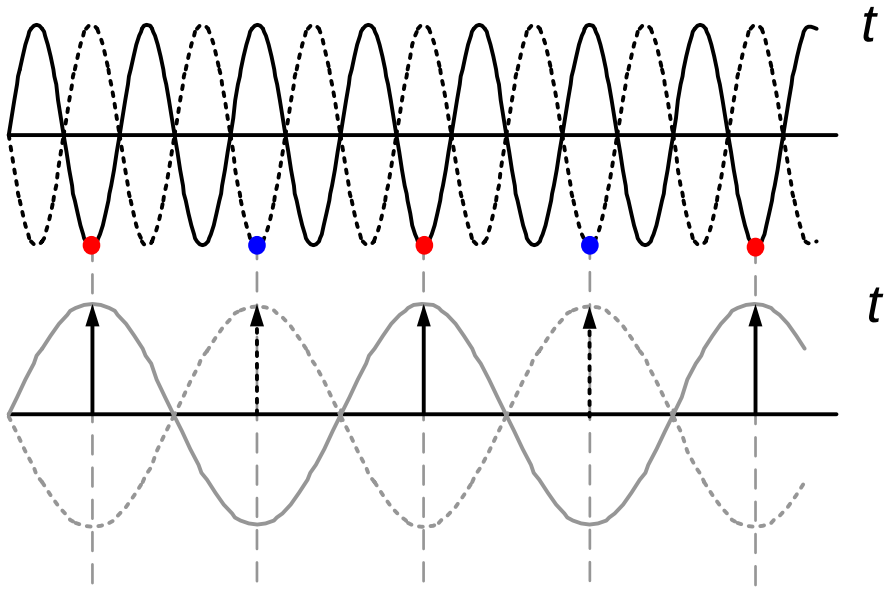
A. Musa, K. Okada, A. Matsuzawa., in A-SSCC Dig. Tech. Papers, pp. 101–102, Nov. 2010.

Injection locking method

Injection locking method is a very important circuit technique for high frequency signal generation and frequency divider. Phase noise of the oscillator is mandated by the injected signal.



parallel injection



Phase noise $PN_{\mathrm{ILO}} = PN_{\mathrm{INJ}} + 20\log(N)$

N: Multiple number

9.5dB @ N=3

Locking frequency range $f_L \approx \frac{f_o}{2Q} \cdot \frac{I_{inj}}{I_{OSC}}$

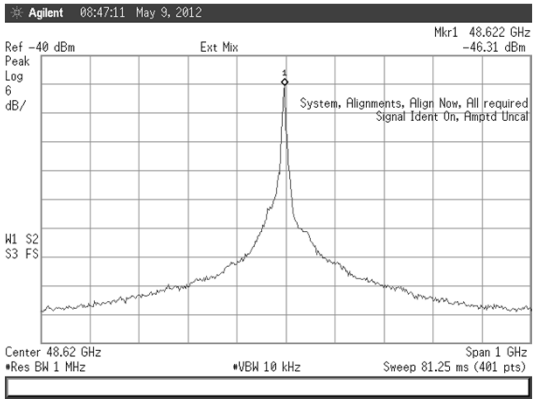
150GHz CMOS injection locked frequency divider

The injection locking methd is useful for high frequency divider.

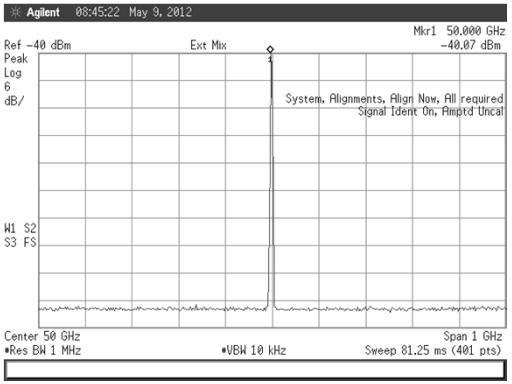
Technology	40nm 1P8M CMOS
Operating frequency	133.3GHz – 151.3GHz
Phase noise	-135.6dBc/Hz @1MHz offset
Power dissipation	12mW @V_{DD}=1.6V
Circuit size	8.8 × 5.3μm²

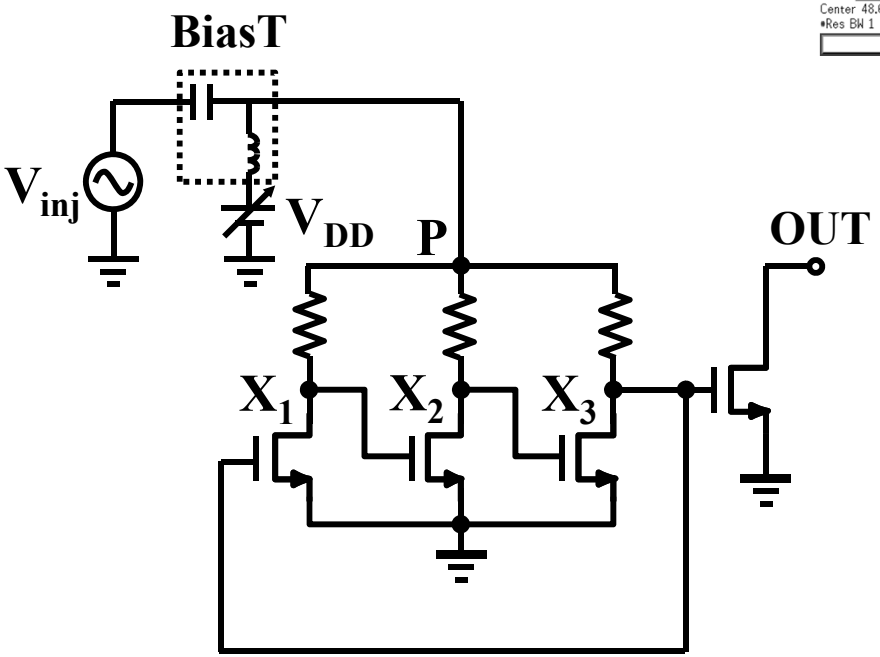
Divide the pulses → control oscillation frequency

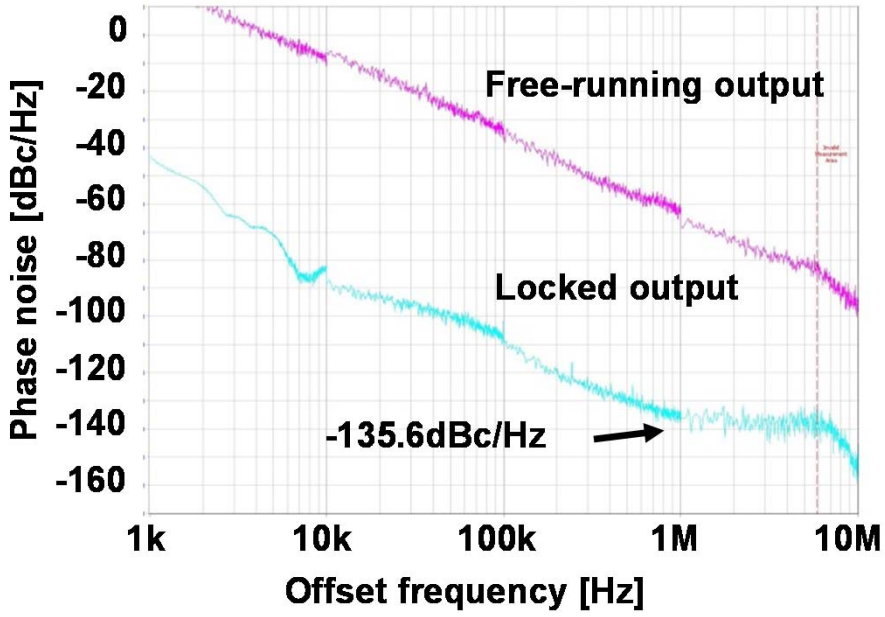
Free-running



Locked







M. Fujishima, et al., SSDM 2012

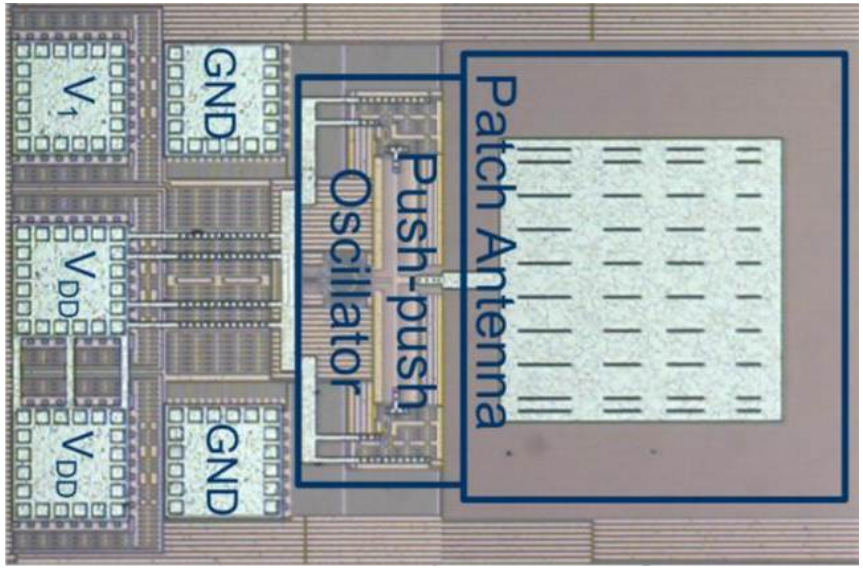
Further high frequency: CMOS Oscillator

Higher frequency can be obtained by CMOS oscillator, using push-push method.

410 GHz

E. Seok, *et al*., ISSCC 2008.

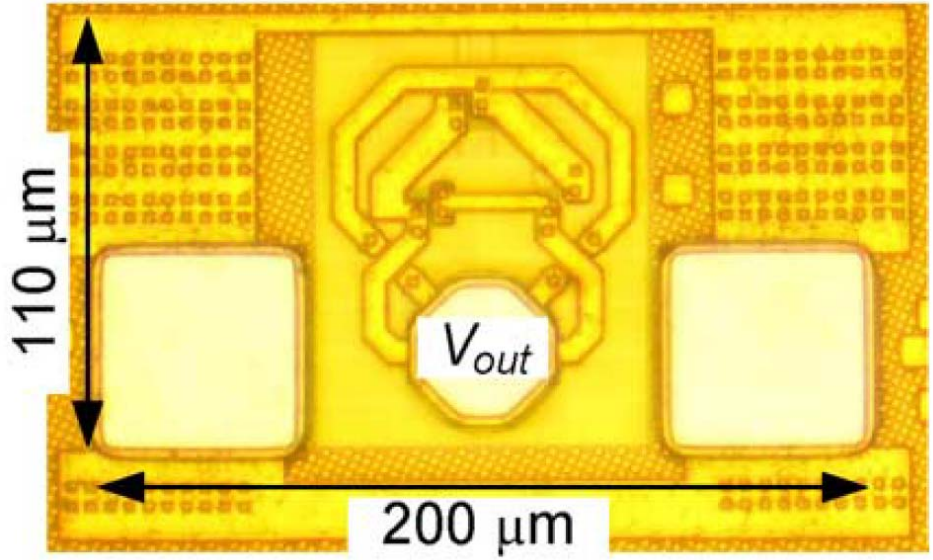
45nm CMOS Push-push Oscillator 205GHz oscillation with 410GHz harmonic output. 11mA @ 1.5V



486 GHz

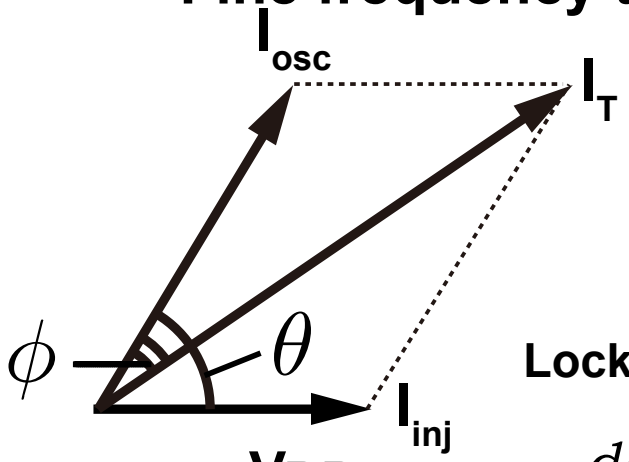
O. Momeni, *et al*., JSSC 2011.

65nm CMOS 486GHz using Triple-Push oscillation -7.9dBm from 61mW Pd.



Issue: Phase control of injection locking oscillator

Fine frequency tuning is required to attain low phase error

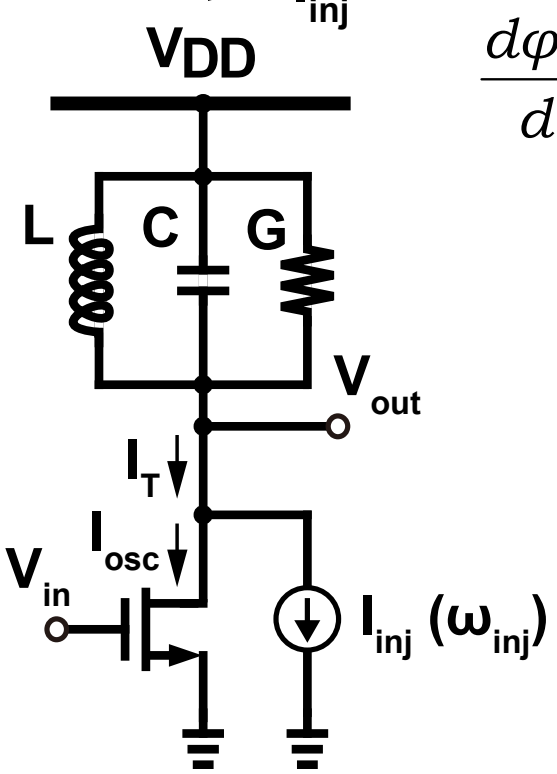


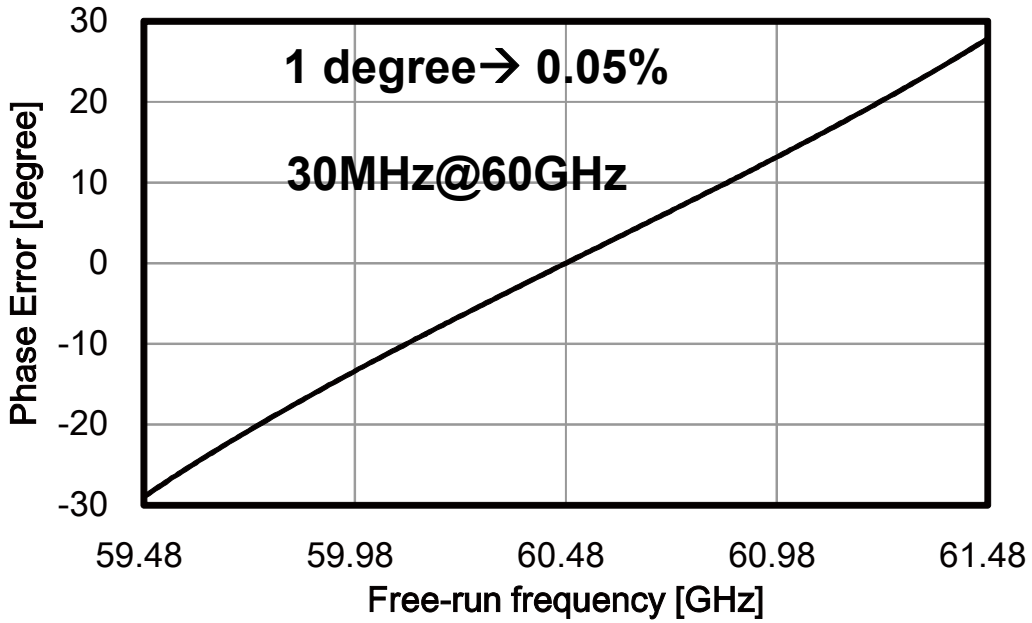
$$I_T \sin\varphi = I_{osc} \sin\theta$$

$$\frac{d\varphi(t)}{dt} = (\omega_0 - \omega_{inj}) - \omega_L \sin\{\varphi(t)\} \qquad \omega_L \approx \frac{\omega_o}{2Q} \cdot \frac{I_{inj}}{I_{OSC}}$$

Locked state

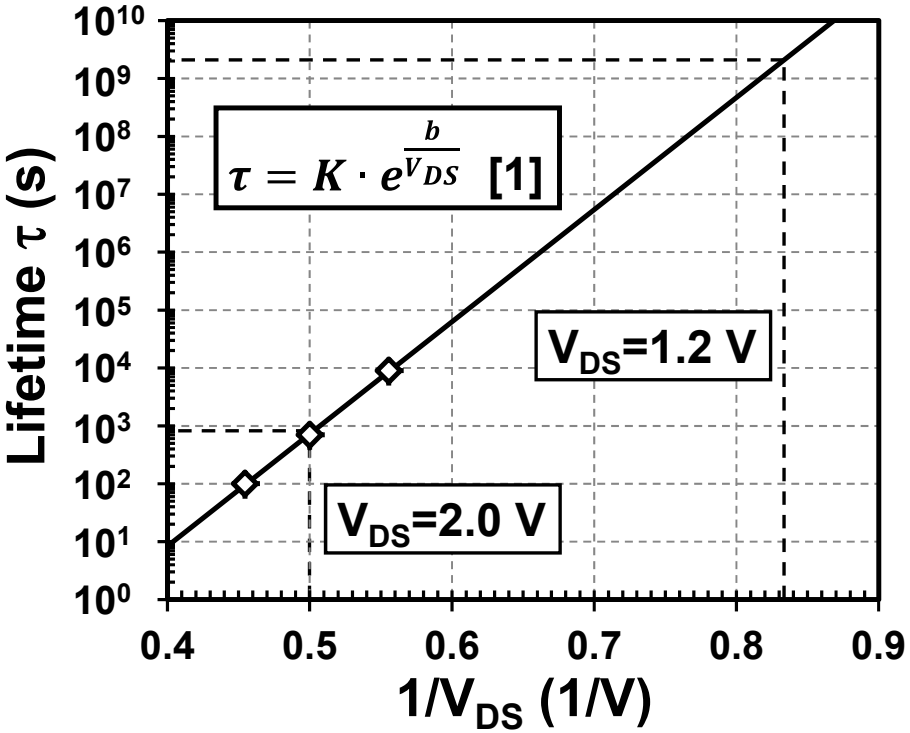
$$\frac{d\varphi(t)}{dt} = 0 \qquad \varphi(t) = \sin^{-1}\left(\frac{\omega_0 - \omega_{inj}}{\omega_L}\right) = \sin^{-1}\left\{2Q\left(\frac{\omega_0 - \omega_{inj}}{\omega_0}\right) \cdot \frac{I_{osc}}{I_{inj}}\right\}$$

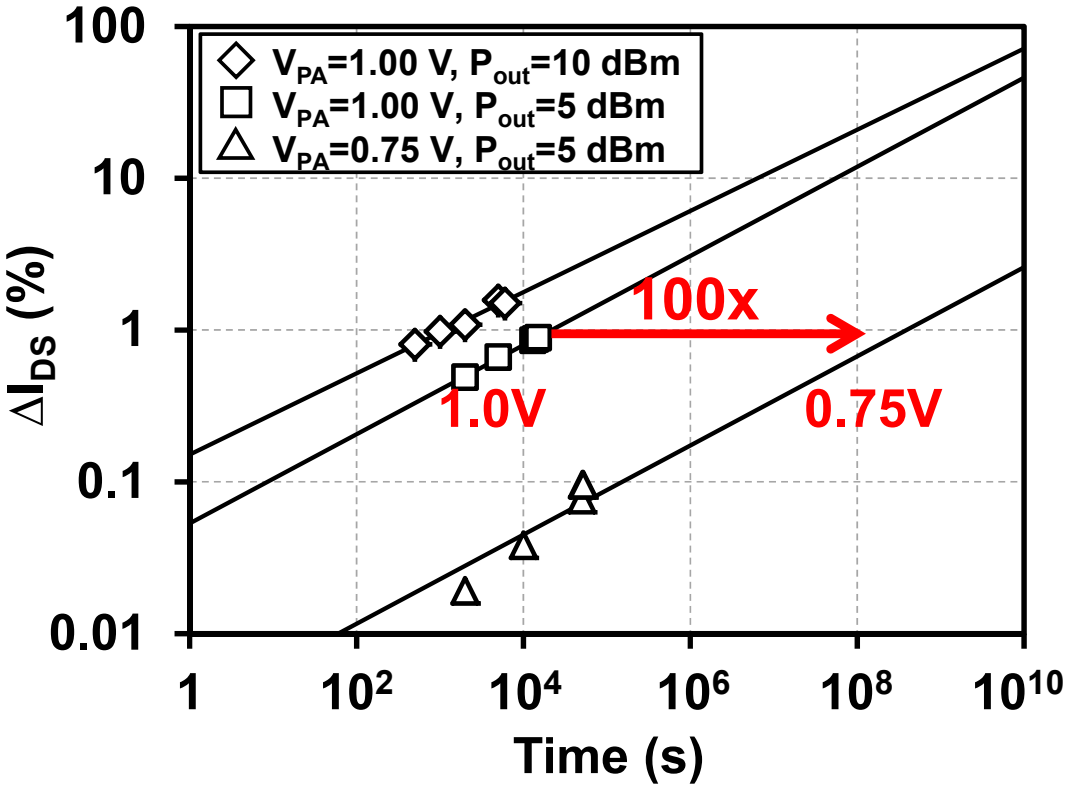




Issue: Hot carrier Injection

Power supply voltage control must be needed to increase the life time



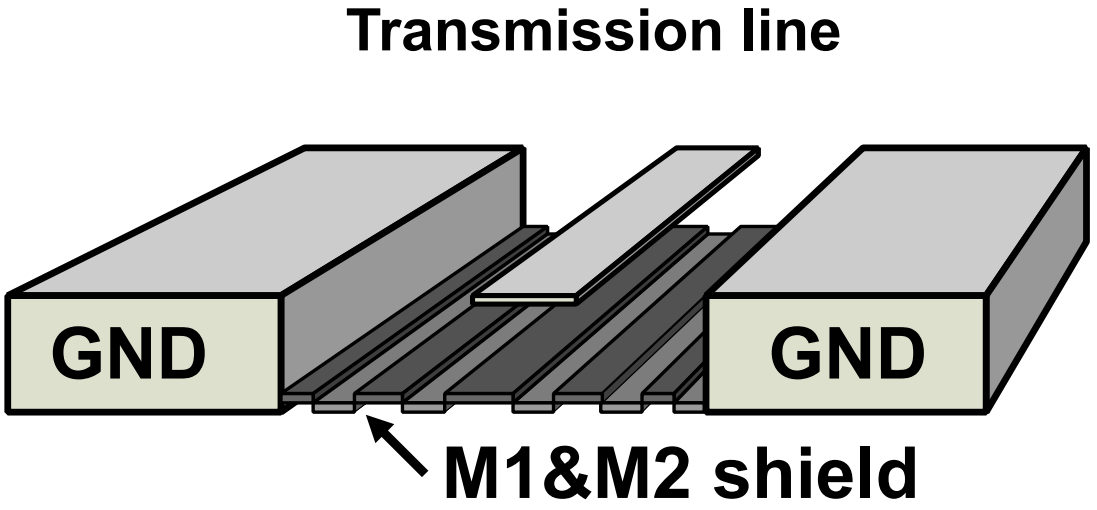


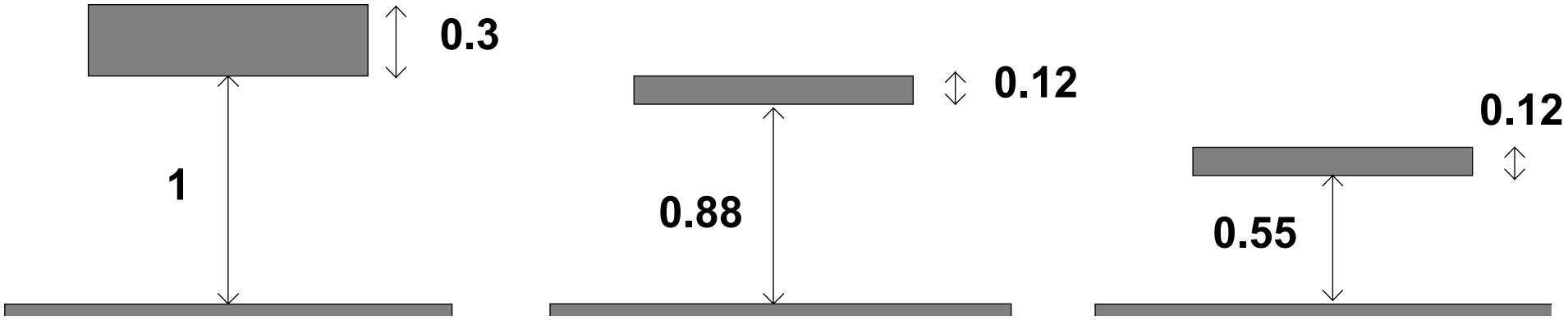
[1] E. Takeda et al., IEDL 1983

Future issue: Loss in transmission line

Reducing the height of the top metal will increase the power loss in the transmission line.

$$\alpha \approx \frac{R}{2Z_o} = \frac{R_u}{2}\sqrt{\frac{C_u}{L_u}} \approx \frac{R_u C_u}{2\sqrt{\varepsilon\mu}}$$





180nm 90nm 40nm

ADC design

ADC performance and the data rate

Data rate is proportional to the product of f_s and N

$$D_{rate} \approx N \cdot f_s$$

If the signal bandwidth is fixed, increase of resolution is required to increase the data rate.

Shannon's theory to determine the communication capacity

$$C = BW \log_2\left(1 + \frac{P_S}{P_N}\right)$$

Higher data-rate can be realized by higher multi-level modulation. It result in increase of ADC resolution.

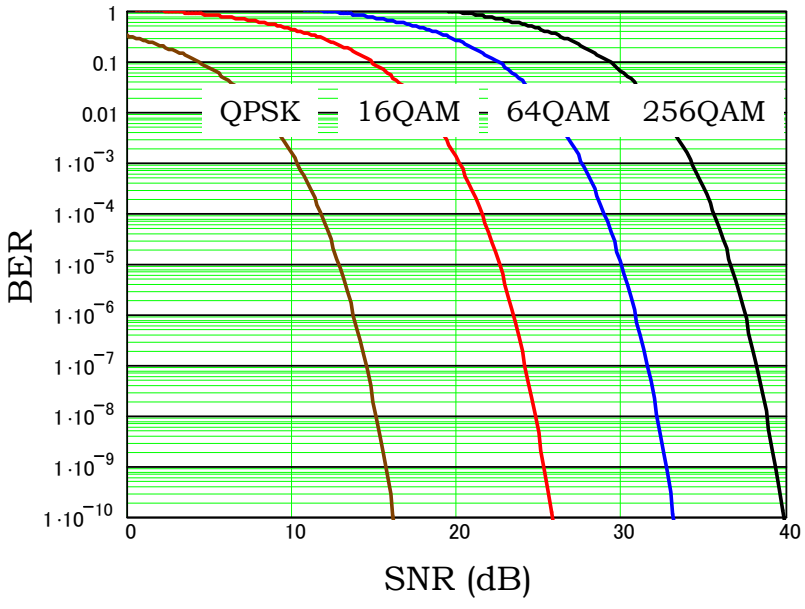
BW and SNR of ADC are

$$BW < \frac{f_s}{2} \qquad \left.\frac{P_S}{P_N}\right|_{ADC} = 1.5 \cdot 2^{2N}$$

Therefore

$$C \approx N f_s$$

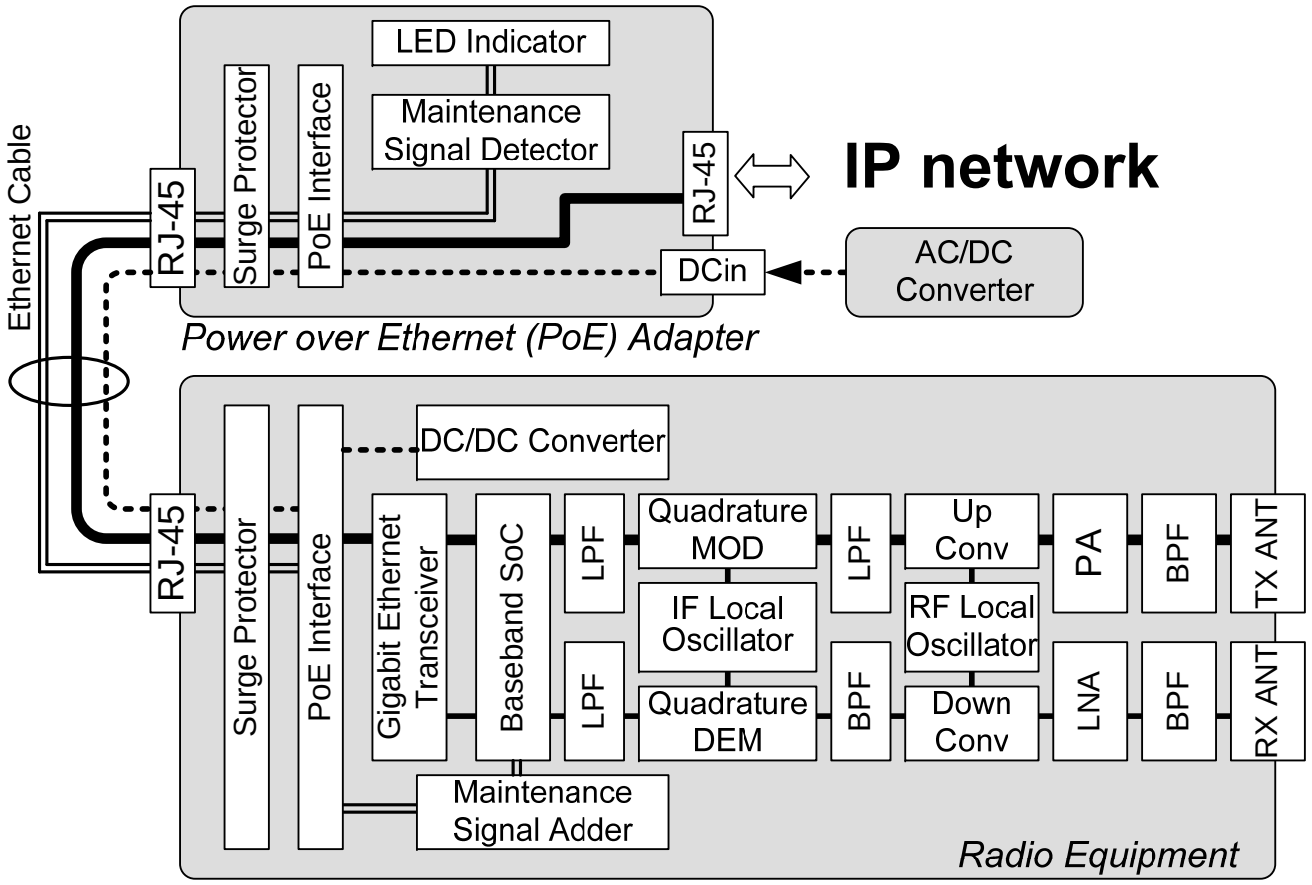
f_s: Sampling frequency
N: Resolution

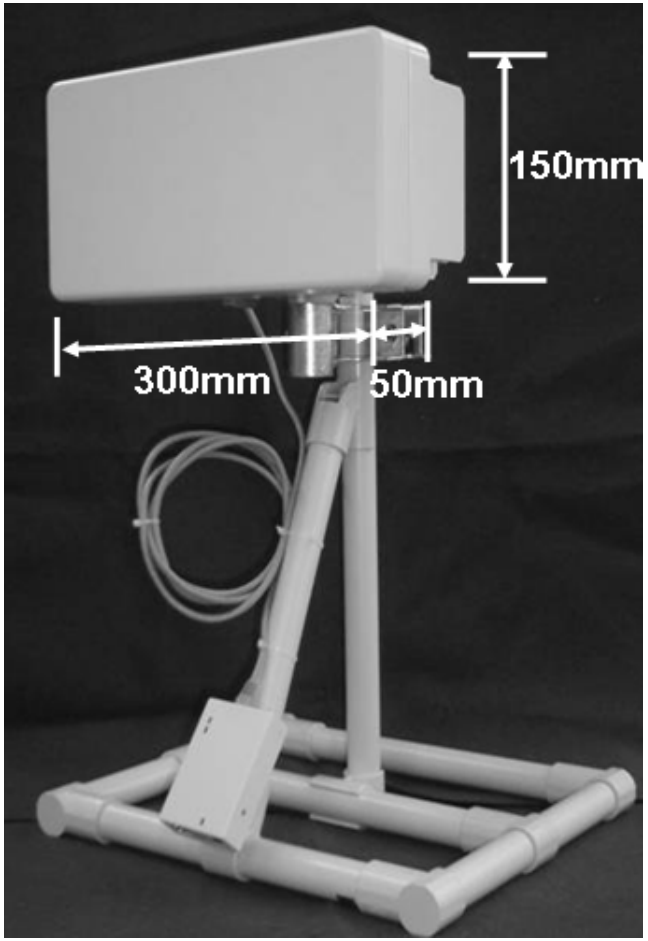


Example: 38GHz 1Gbps fixed point wireless

38GHz 1Gbps fixed point wireless system has been developed.

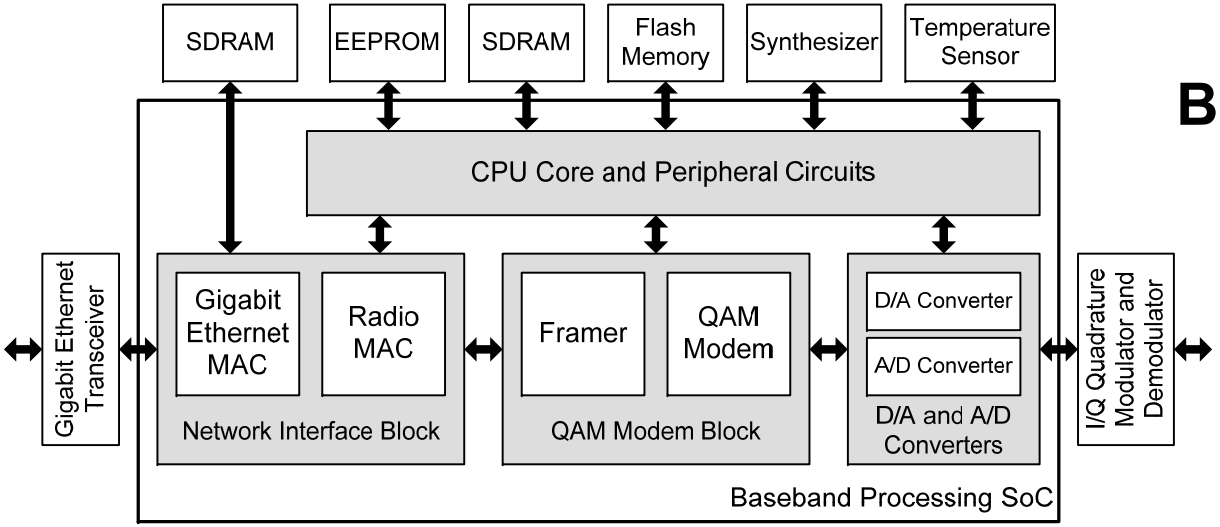
Compatible with Gbit Ethernet
Hole system is integrated with planar antenna





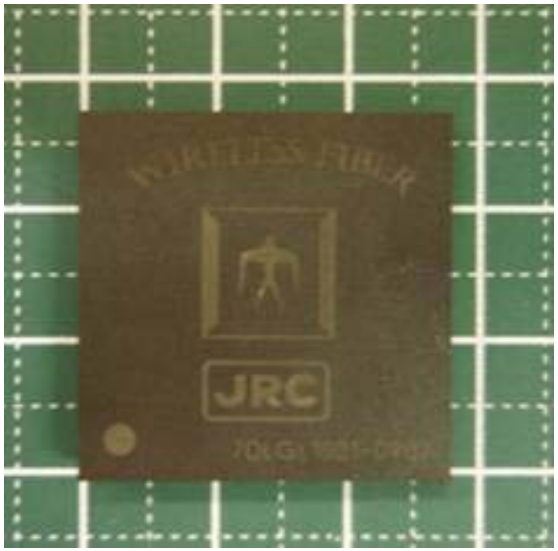
Mixed signal BB SoC

A mixed signal SoC has been developed to realize 64QAM (1Gbps) with BW of 260MHz.

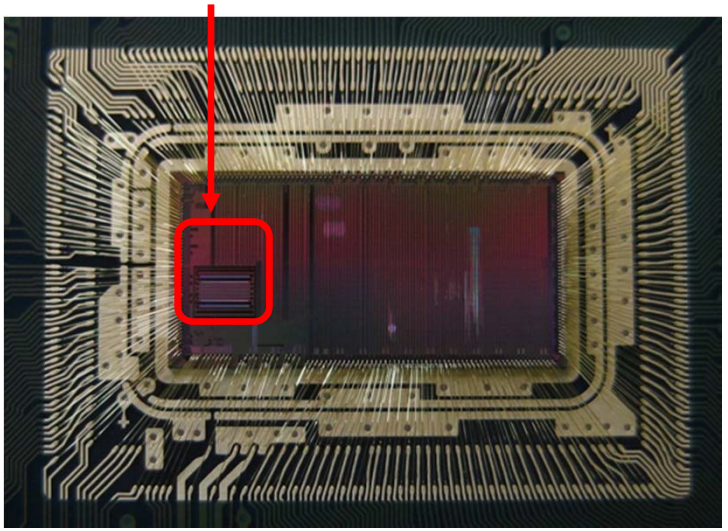


Base band SoC

90nm CMOS
40M Transistors

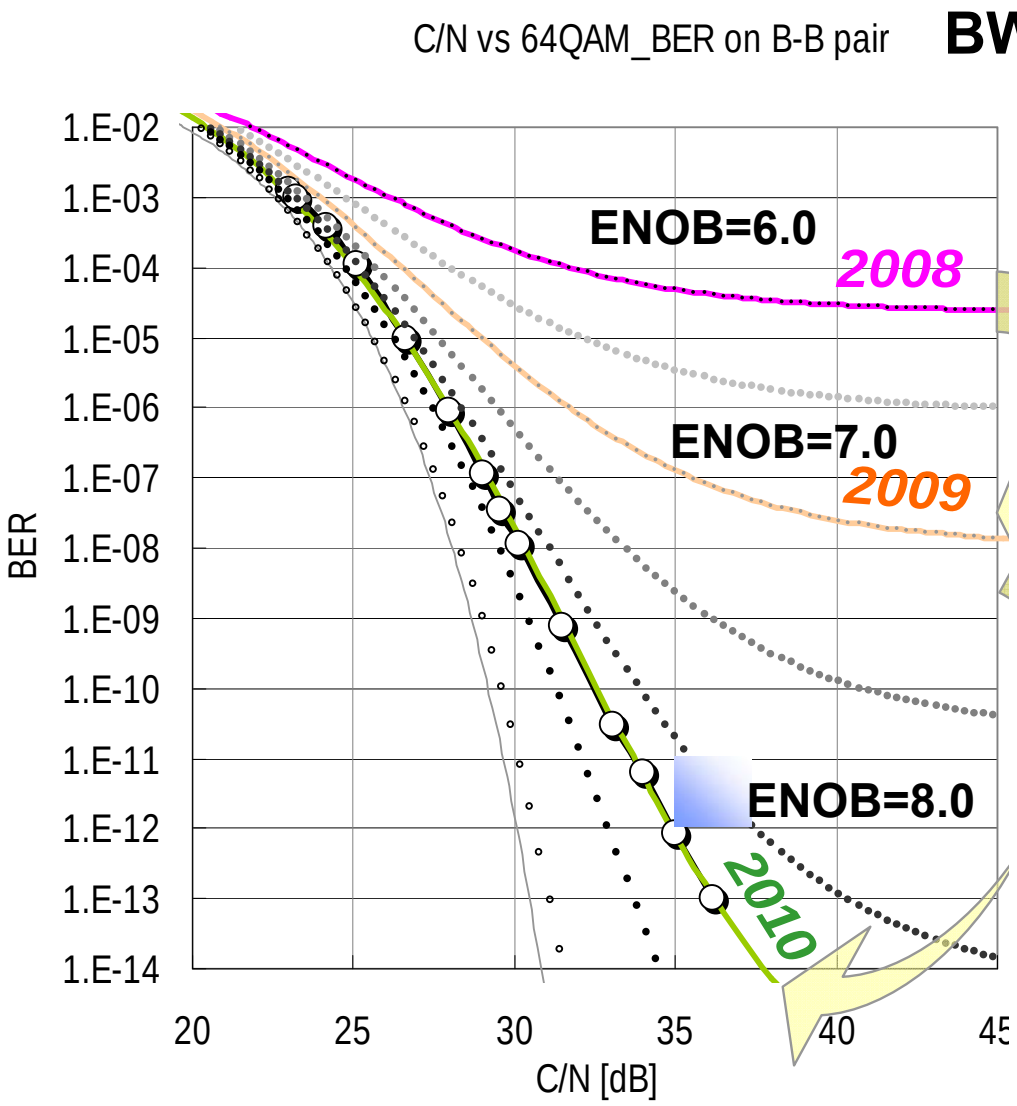


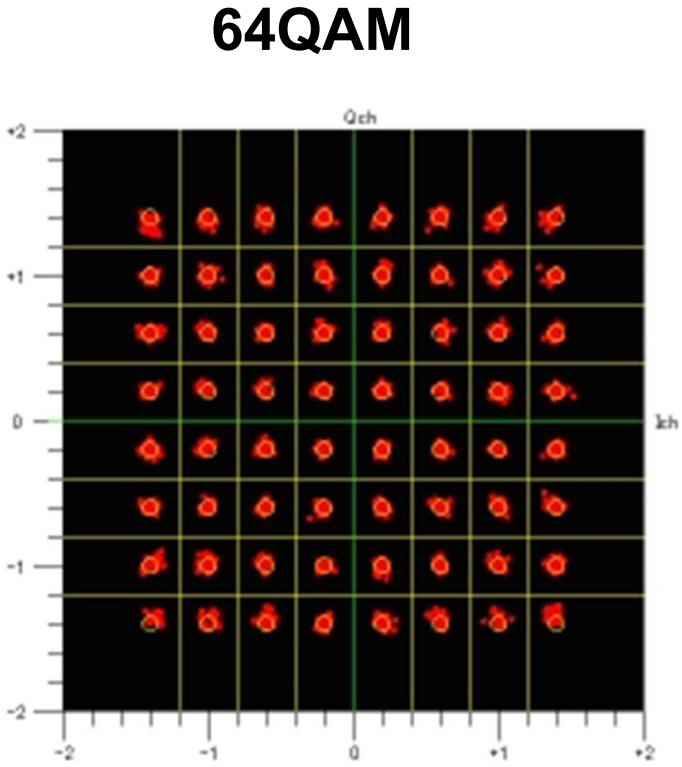
Our lab developed ADC & DAC



ADC performance and BER

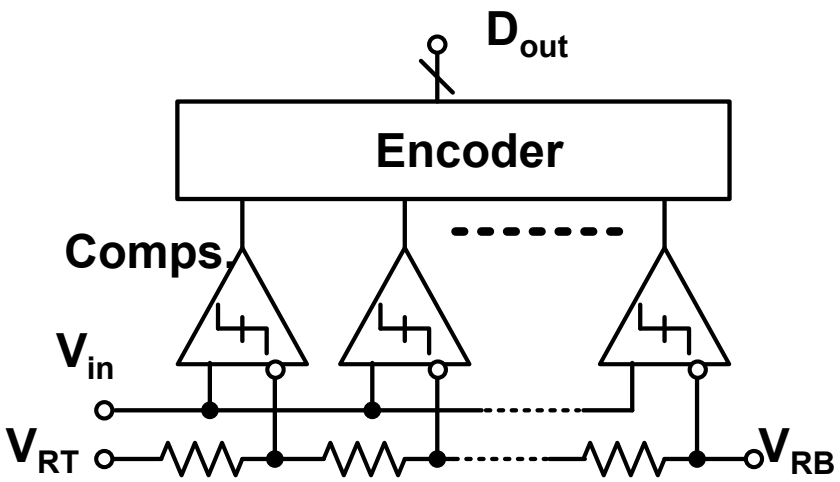
Increase of ADC performance reduces BER of 64 QAM



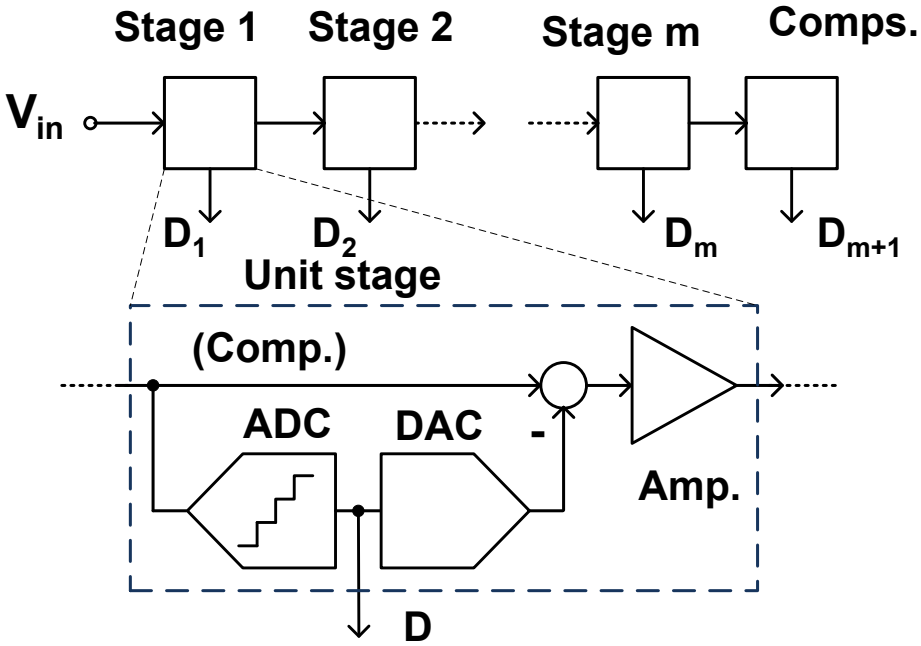


ADC architectures

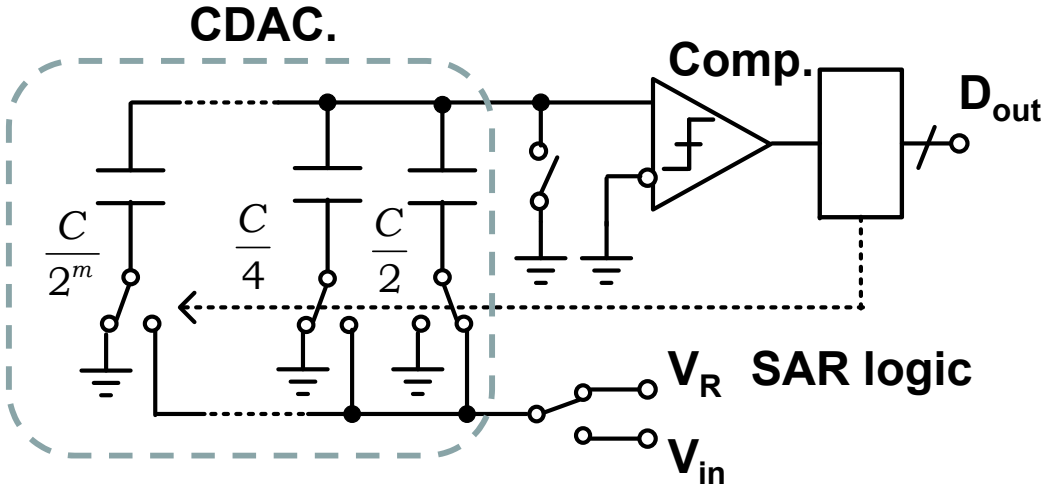
Flash, SAR, pipelined, and sigma-delta are four major ADC architectures



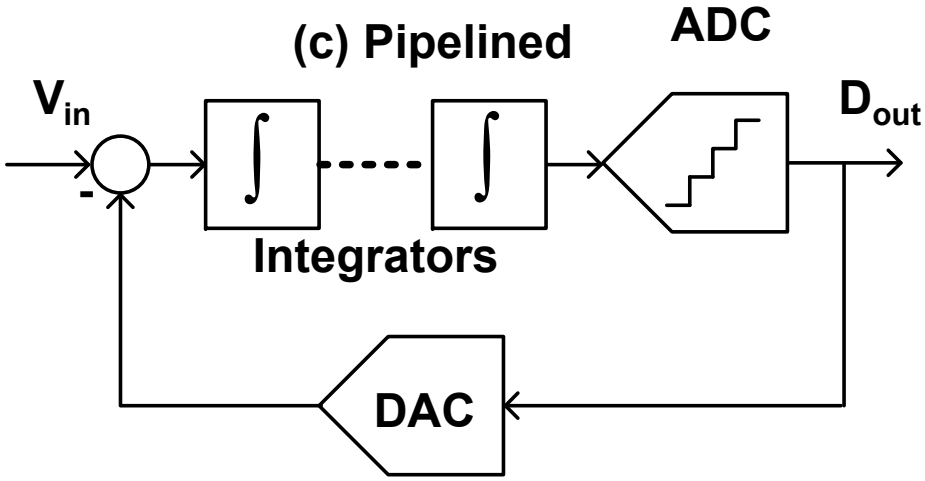
(a) Flash



(c) Pipelined



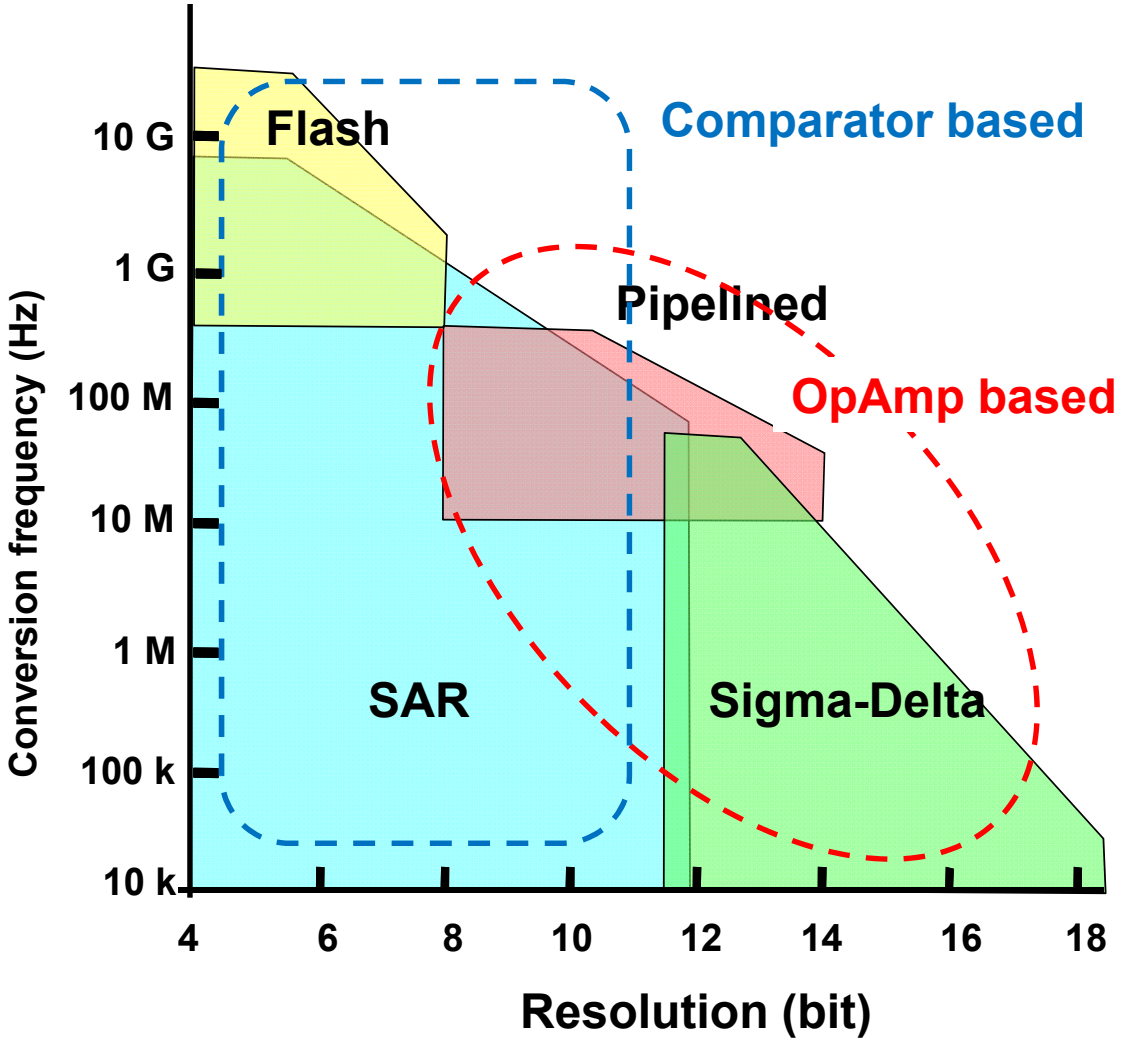
(b) SAR



(d) Sigma-Delta

ADC architecture and covered area

Covered performance area of comparator based ADCs have been increased. However OpAmp based ADCs are still needed for higher resolution.



Comparator based ADC design

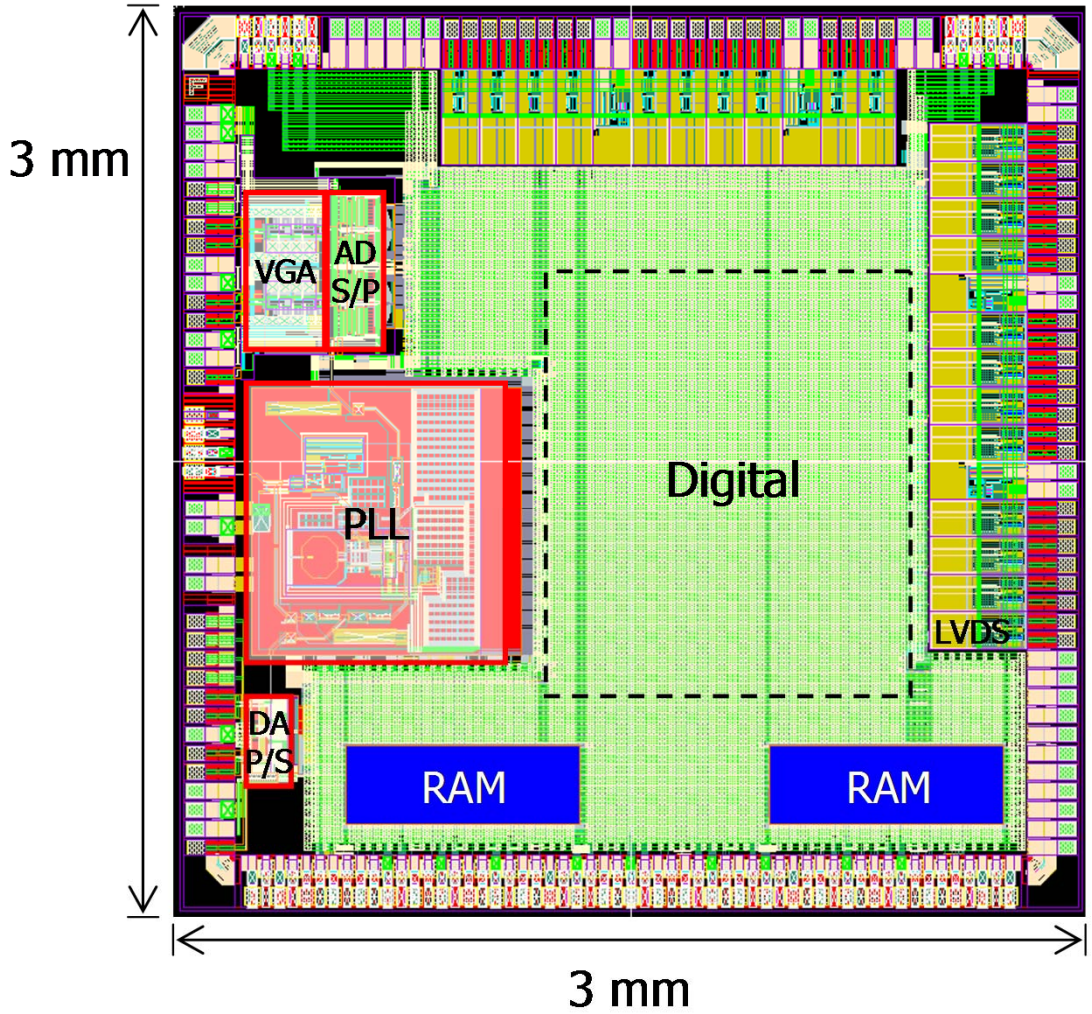
Flash ADC

Developed baseband SoC and flash ADC

Baseband SoC for the 60GHz transceiver has been developed.
ADC, DAC, VGA, and PLL, are integrated in 40nm CMOS.

K. Okada and A. Matsuzawa, et al., ISSCC 2012

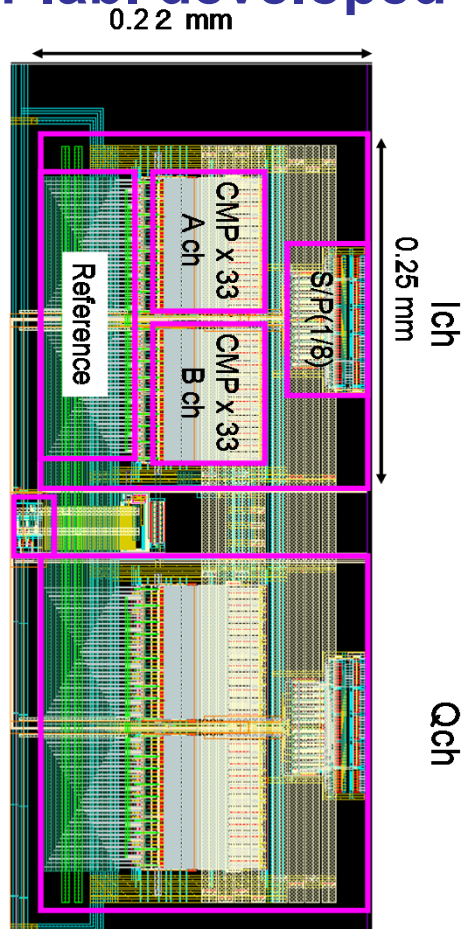
RX: 300mW, TX: 110mW
40nm CMOS technology



M. Miyahara and A. Matsuzawa, et al., RFIC 2012.

ADC 5b, 2.3GSps, 12mW/ch

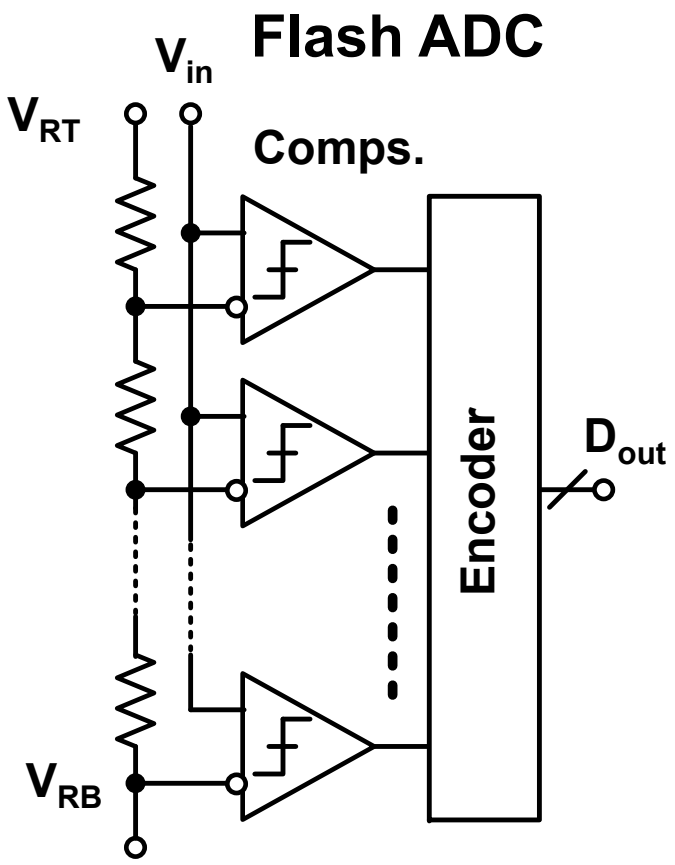
Our lab. developed



Flash ADC

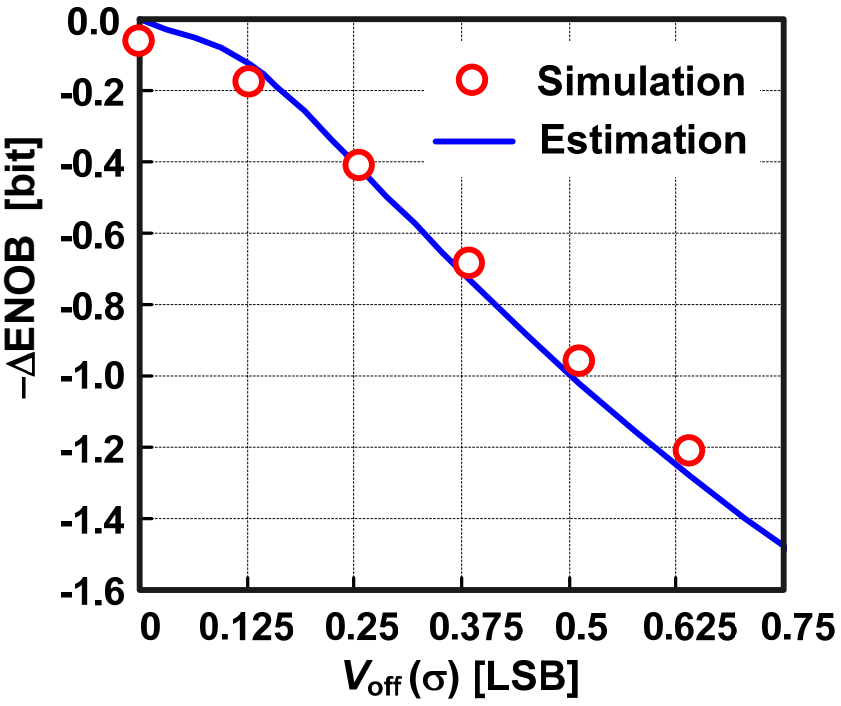
- **Flash ADC is still reasonable for GHz and low resolution conversion.**
- **Comparator determines the ADC performance** $N \leq 6$

Offset mismatch mainly determines the effective resolution.



$$\Delta ENOB = \frac{1}{2}\log_2\left(1 + 12\left(\frac{V_{\text{off}}(\sigma)}{V_q}\right)^2\right)$$

6bit : V_{off}<3mV

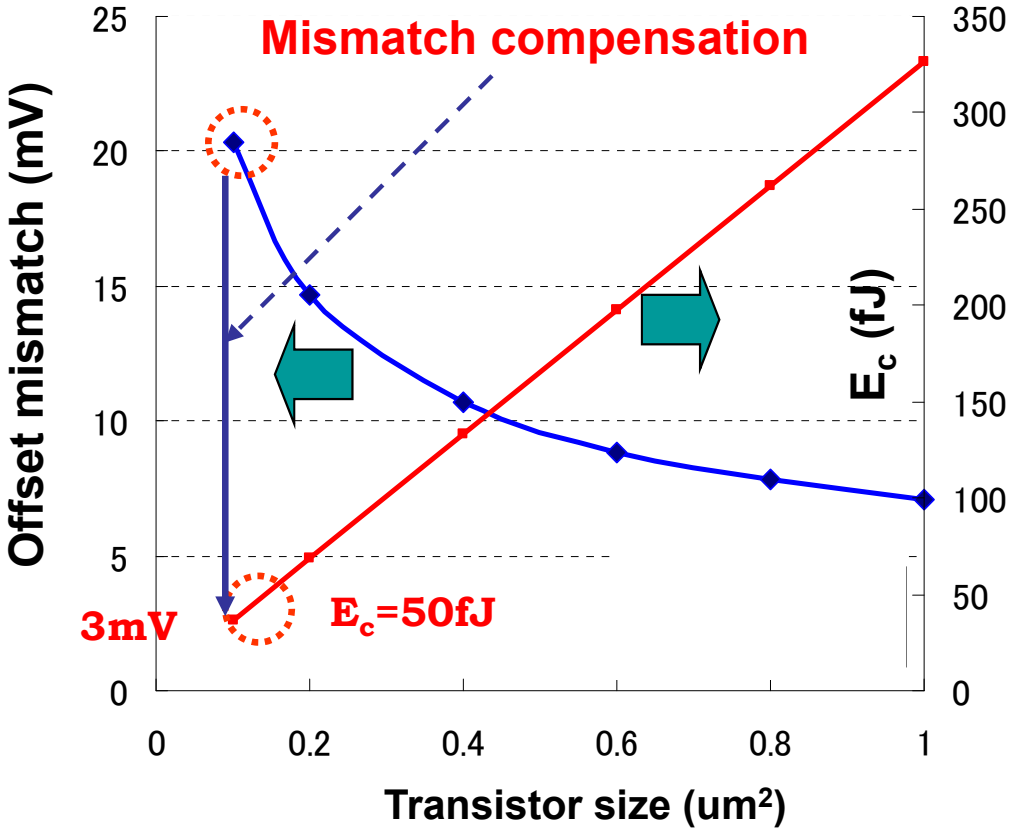


The smaller is the better

Use smaller transistor to reduce energy and compensate mismatch digitally

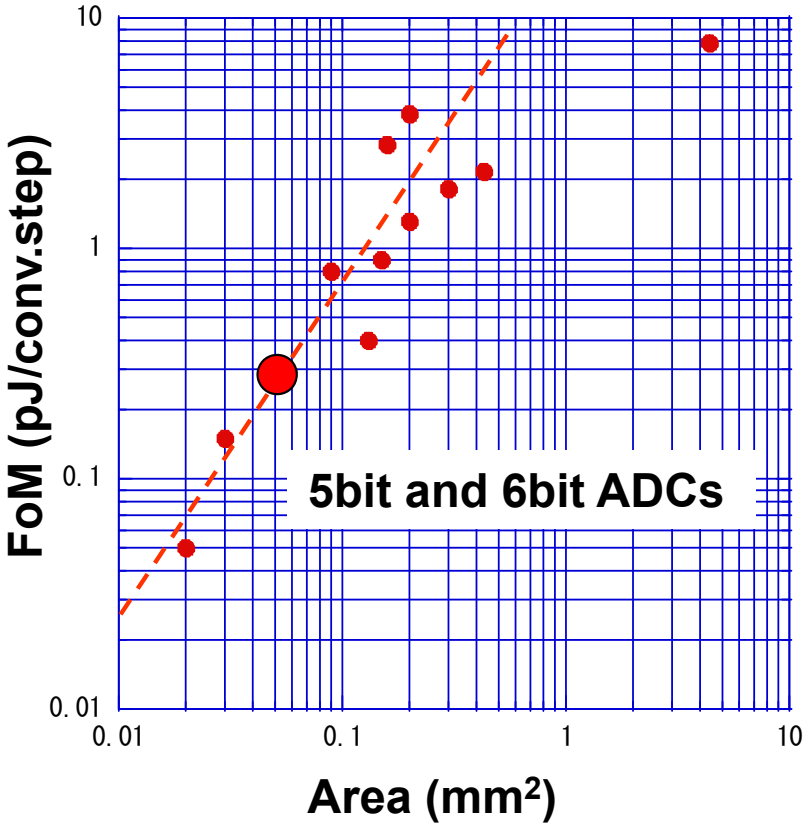
Larger transistor is required to reduce mismatch voltage and results in increase of gate area and consumed energy.

$$V_{\text{offset}}(\sigma) \propto \frac{1}{\sqrt{LW}}$$



Only small ADCs attain low FoM

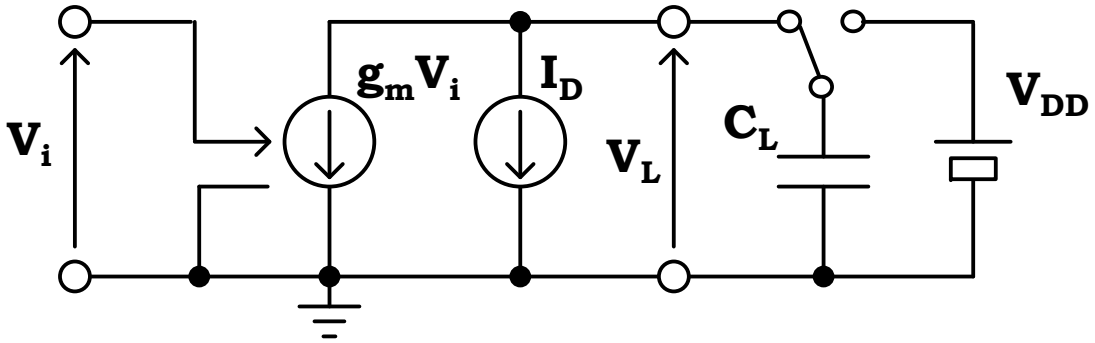
$$E_c \propto C \propto Area$$



Proposed dynamic comparator and offset voltage

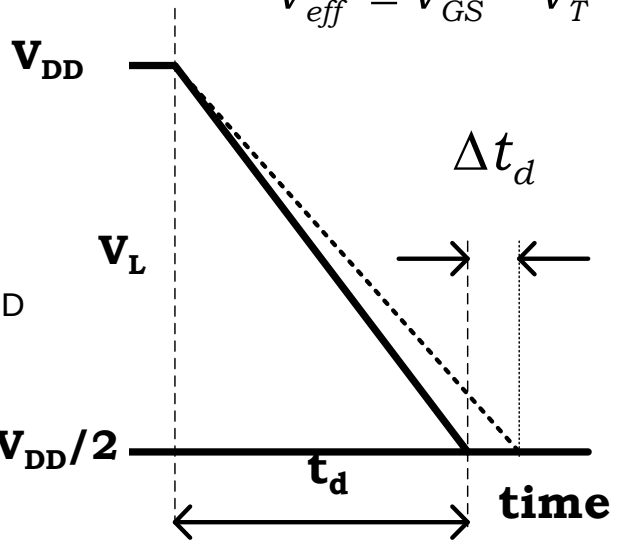
Offset voltage can be corrected by changing the C_L and I_D

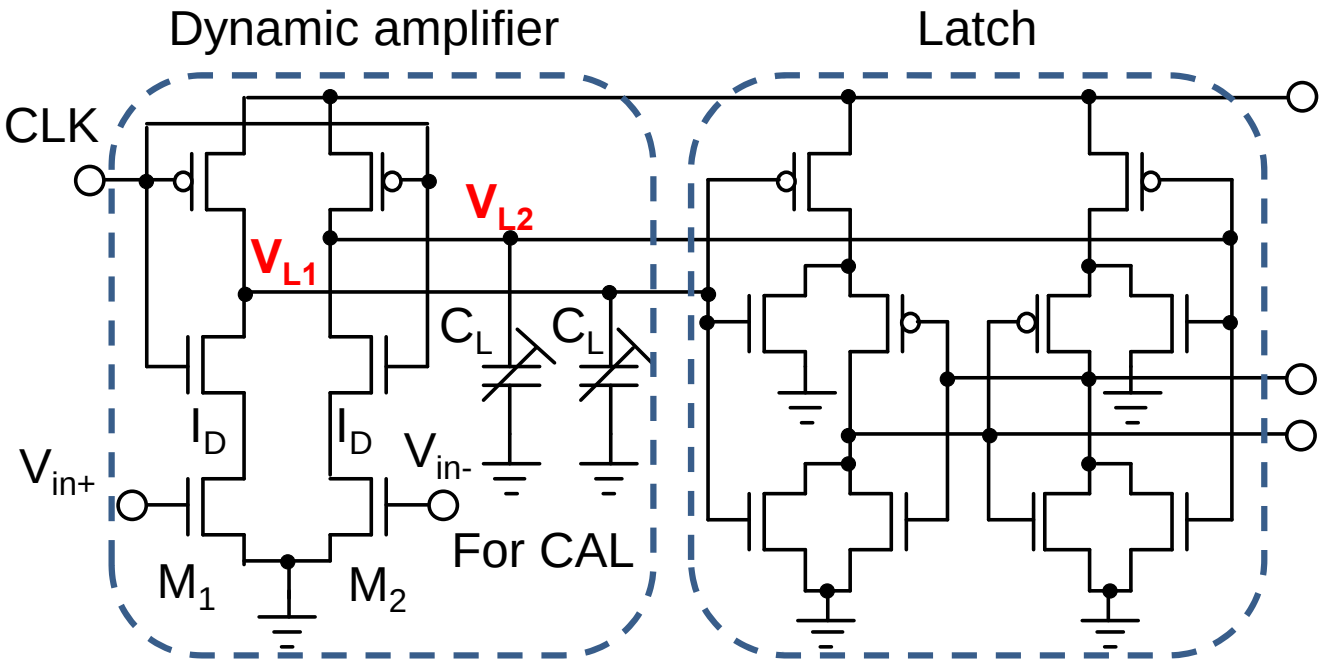
Equivalent circuit for the fist stage



$$\Delta V_i = \frac{V_{eff}}{2}\left(\frac{\Delta C_L}{C_L} - \frac{\Delta I_D}{I_D}\right)$$

$$V_{eff} \equiv V_{GS} - V_T$$

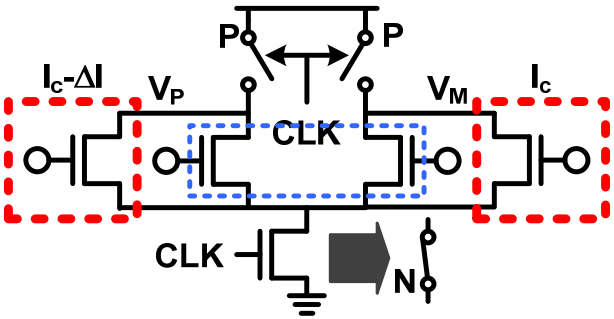




M. Miyahara and A. Matsuzawa, et al., A-SSCC, Nov. 2008.

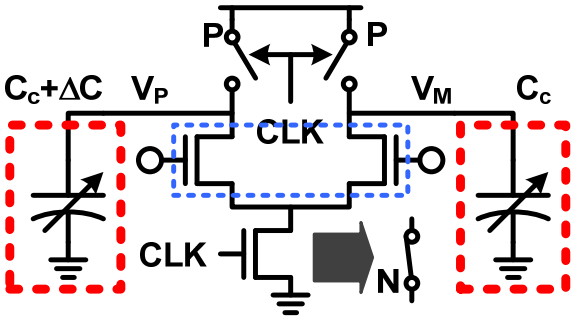
Digital offset mismatch calibration methods

Resistor ladder type

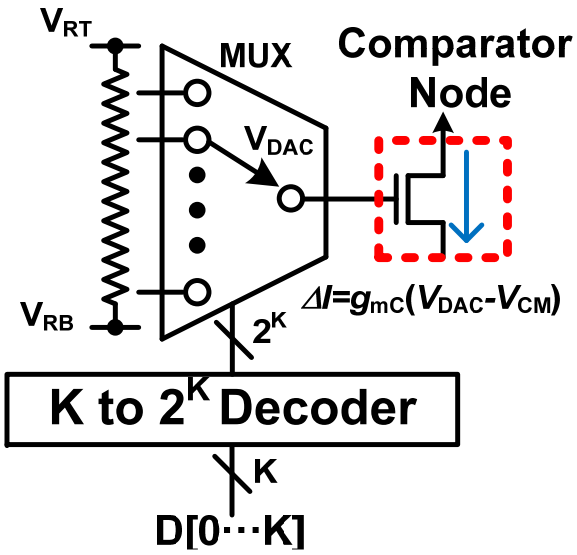


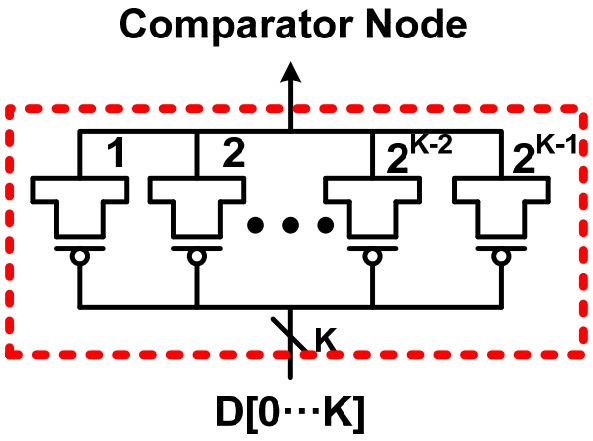
Current calibration

Capacitor array type



Capacitance calibration





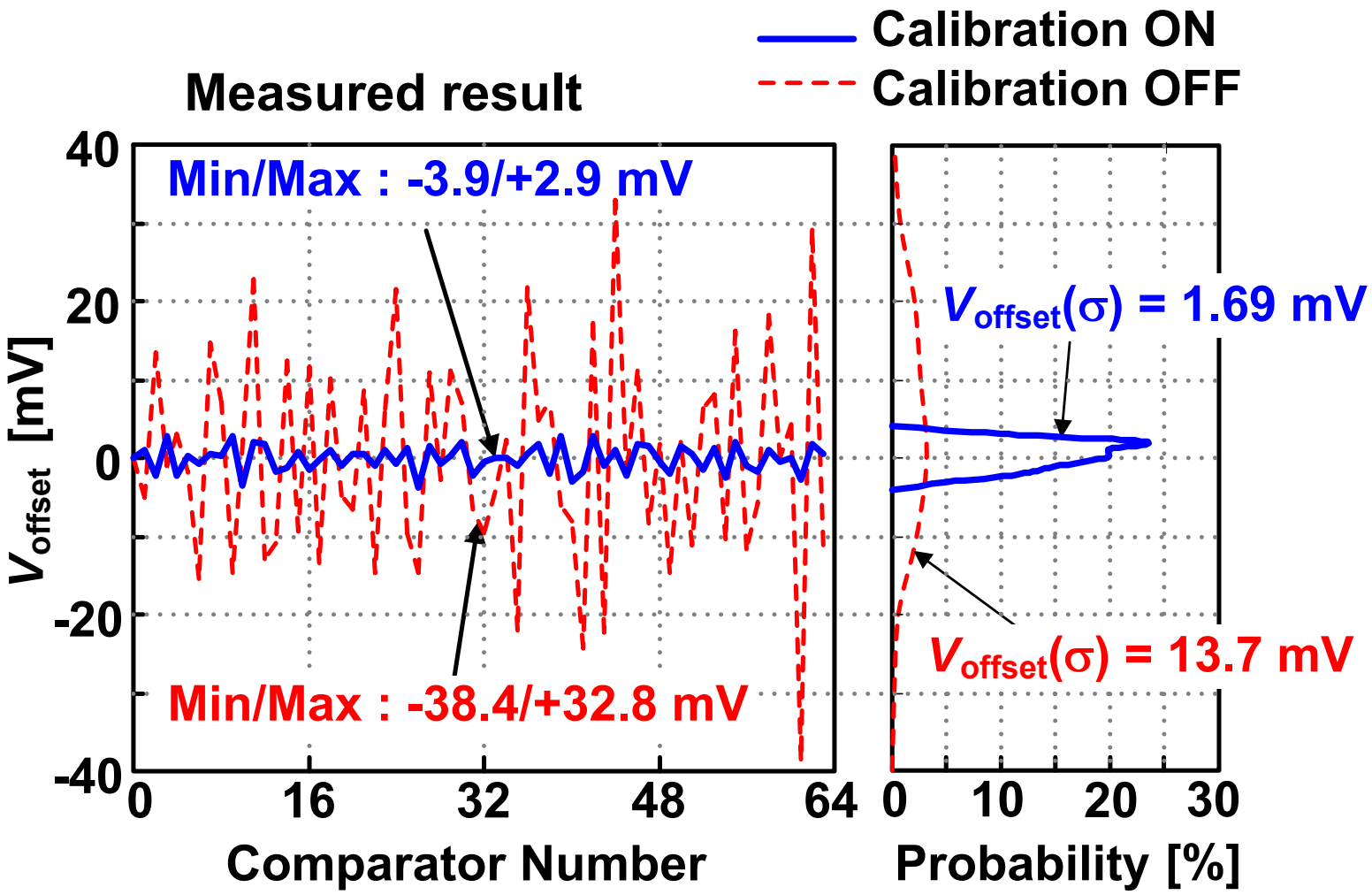
Binary weighted capacitor array

Y. Asada, K. Yoshihara,T. Urano, M. Miyahara and A. Matsuzawa,

"A 6bit, 7mW, 250fJ, 700MS/s Subranging ADC" A-SSCC, pp. 141-144, Nov. 2009.

Effect of digital mismatch compensation

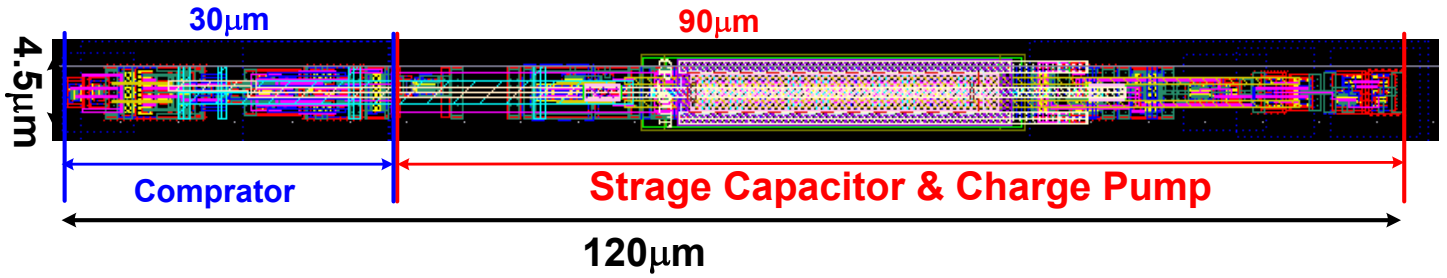
The mismatch voltage can be reduced from 14mV to 1.7mV.

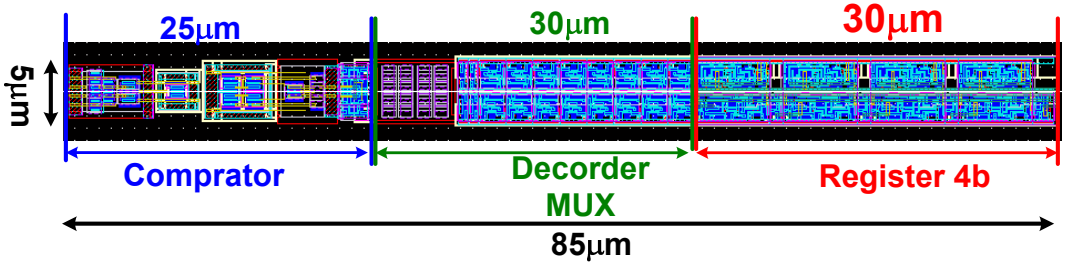


M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," A-SSCC, Nov. 2008.

Area comparison

Penalty area for digital compensation will be reduced with technology scaling.

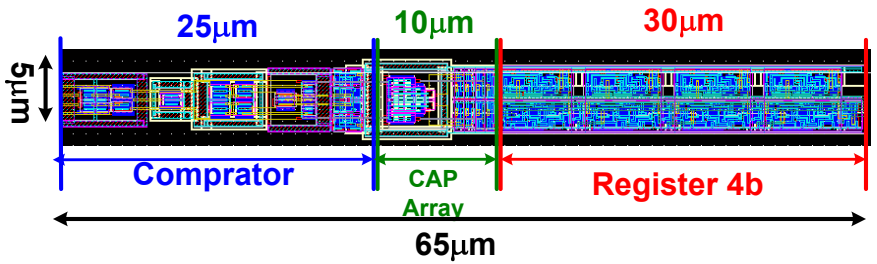




Resistor ladder

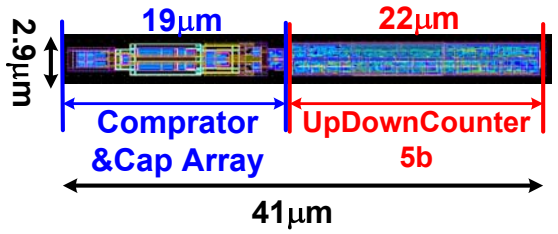
(High speed, but noisy)

90 nm



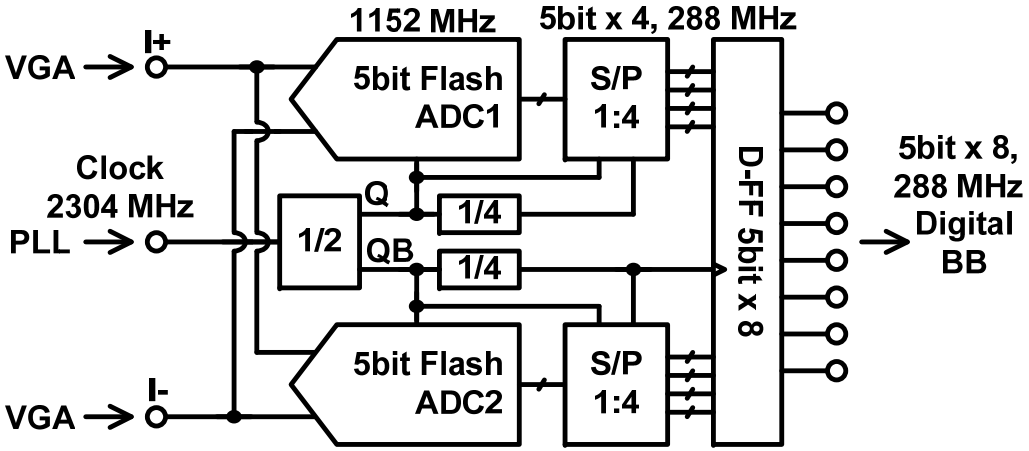
Capacitor array

(Small noise, but moderate speed)

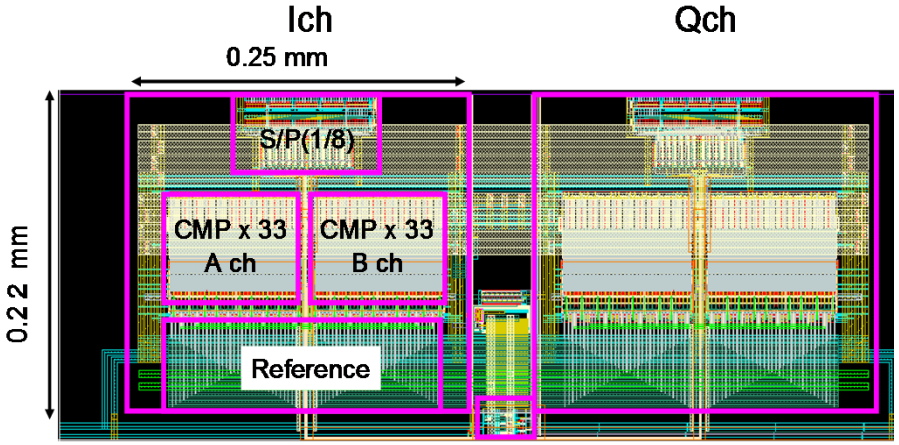


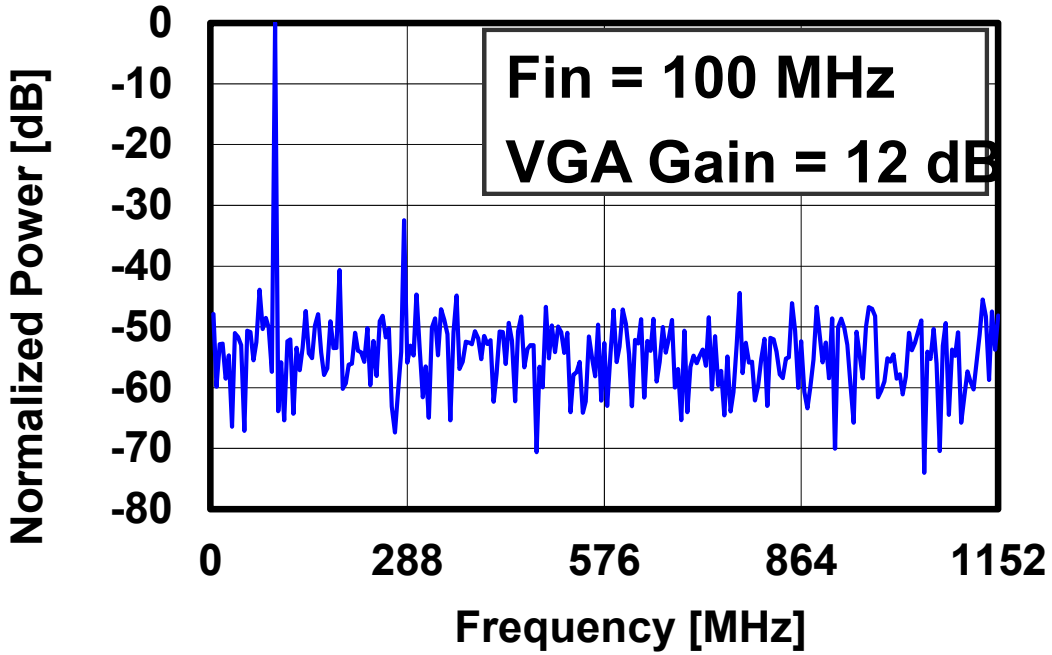
Capacitor array 40 nm

Flash ADC for 60GHz transceiver



M. Miyahara and A. Matsuzawa, et al., RFIC 2012.





VGA Gain range	0-40 dB
ADC Resolution	5 bit
Sampling rate	2304 MS/s
Power Consumption	VGA : 9 mW ADC : 12 mW*
DNL, INL	< 0.8 LSB
SNDR	26.1 dB
FoM of ADC	316 fJ/conv.-s

*single channel inc. S/P

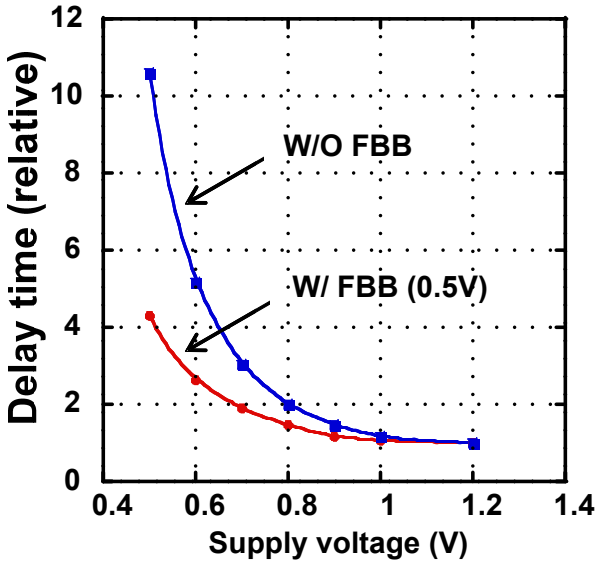
ADC Comparison

Low power & small size ADC has been developed for 60GHz transceiver.

	Architecture	Cal.	fs [GS/s]	SNDR [dB]	Power [mW]	FoM [fJ/-c.s.]	Process [nm]	Area [mm^2]
[1]	Flash	-	3.5	31.2	98	946	90	0.149
[2]	SAR	Internal	2.5	34.0	50	489	45	1
[3]	Folding	Internal	2.7	33.6	50	474	90	0.36
[4]	Pipeline, Folding	External	2.2	31.1	2.6	40	40	0.03
[5]	Flash	Internal	2.88	27.8	36	600	65	0.25
This work	**Flash**	**Internal**	**2.3**	**26.1**	**12**	**316**	**40**	**0.06**

[1] K. Deguchi, *et al*., *VLSI Circuits* 2007 [2] E. Alpman, *et al*., *ISSCC* 2009
[3] Y. Nakajima, *et al*., *VLSI Circuits* 2007 [4] B. Verbruggen, *et al*., *ISSCC* 2010
[5] T. Ito, *et al*., *A-SSCC* 2010

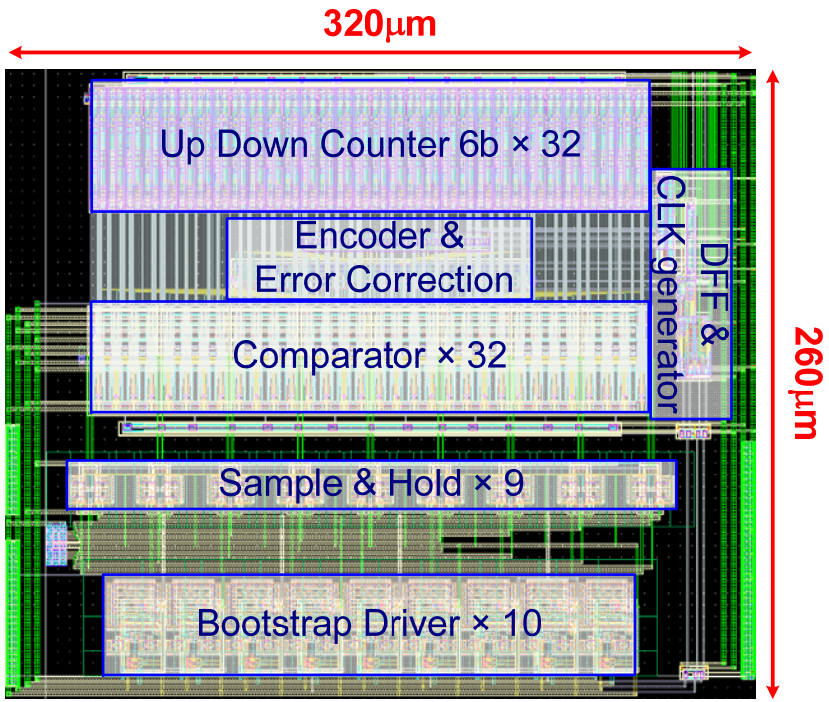
0.5V Flash ADC



5bit 0.5V 600MSps Flash ADC has been developed.

S/H circuits use gate boosted switches.

Forward body bias is used to decrease gate delay.



M. Miyahara , J. Lin, K. Yoshihara, and A. Matsuzawa,
"A 0.5 V, 1.2mW, 160fJ, 600 MS/s 5 bit Flash ADC"
A-SSCC, pp. 177-180, Nov. 2010.

Reference #	[7]	[8]	[9]	[10]	This work
Resolution (bit)	5	5	5	5	**5**
fs (GS/s)	0.5	1.75	1.75	0.06	**0.6**
SNDR (dB)	26	30	30	26	**27**
Pd (mW)	5.9	2.2	7.6	1.3	**1.2**
Active area (mm^2)	0.87	0.017	0.03	-	**0.083**
Vdd (V)	1.2	1	1	0.6	**0.5**
FoM(fJ)	750	50	150	1060	**160**
CMOS Tech. (nm)	65	90	90	90	**90**
Architecture	SAR	Fold+Flash	Flash	Flash	**Flash**

FoM_{Fmax} = 160fJ @ 600MSps
FoM_{Best} = 110 fJ @ 360MSps

[7] B. P. Ginsburg, J. Solid-State Circuits 2007.
[8] B. Verbruggen, ISSCC 2008.
[9] B. Verbruggen, VLSI Circuits 2008.
[10] J. E. Proesel, CICC 2008.

Comparator based ADC design

: SAR ADC

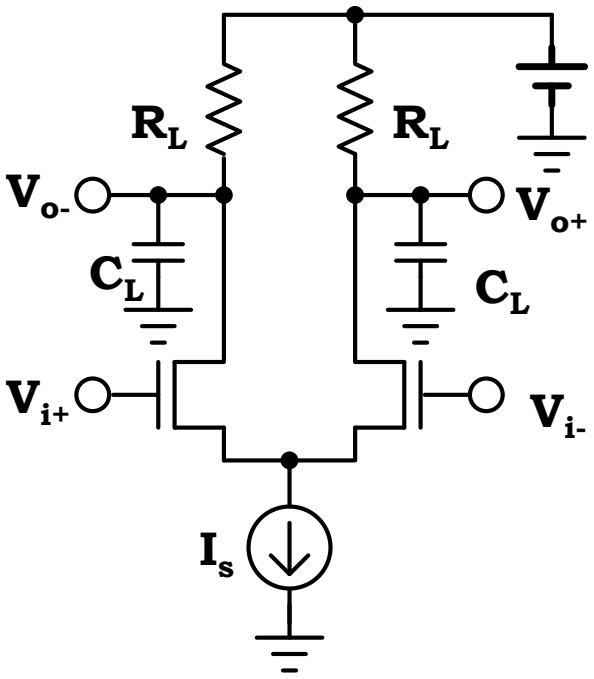
Basic idea for low energy analog design

Conventional analog circuit consumes larger energy.

Dynamic circuits doesn't consume larger energy.

CMOS: Consumed energy is independent of the delay time.

CML, OpAmp

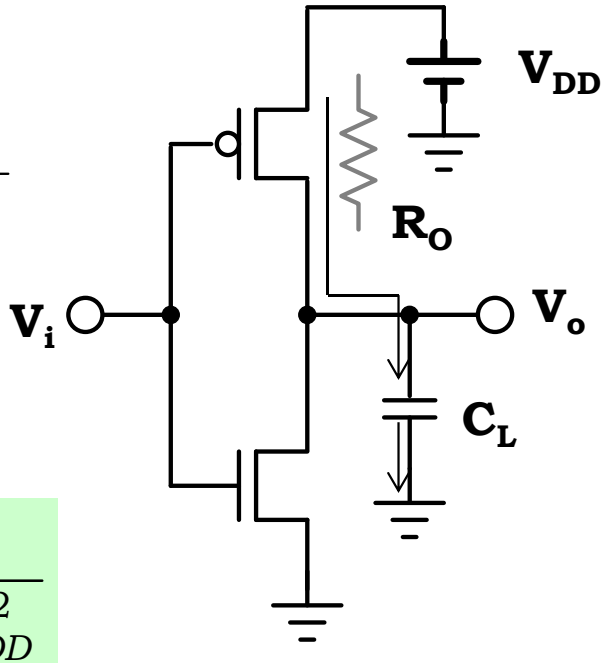


$$f_{togle} \propto \frac{I_s}{V_{DD} C_L}$$

$$P_d = V_{DD} I_s$$

$$f_{togle} \propto \frac{P_d}{C_L V_{DD}^2}$$

CMOS



$$f_{togle} \propto \frac{1}{T_r} \propto \frac{1}{R_o C_L}$$

$$P_d = f E_d = \frac{1}{2} f C_L V_{DD}^2$$

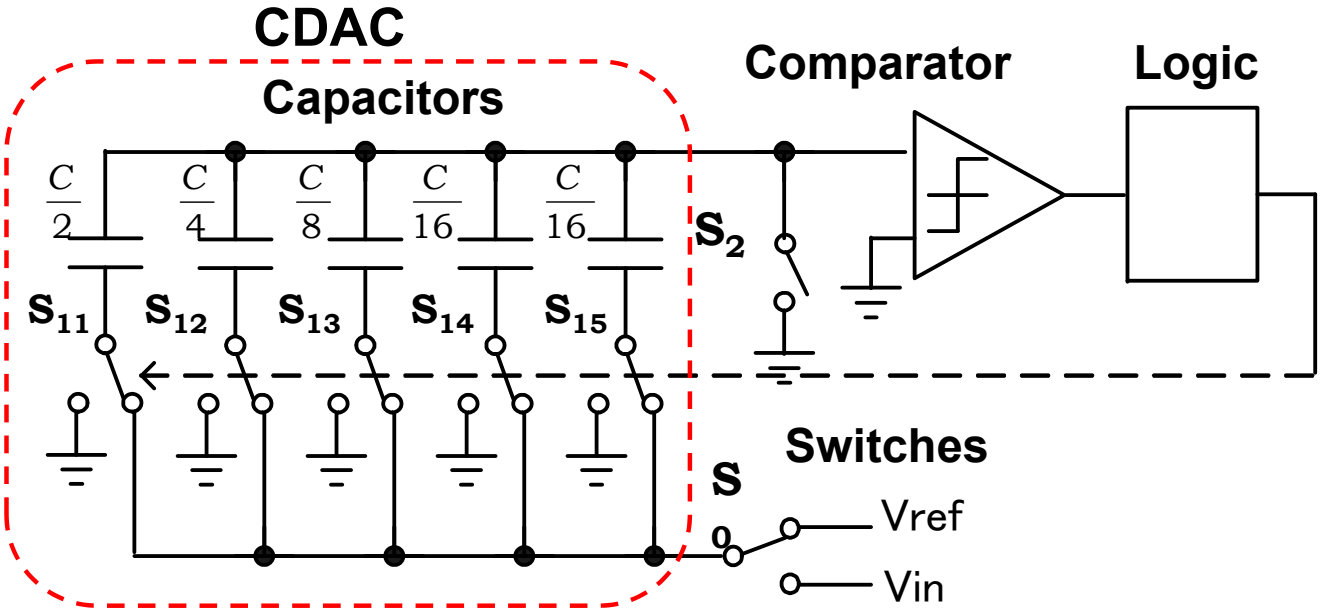
$$E_d = \frac{1}{2} C_L V_{DD}^2$$

$$f_{togle} \propto \frac{1}{R_o C_L}$$

SAR ADC

SAR can be designed to consume no static power.

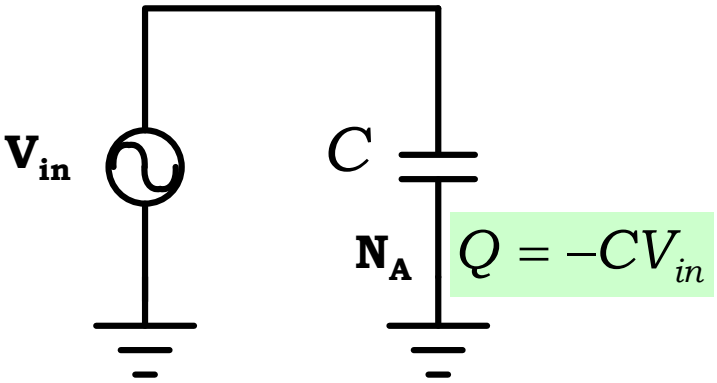
SAR can realize larger signal swing compared with pipeline ADC.



Not OpAmp based, but comparator based

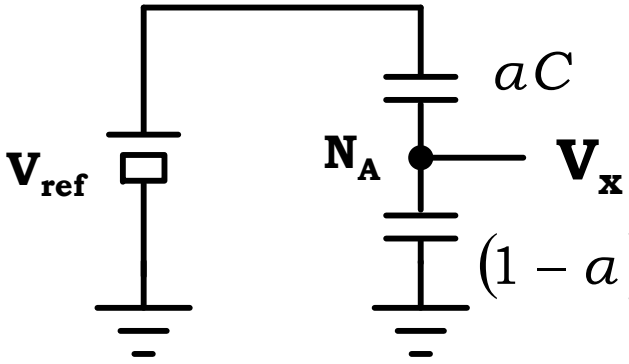
No resistors
No static current !
Potentially full swing

Sample



$Q = -CV_{in}$

Generating subtracted signal



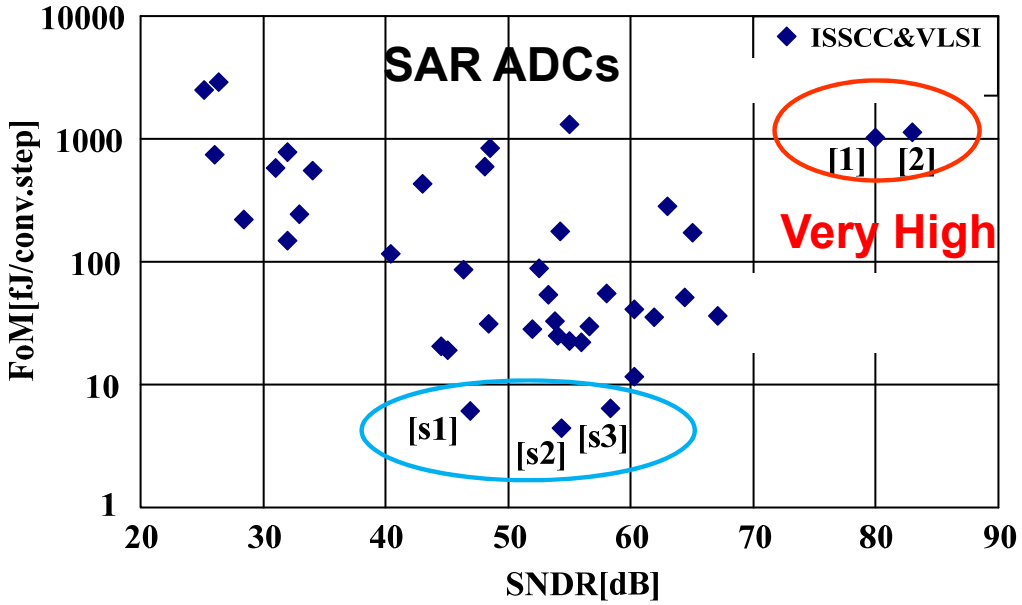
$$E \approx \frac{1}{2} C V_{ref}^2$$

$$V_x = -\left(V_{sig} - a \cdot V_{ref}\right)$$

$0 < a < 1$

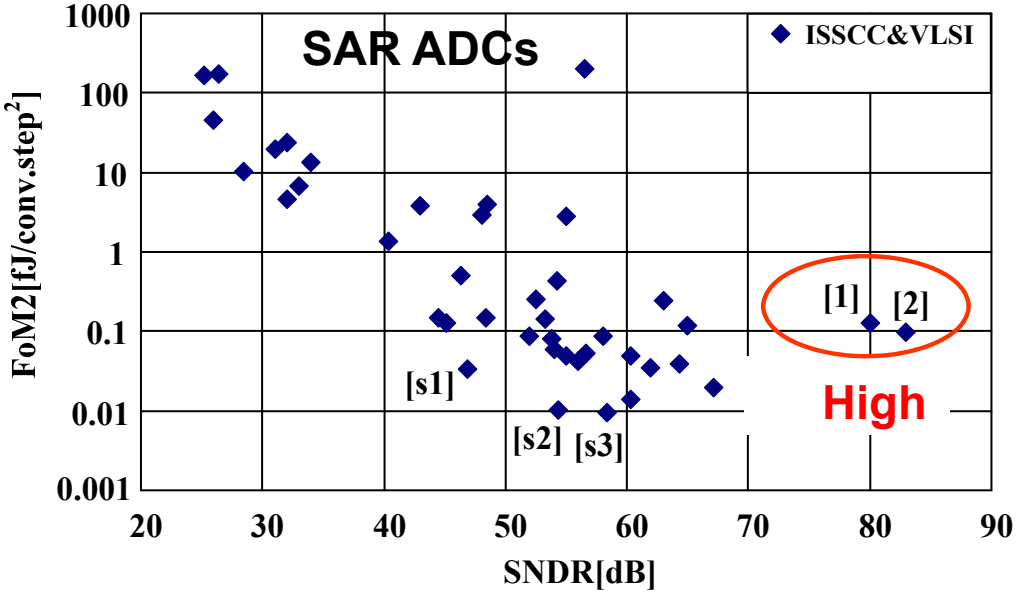
FoM and FoM2

High SNDR over 70dB and low FoM of less than 50fJ looks not easy.



FoM LT. 10fJ is possible, however its SNDR is < 60dB

Low FoM, if SNDR is > 70dB is not easy.



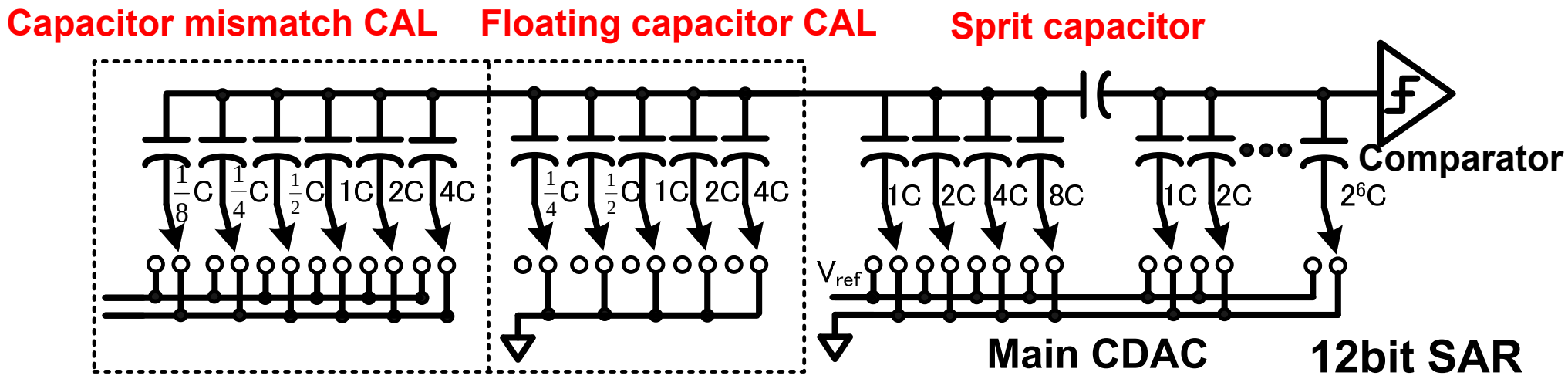
FoM2 is supported by theory and show the energy trend more clearly.

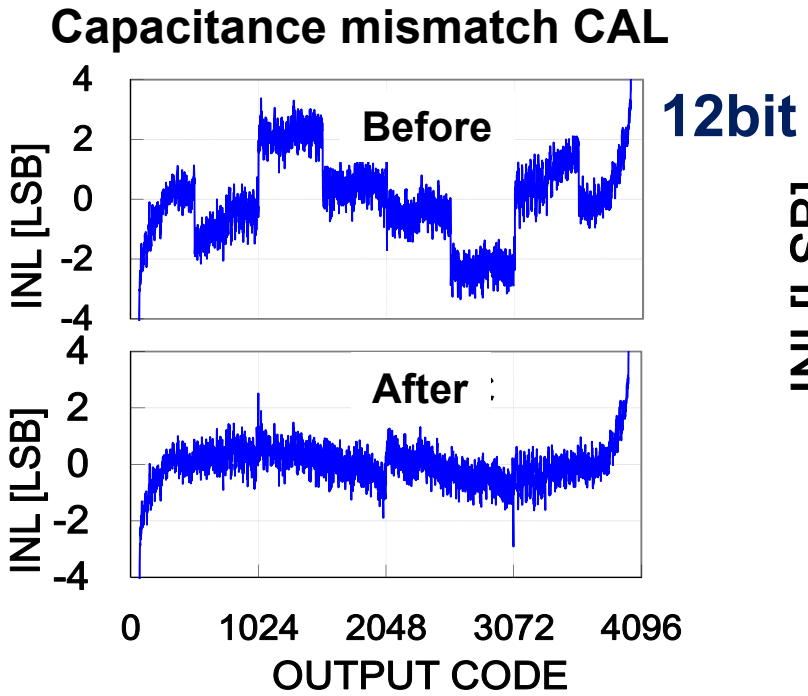
$$FoM = \frac{P}{2^{(SNDR-1.76)/6.02} \cdot Fs}$$

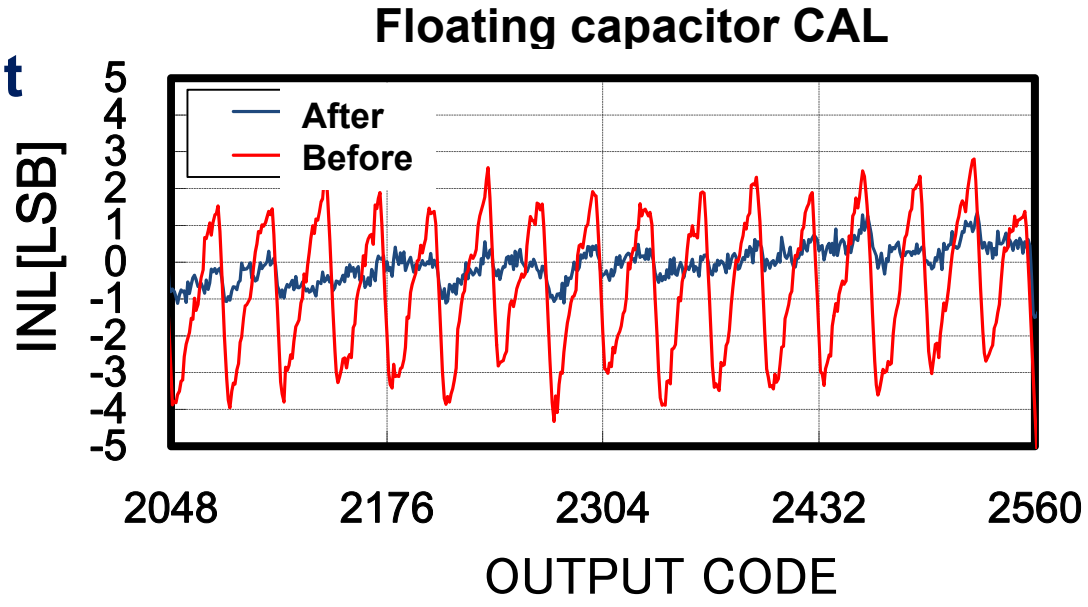
$$FoM2 = \frac{P}{2^{2\cdot(SNDR-1.76)/6.02} \cdot Fs}$$

Linearity of SAR ADC

Non-linearity is caused by CDAC, and it can be calibrated digitally. Therefore, a small capacitance determined by noise can be used.

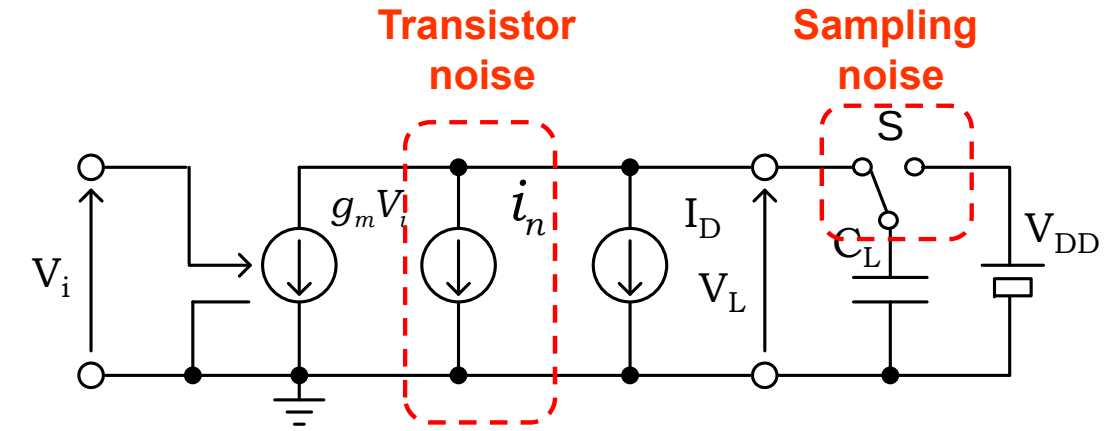






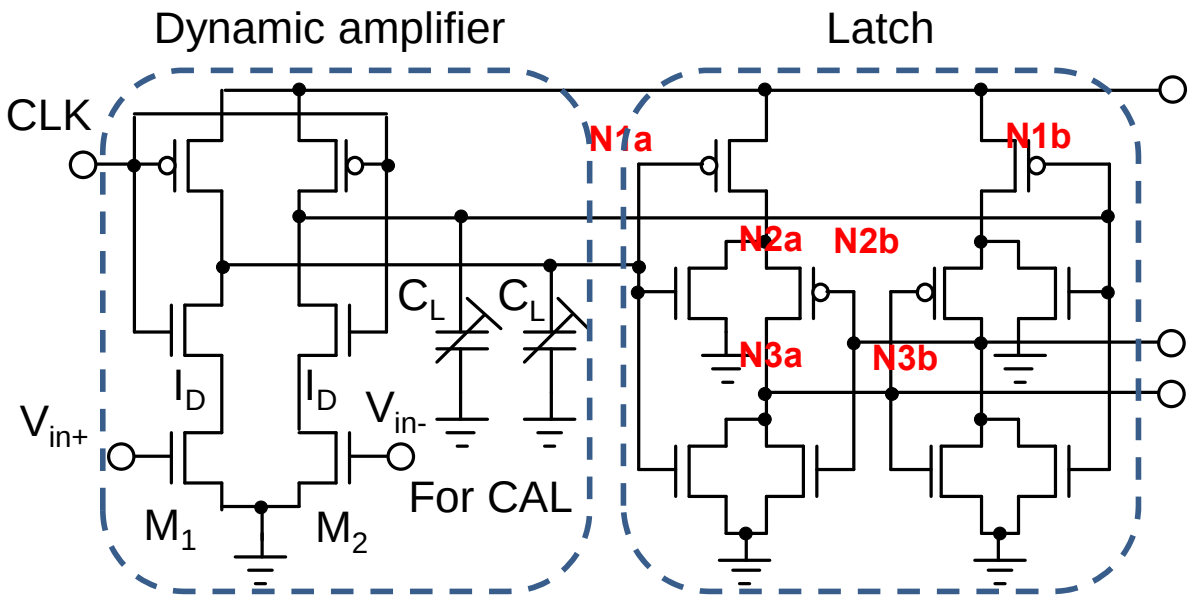
Noise of dynamic comparator

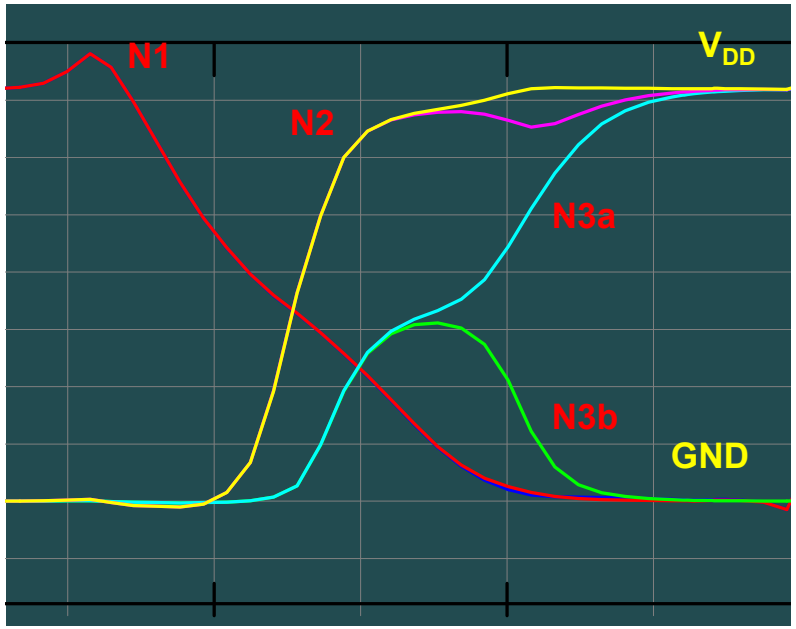
Basic noise of the dynamic comparator is determined by load capacitor



Obtained noise equation

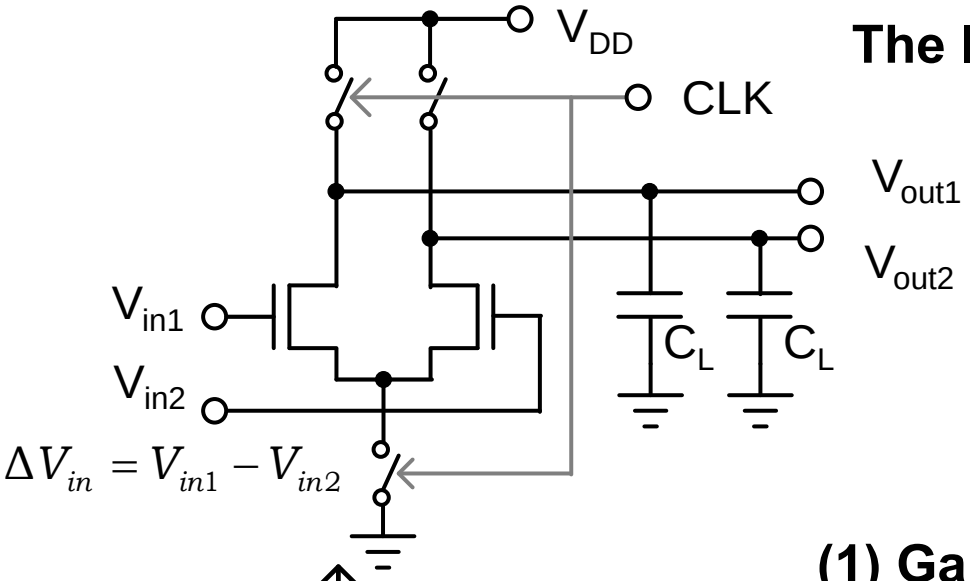
$$\delta V_{in}^2 = \frac{kTV_{eff}^2}{C_L V_{dd}^2}\left(2\gamma\frac{V_{dd}}{V_{eff}}+1\right)$$

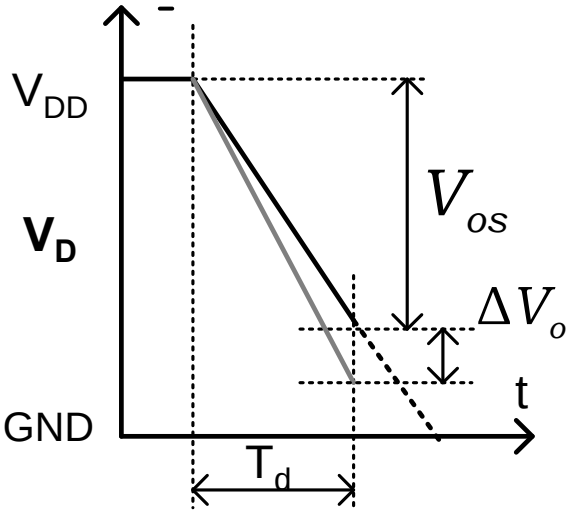


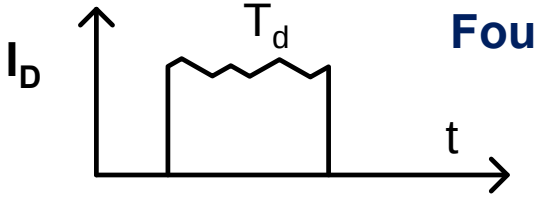


A. Matsuzawa," IEEE 8th International Conference on ASIC(ASICON), pp. 218-221, Oct. 2009.

Gain and noise of the dynamic amplifier



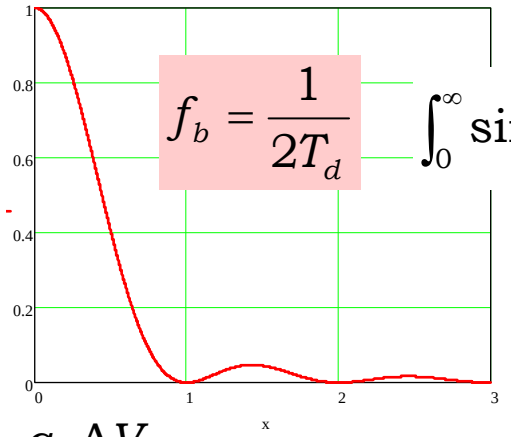




Fourier

The larger gain requires the larger voltage swing

$$\sin c^2(x)$$



$$f_b = \frac{1}{2T_d} \qquad \int_0^\infty \sin c^2(x)dx = \frac{1}{2}$$

$$x = f \cdot T_d$$

(1) Gain $\Delta V_o = -\frac{g_m \Delta V_{in}}{C_L} T_d$

$$G = -\frac{g_m}{I_D} V_{os} \approx -\frac{2V_{os}}{V_{eff}} \qquad T_d = \frac{V_{os} C_L}{I_D}$$

(2) Noise

$$\overline{i_{n0}^2} = \int_0^\infty \left(\frac{i_{no}^2}{Hz}\right) |H(f)|^2 df = \frac{i_{no}^2}{Hz} \int_0^\infty T_d^2 \sin c^2(fT_d) df$$

$$= \frac{i_{no}^2}{Hz} \frac{T_d^2}{T_d} \int_0^\infty \sin c^2(x)dx = \frac{i_{no}^2}{Hz} \frac{T_d}{2}$$

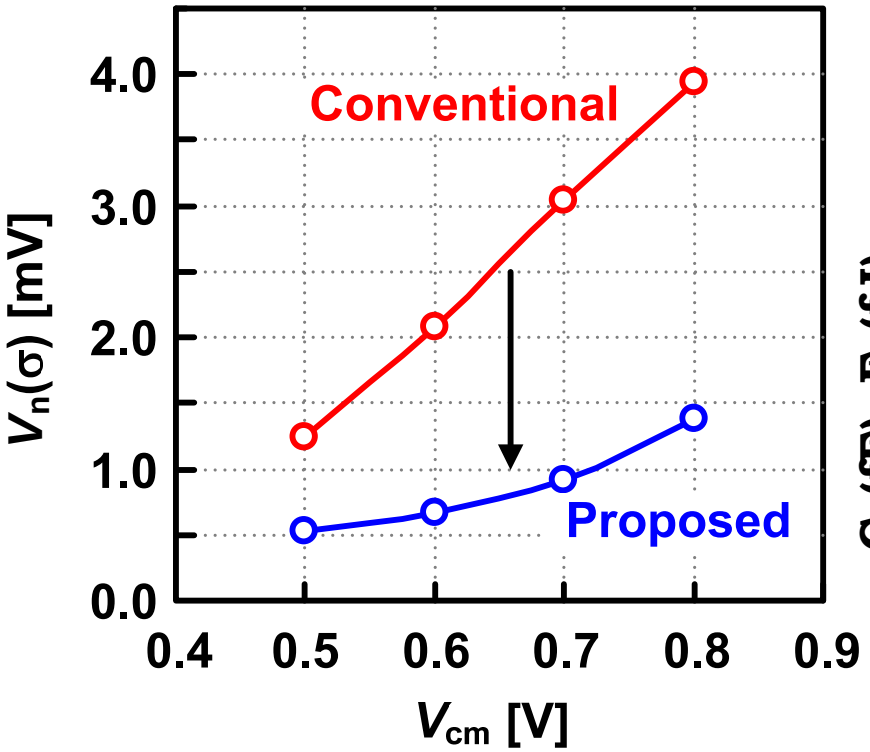
$$\overline{v_{ni}^2} = \frac{\overline{v_{n0}^2}}{G^2} = \frac{V_{eff}^2}{4V_{os}^2} \times \frac{4kT\gamma g_m T_d}{C_L^2} = \frac{2kT\gamma}{C_L} \frac{V_{eff}}{V_{os}} = \frac{2kT\gamma}{g_m T_d}$$

$$H(f) = \frac{2}{2\pi f} \sin(\pi f T_d) = T \cdot \sin c(fT_d)$$

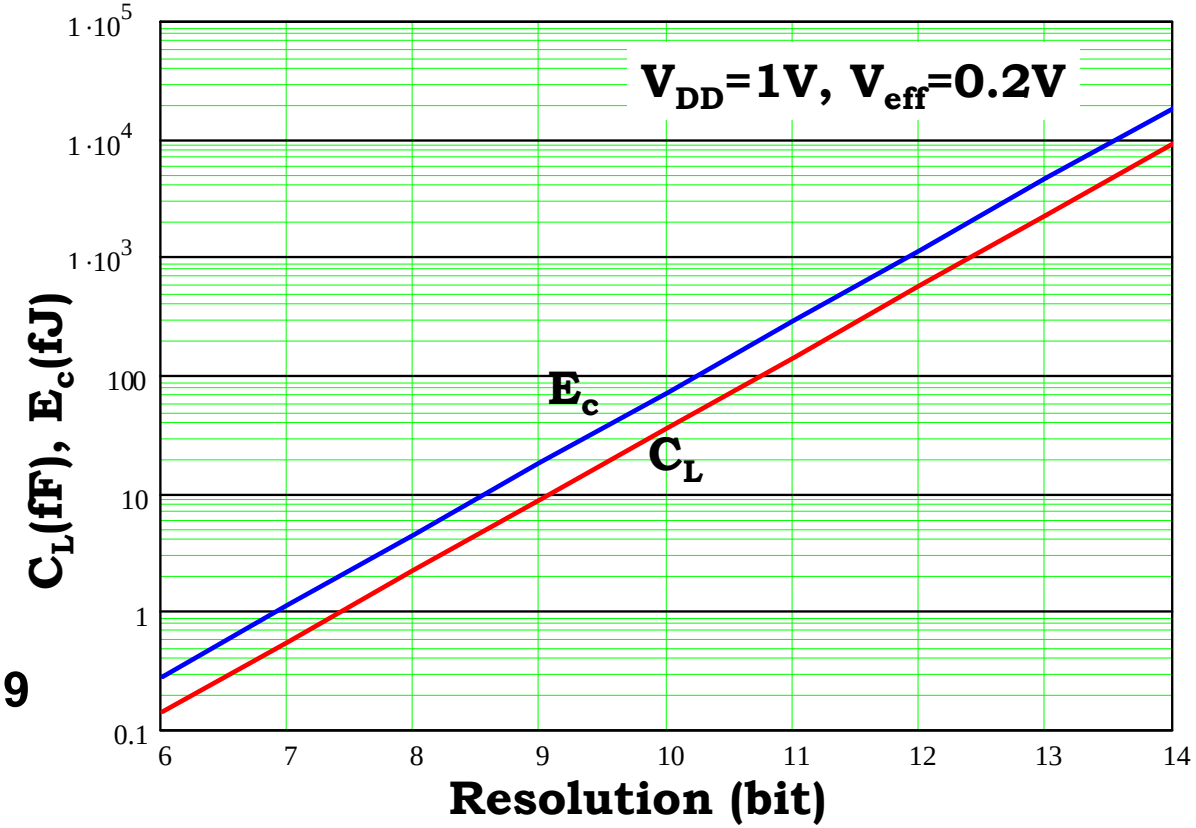
Required capacitance and consumed Energy

Node capacitances should be increased to realize higher ADC resolution. This results in increase of consumed energy of the dynamic comparator.

$$\overline{V_n^2} = \frac{V_{n\_latch}^2}{G^2} = \frac{V_{eff}^2}{4V_{os}^2} V_{n\_latch}^2$$



A dynamic amplifier with CMOS amplifier suppresses the noise from the latch



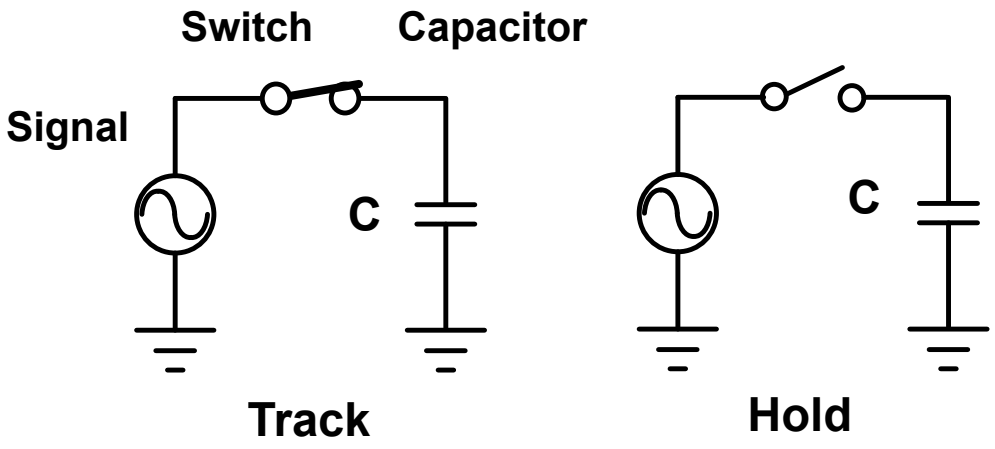
Fundamental Energy of sampling circuit

Fundamental energy of sampling is often used.

$$E_s = 24kT2^{2N}$$

However this neglects the power for comparison.

Sampling circuit



Quantization voltage

$$V_{qn} = \frac{V_{FS}}{2^N}$$

Quantization noise power

$$P_{qn} = \frac{V_{qn}^2}{12} = \frac{V_{FS}^2}{12 \cdot 2^{2N}}$$

Noise balance $V_n^2 = P_{qn}$

Capacitance $C = 12kT\frac{2^{2N}}{V_{FS}^2}$

Electrical energy=Thermal energy

$$\frac{1}{2}CV_n^2 = \frac{1}{2}kT \quad \therefore \; V_n^2 = \frac{kT}{C}$$

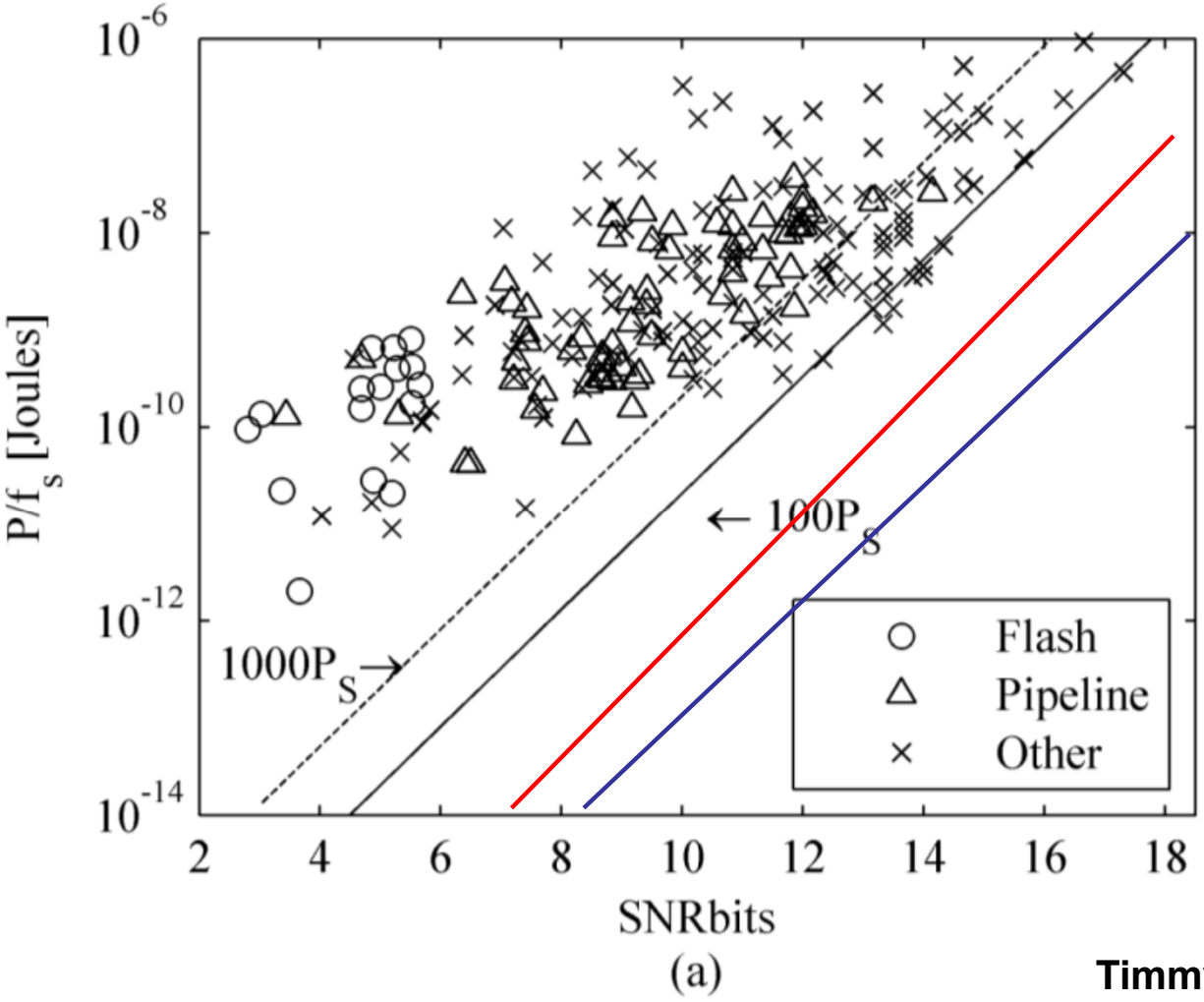
P_d of sampling circuit

$$E_d = 2CV_{FS}^2 = 24kT2^{2N}$$

Energy consumption of ADC

Consumed energy of ADC is mainly determined by the resolution.

Energy of ADC is reaching 100x of the fundamental sampling energy, and 10x of the fundamental ADC energy consumption.



Conventional fundamental sampling energy

$\mathbf{E_{ADC}}$

$\mathbf{E_s}$

$$E_s = 24kT_s 2^{2N}$$

$$E_s = 2^{2N} \times 10^{-19}$$

Fundamental ADC conversion energy involving energy consumption of comparato

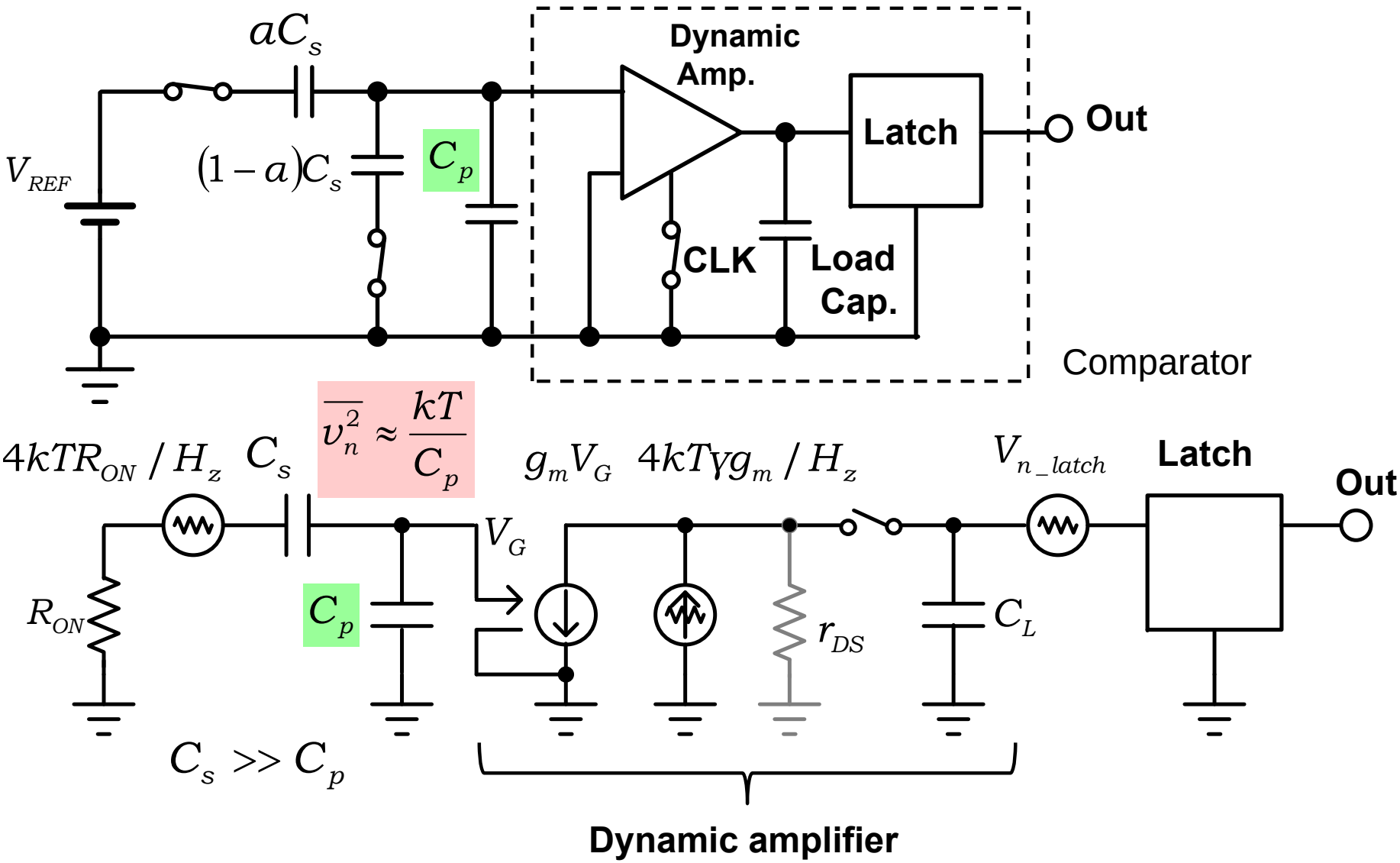
$$E_{ADC} \approx N \cdot E_s$$

$$E_{ADC} = N \times 2^{2N} \times 10^{-19}$$

Timmy Sundstrom, PhD thesis, Linkoping 2011.

Noise in comparison phase

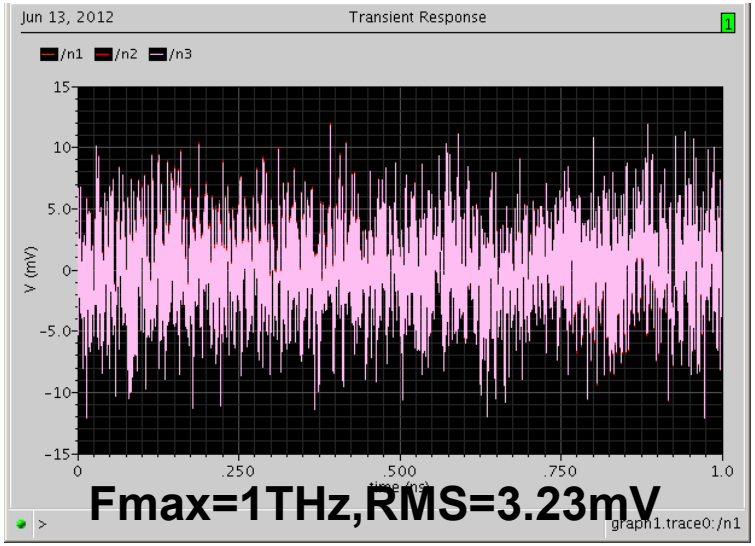
The switch resistance generates the noise and the noise voltage at the comparator is large due to the small parasitic capacitance.



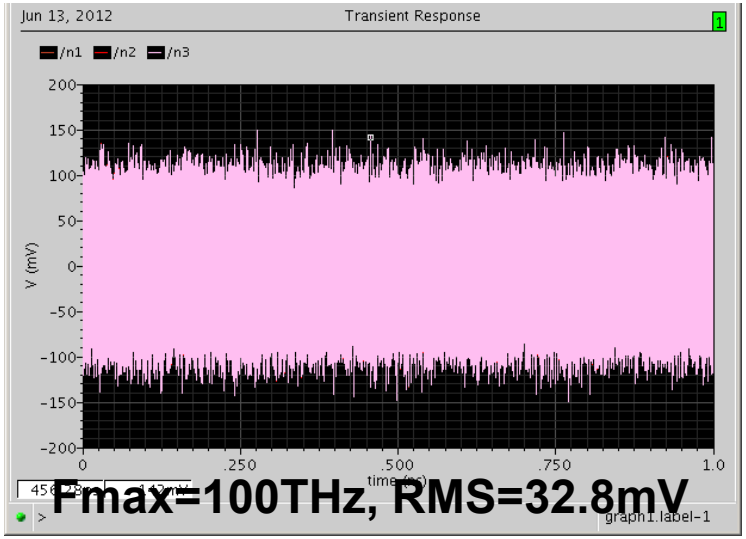
Transient noise simulation

Input noise is increased with frequency bandwidth, if C_p is very small.
If Cp exists, it determines noise voltage.

C_p=0

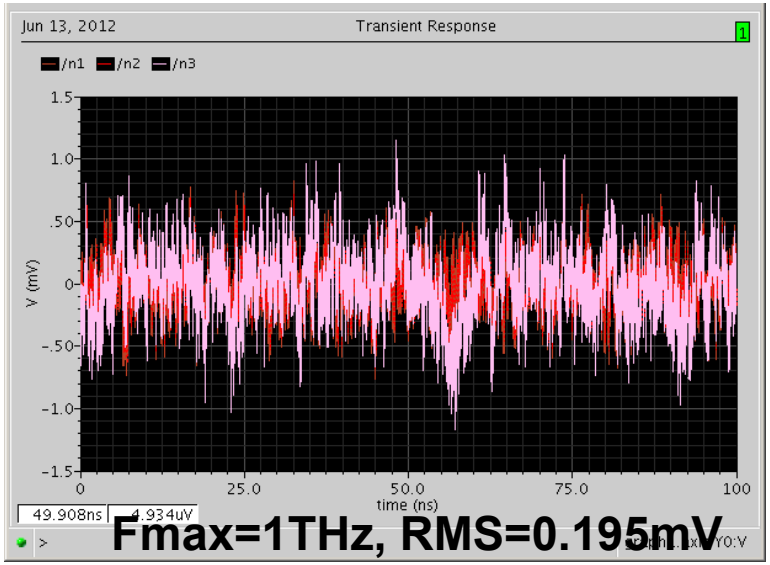


Fmax=1THz,RMS=3.23mV

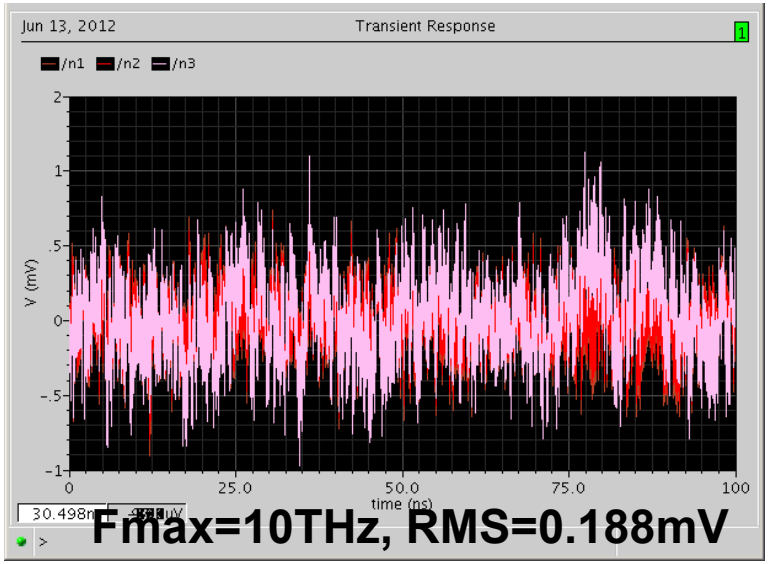


Fmax=100THz, RMS=32.8mV

C_p=100fF



Fmax=1THz, RMS=0.195mV



Fmax=10THz, RMS=0.188mV

Noise in comparison phase

Clear tradeoff between noise, speed and energy.

For low noise voltage

1）Large sampling capacitance
2) Small switch resistance
3) Long integration time
4) Large Load capacitance
5) Small latch noise
6) Large voltage swing
7) Small gate effective voltage

1) Sampling noise of C_s

$$\overline{V_{n1}^2} = \frac{2kT}{C_s}$$

2)Effective noise caused by the switch

$$\overline{V_{n2}^2} = \frac{4kTR_s}{\left(1+\frac{C_p}{C_s}\right)^2}\frac{1}{T_d}$$

3) Noise by the dynamic amplifier

$$\overline{V_{n3}^2} = \frac{4kT\gamma}{C_L}\frac{V_{eff}}{V_{os}} = \frac{4kT\gamma}{g_m T_d}$$

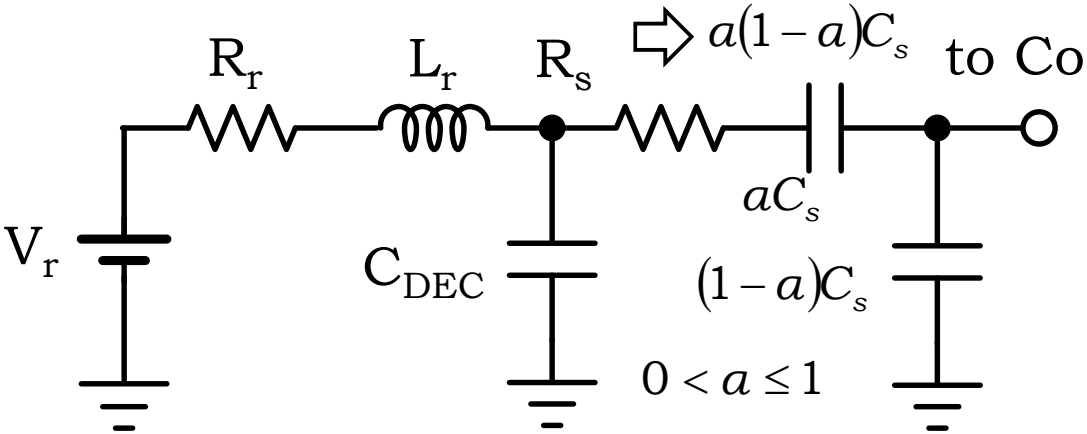
4) Noise by from the latch

$$\overline{V_{n4}^2} = \frac{V_{n\_latch}^2}{G^2} = \frac{V_{eff}^2}{4V_{os}^2}V_{n\_latch}^2$$

Dynamic response of reference circuit

Dynamic response of the reference circuit affects the linearity of the ADC.

Large decoupling capacitance is required to suppress this effect.
Impedance design (IC, bonding, package, board, etc.) becomes important.



$C_s = 4pF$
$a = 0.5$
$R_s = 20\Omega$
$R_r = 30\Omega$
$L_r = 5nH$
$V_r = 1.0V$

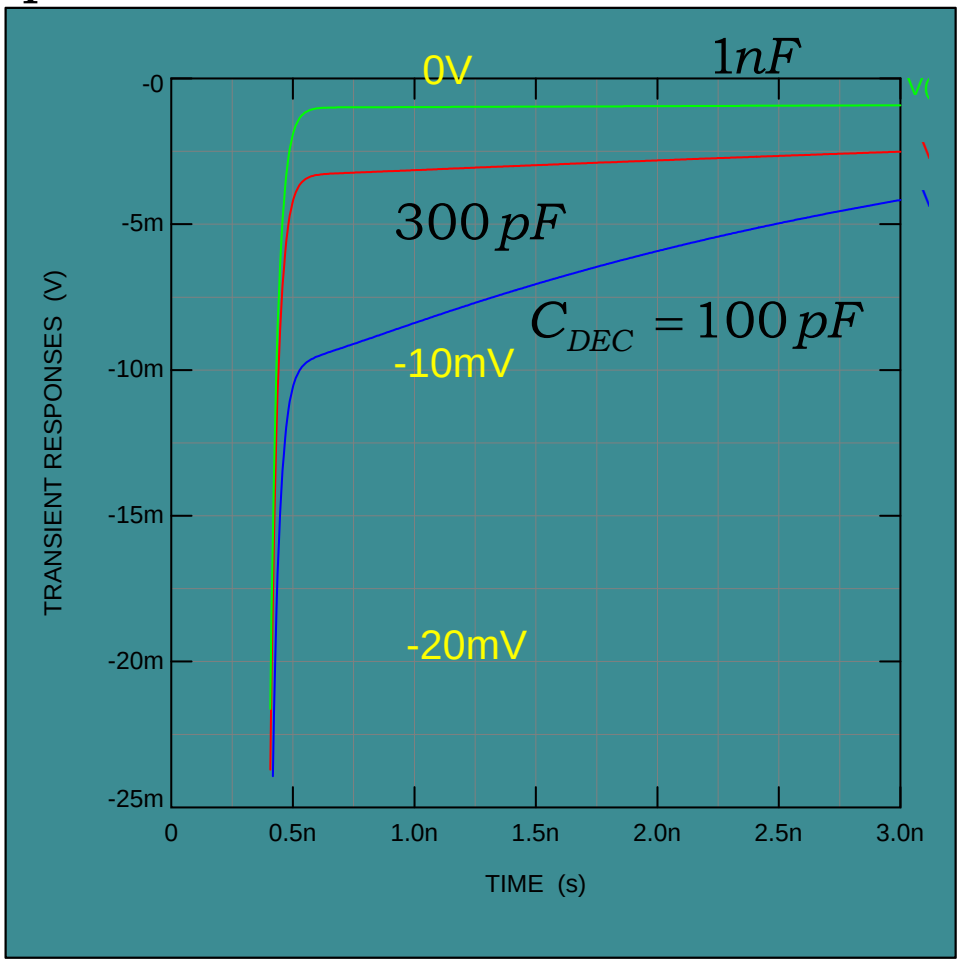
$$\Delta V_r \approx \frac{(1-a)C_s}{C_{DEC}}(V_R - V_{\text{int}})$$

V_{int}: Initial voltage of C_s

$$\Delta V_r(t) \approx \Delta V_r(0)e^{-\frac{t}{\tau}}$$

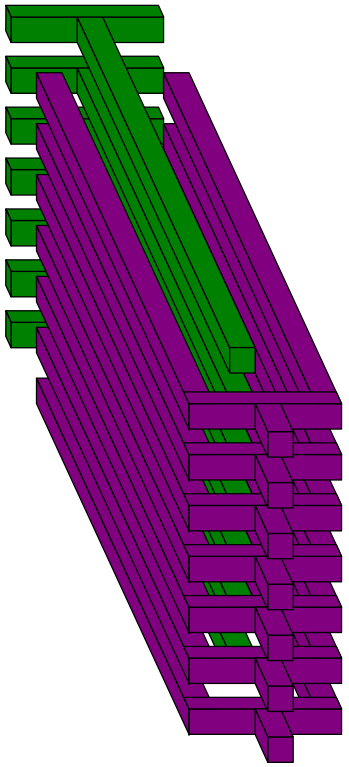
$$\tau \approx R_r C_{DEC}$$

1LSB: 0.5mV @12bit

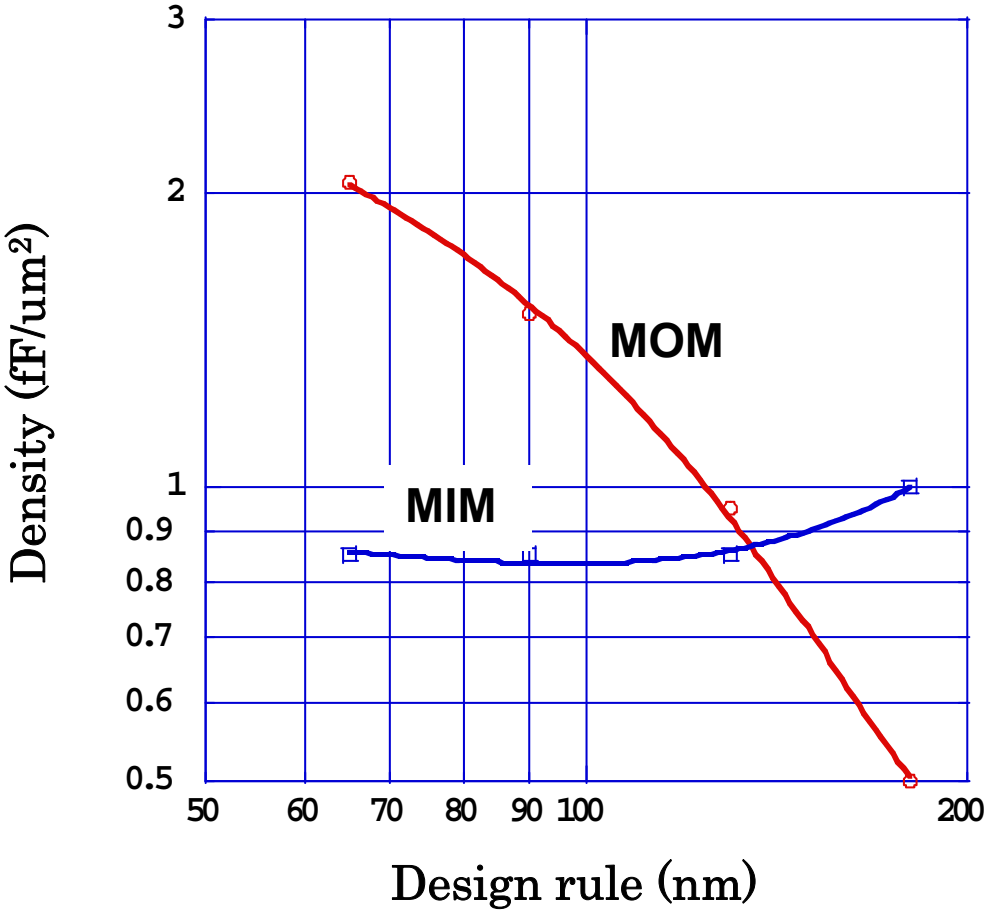


MOM capacitance

MIM capacitance has a good matching, MOM is not so,,,.
However matching issue can be solved by digital mismatch compensation.
Capacitor density is increased by technology scaling.
Very small capacitance (<0.1fF) is available and useful for the mismatch comp.



MOM capacitance



OpAmp based ADC design

Interpolated pipeline ADC

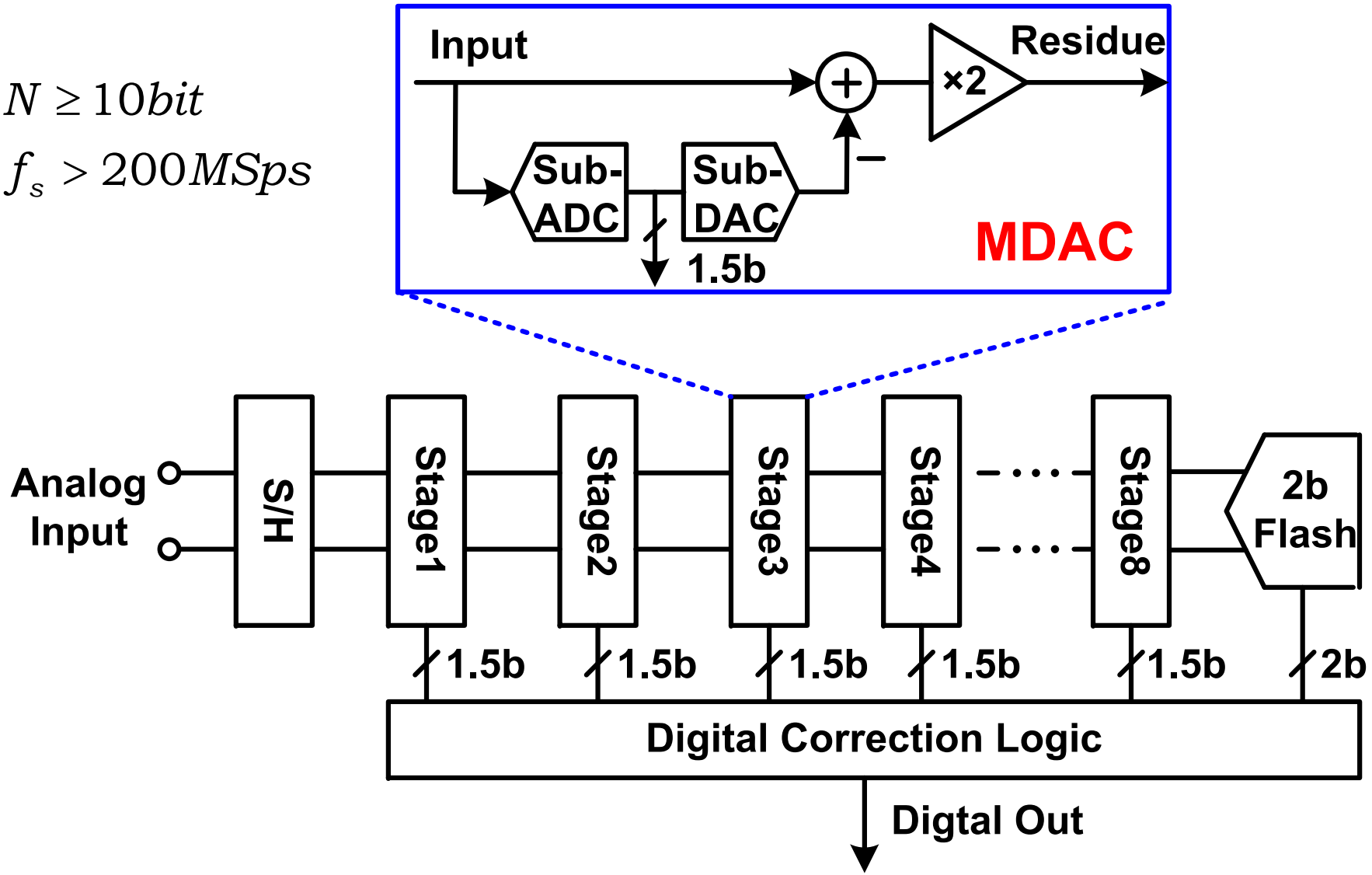
Conventional Pipelined ADC

Pipelined ADCs are still needed for high resolution and high speed ADC.

However, conventional pipelined ADC requires accurate MDAC

$N \geq 10bit$

$f_s > 200MSps$



OpAmp gain and conversion error

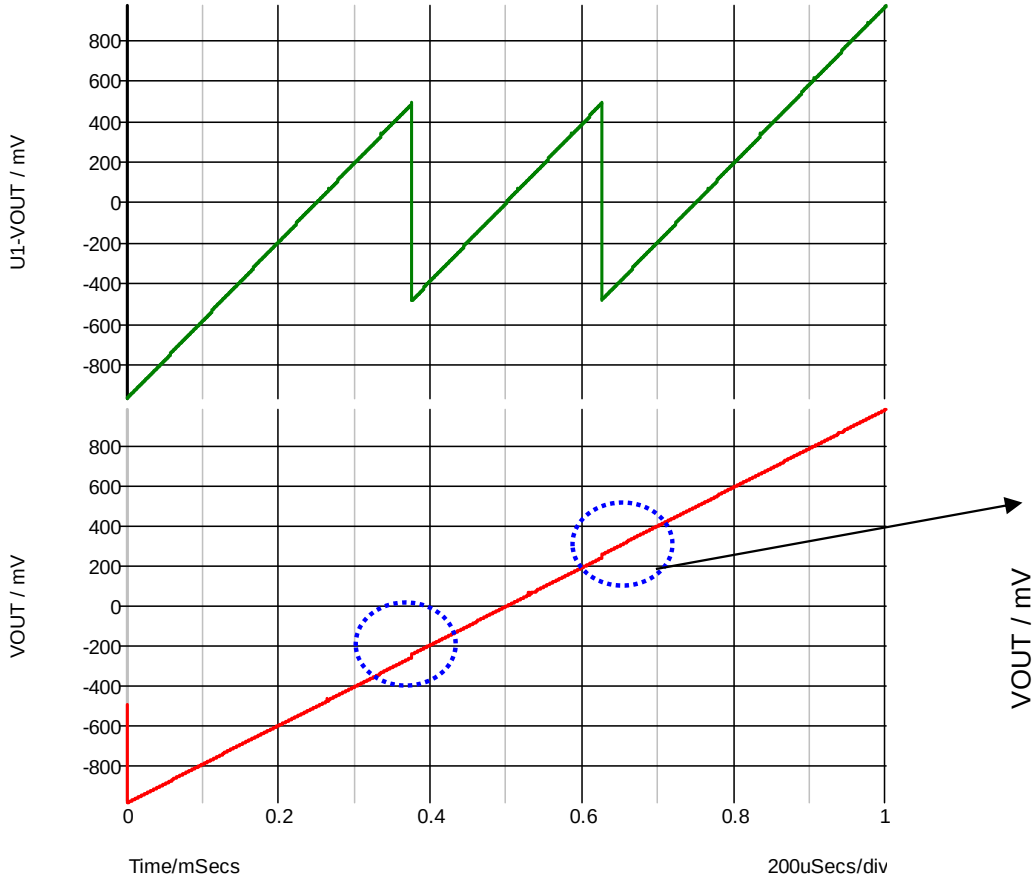
$$\varepsilon_{(LSB)} = \frac{3 \times 2^N}{G} \qquad G > \frac{3 \times 2^N}{\varepsilon_{(LSB)}}$$

$$G > 6N + 10\,(dB)$$

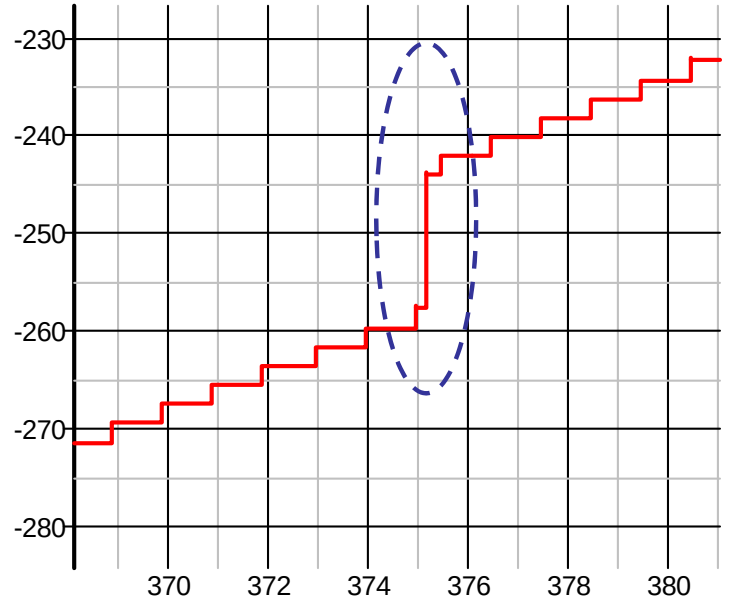
Gain>70dB

10bit ADC

Large error occurs



40dB gain



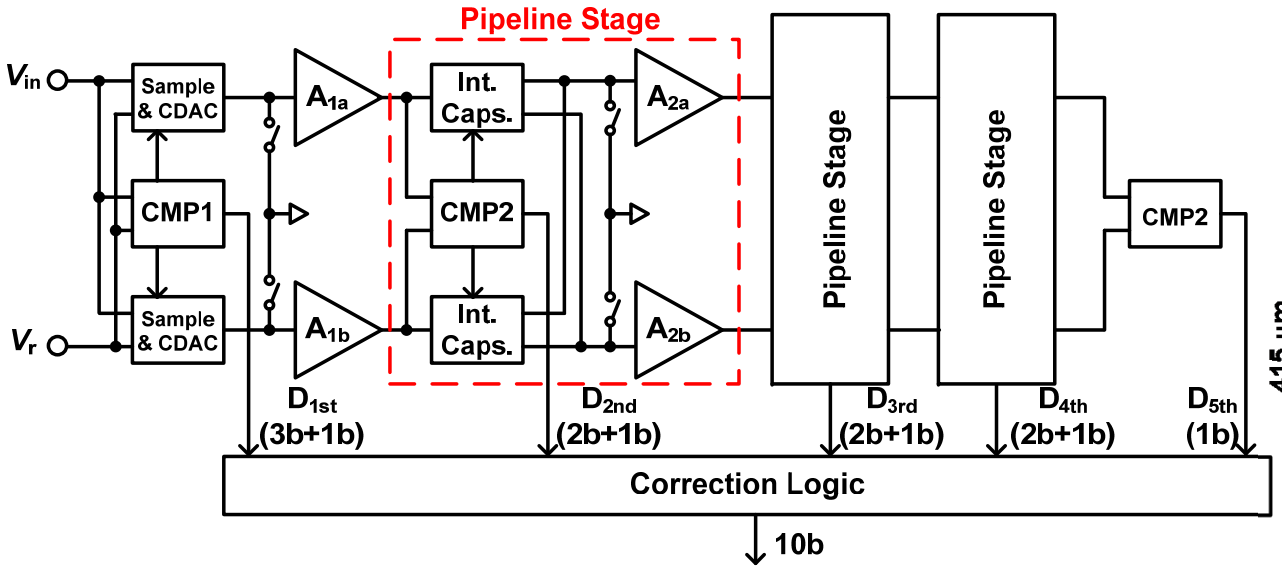
Developed ADC

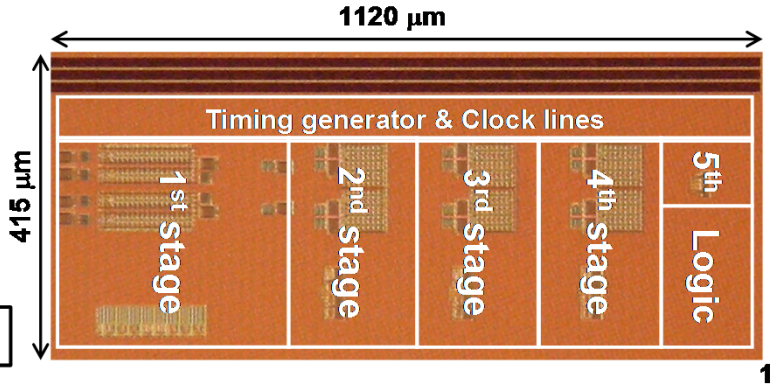
Developed new 10b ADC to address 64 QAM.

Interpolated pipeline scheme
No need of high gain OP amps

10b, 320 MSps, 40mW ADC

Suitable for low gain and low V_{DD} scaled CMOS



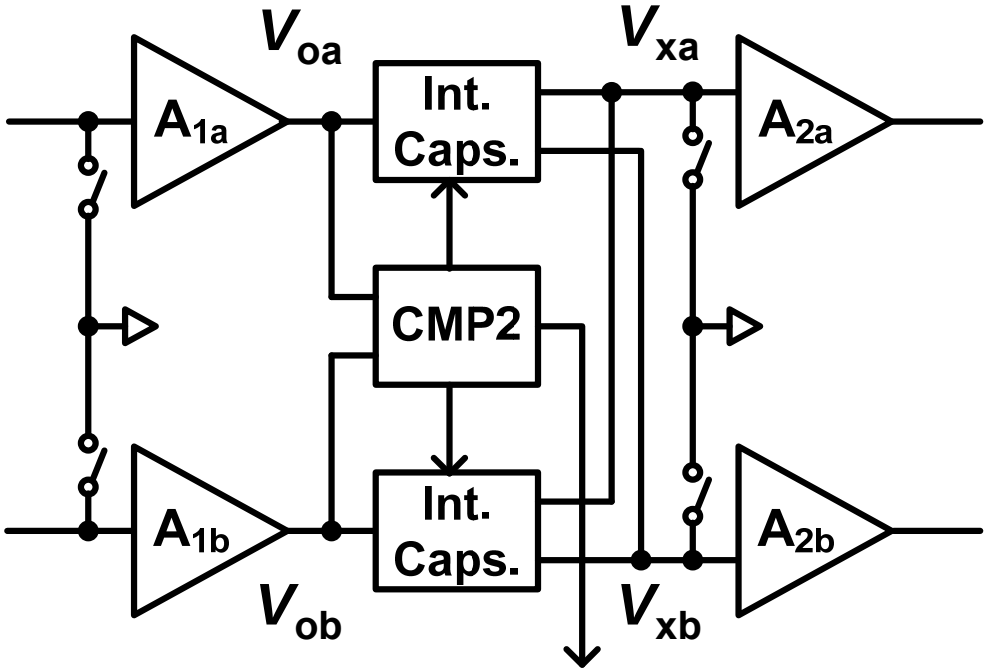


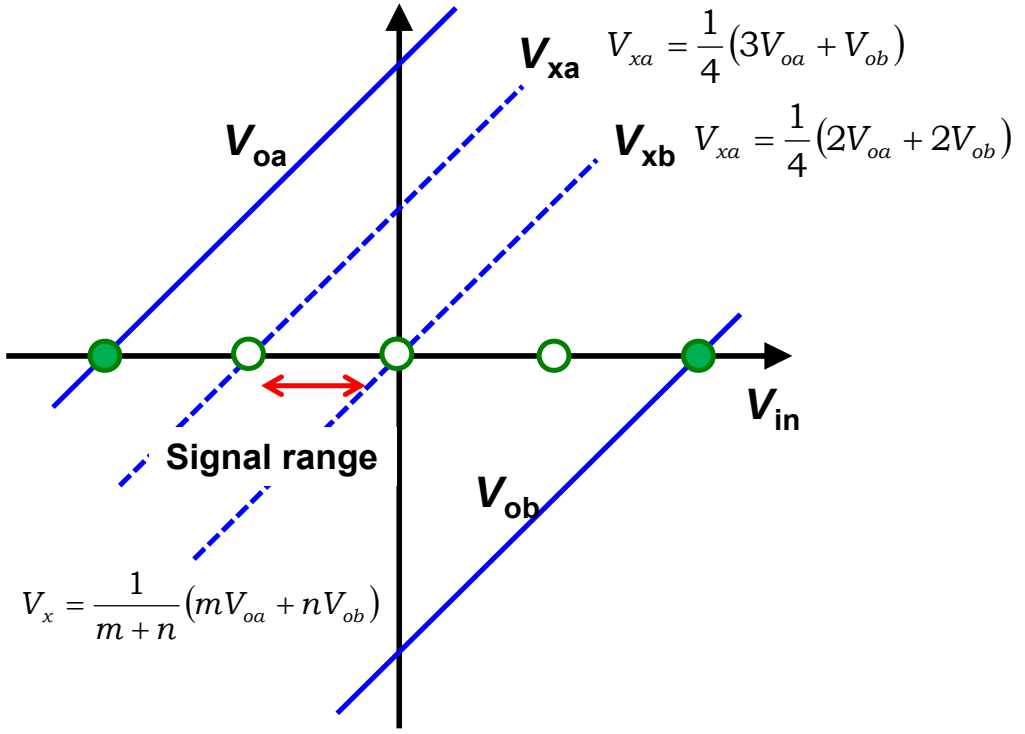
M. Miyahara, A. Matsuzawa, VLSI-CS, 2011.

Pipelined interpolation

The interpolation can realize the fine A/D conversion.
No accurate absolute gain is required.

The accuracy of cross points depends the gain mismatch, and does not depend the absolute gain



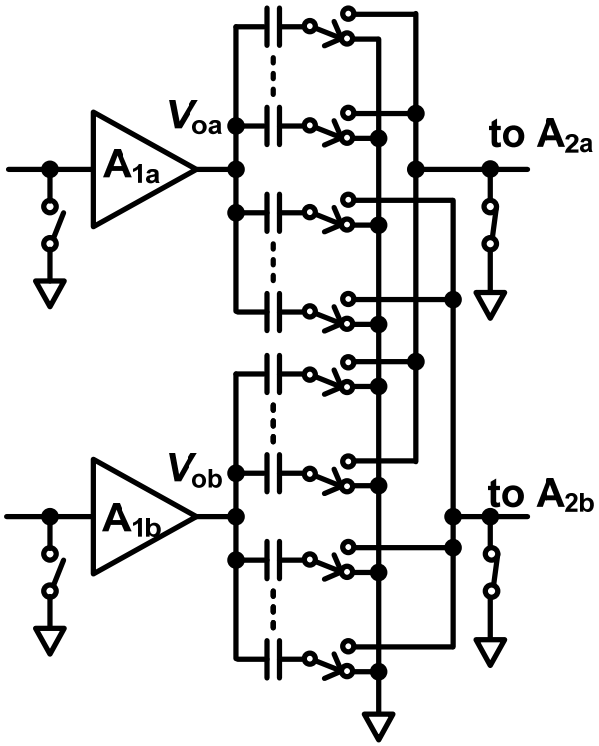


Gain of amplifiers is about 4

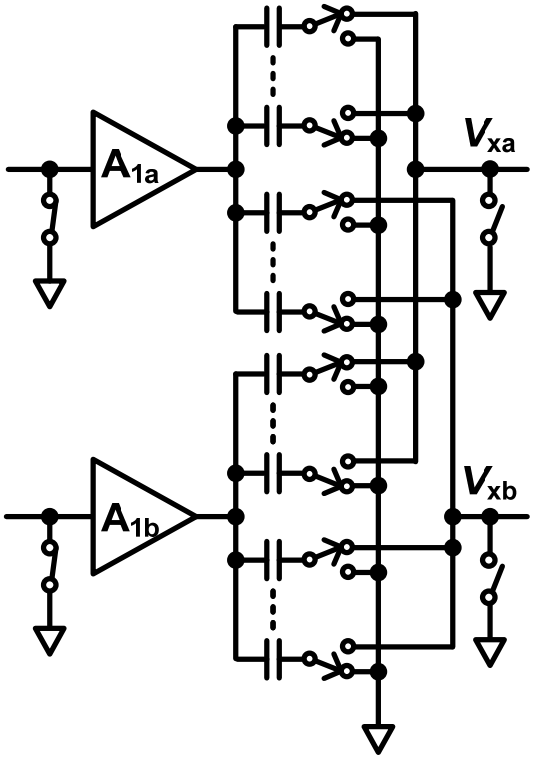
Proposed Weight Controlled Capacitor Array

Proposed weight controlled capacitor array realizes accurate interpolation. Furthermore, the offset voltages of amplifiers are cancelled.

$$V_x = -\left\{\frac{m}{m+n}G_a\left(V_{in}-V_{ra}\right)+\frac{n}{m+n}G_b\left(V_{in}-V_{rb}\right)\right\}$$



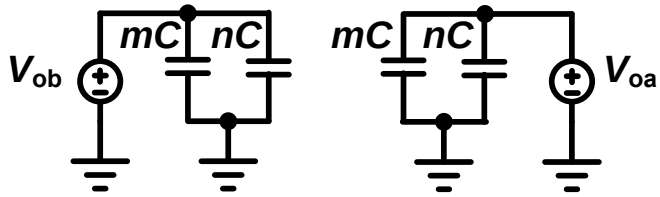
Sampling Phase



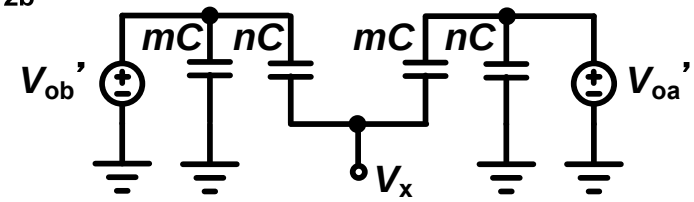
Interpolation Phase

$$V_{oa} = G_a\left(V_{in} - V_{ra} - V_{off\_a}\right)$$
$$V_{ob} = G_b\left(V_{in} - V_{rb} - V_{off\_b}\right)$$
$$V'_{oa} = G_a\left(-V_{off\_a}\right)$$
$$V'_{ob} = G_b\left(-V_{off\_b}\right)$$

$2^M = m+n$



Sampling phase

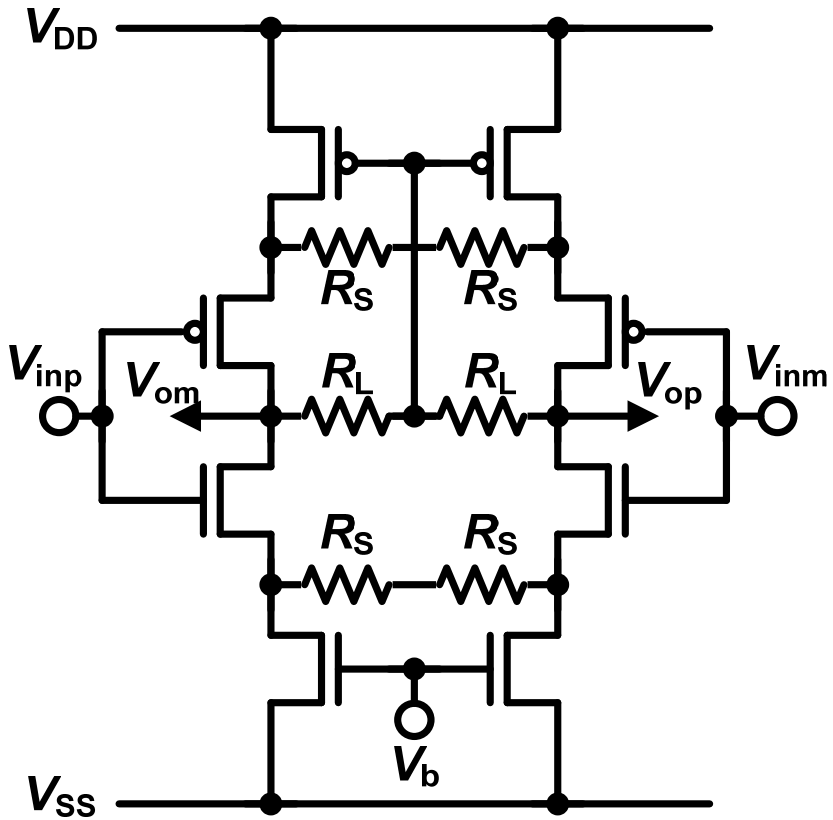


Interpolation phase

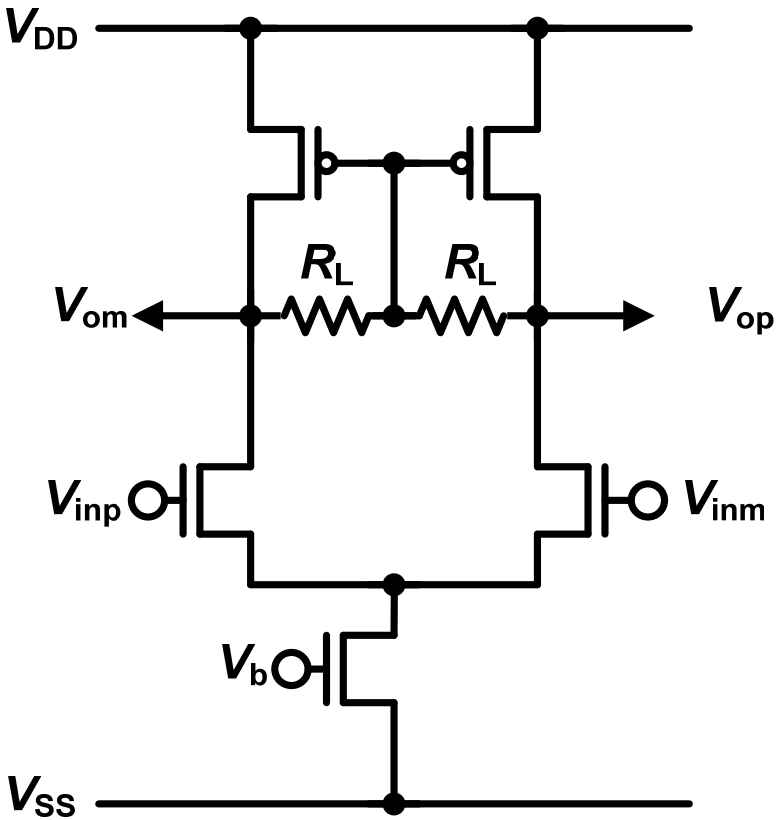
Low gain Amplifier

1st stage amplifier require good linearity
=>CMOS input with source degenerations

G= 4
Gain mismatch < 2.1%(3σ)



1st stage amplifier



2nd stage amplifier

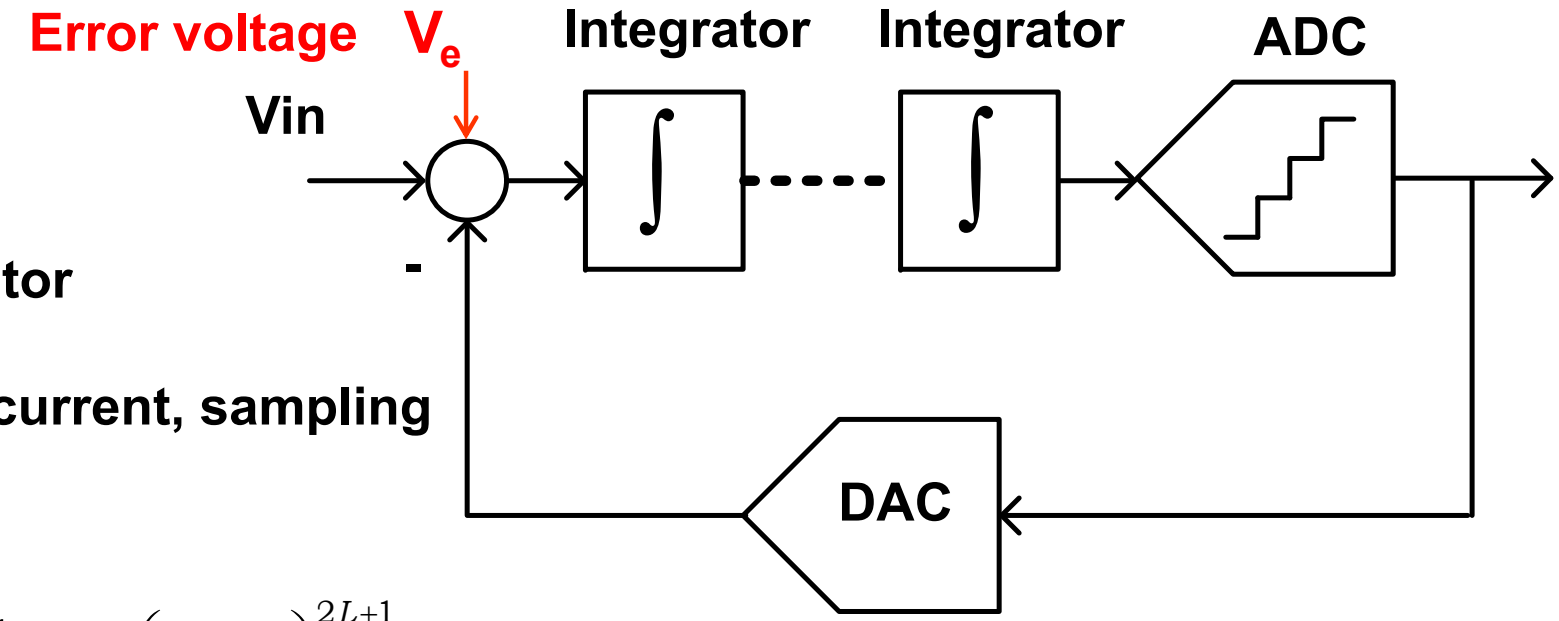
Performance summary

	This Work	[2]	[6]	[7]
Resolution (bit)	10	10	10	10
F_{sample} (MS/s)	320	500	205	320
V_{DD} (V)	1.2	1.2	1.0	-
Power (mW)	40	55	61	42
$ENOB_{peak}$ (bit)	8.5	8.5	8.7	8.7
FoM_{Fs}/ FoM_{ERBW} (pJ/c.-s)	0.35 / 0.77	0.31	0.65	0.36/0.44
Technology (nm)	90	90	90	90
Active Area (mm^2)	0.46	0.5	1	0.21
Amplifier type	Open	Closed	Closed	Closed
Linearity Compensation	No	Yes	No	Yes

[2] A. Verma and B. Razavi, IEEE J. Solid-State Circuits, vol. 44, Nov., 2009.
[6] S. Lee, Y. Jeon, K. Kim, J. Kwon, J. Kim, J. Moon, and W. Lee," ISSCC, 2007.
[7] H. Chen, W. Shen, W. Cheng, and H. Chen, A-SSCC, 2010.

Sigma-delta ADC

Sigma delta ADC can suppress only the quantization noise of ADC.
The performance is limited by the input error voltage.
For wide band signal, SD ADC may not be efficient architecture.



Error voltage
Noise of 1st integrator
Error of DAC
Noise of Resistor, current, sampling

$$N_q = \left(\frac{V_q}{2}\right)^2 \frac{1}{3\pi(2L+1)}\left(\frac{\pi}{OSR}\right)^{2L+1}$$

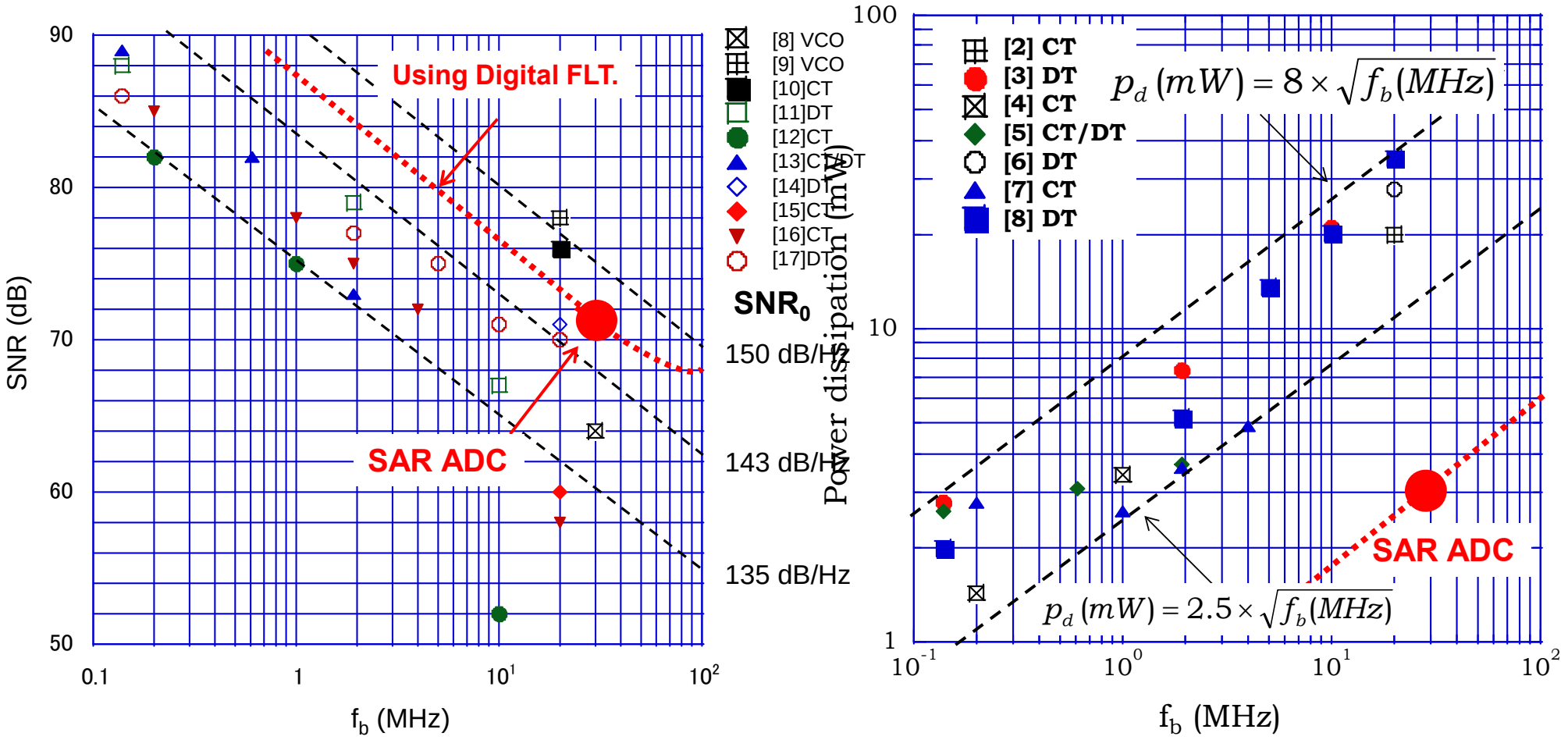
Quantization noise can be suppressed so much

$$V_{e\_eff} \approx \frac{V_e}{OSR}$$

Error voltage at input summing node can't be suppressed so much. Suppressed by only OSR.

SNR and P_d od SD ADC and SAR ADC

SNR and Power dissipation of wide band (multi-bit) SAR ADC are Not attractive. SAR ADC will reach the SNR and exhibit very low power consumption.

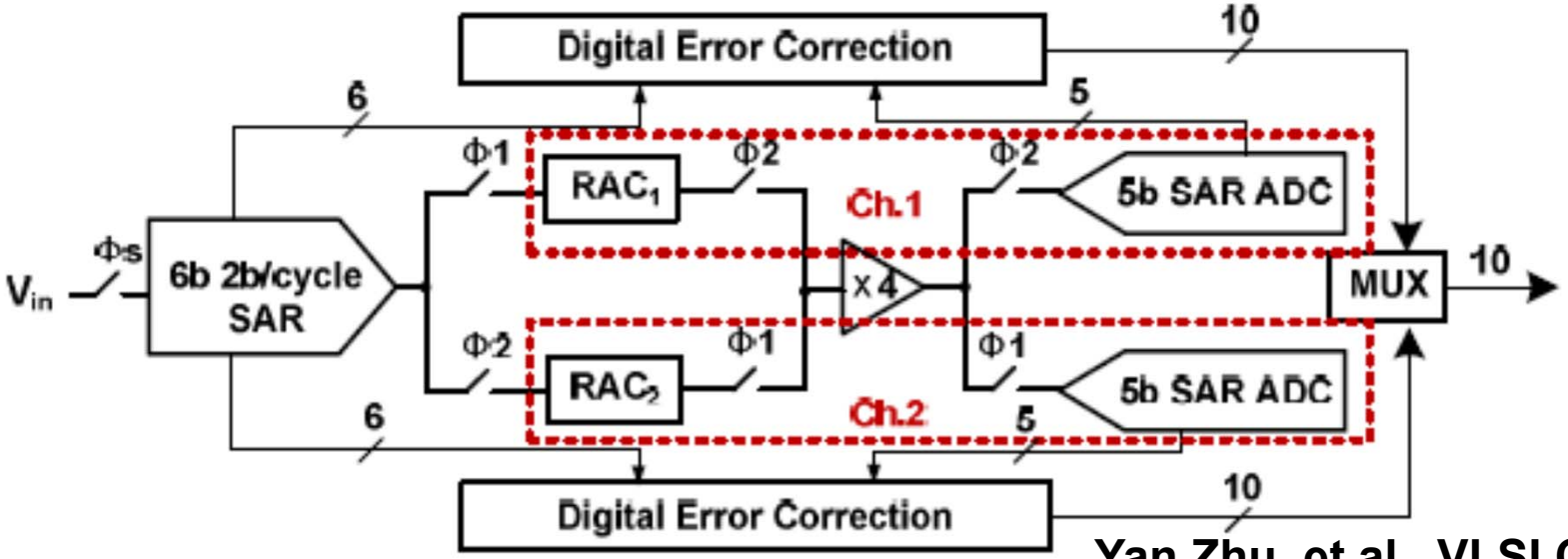


SAR Pipelined ADC

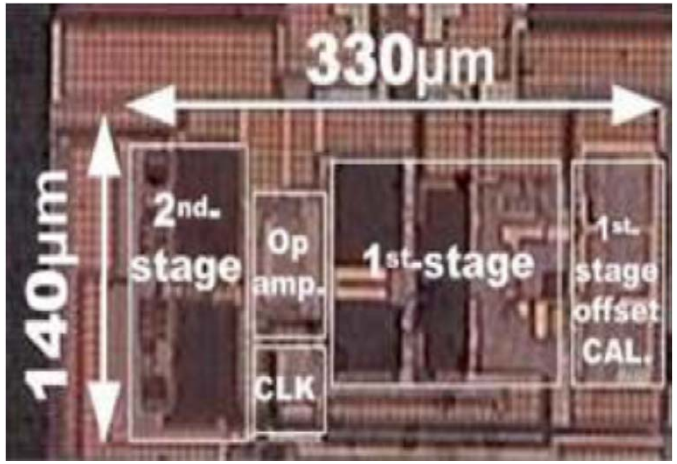
For wide fb and high SNDR ADC, SAR-Pipelined ADC is very attractive.

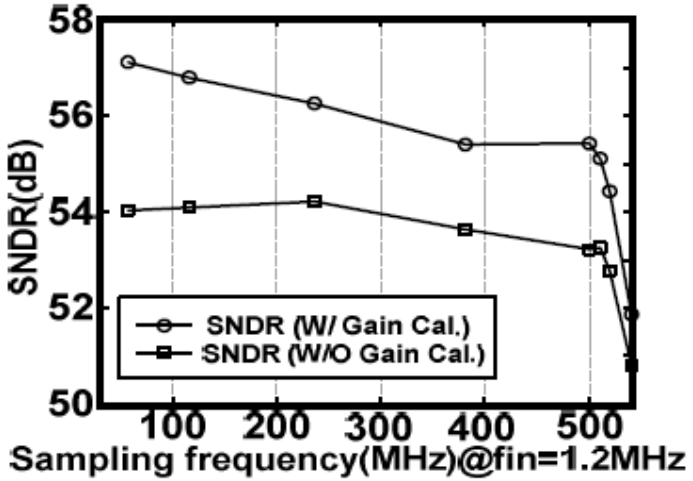
It can relax the requirement of settling time and noise of comparator

10bit, 500MSps, 8.2mW, FoM of 34fJ



Yan Zhu, et al., VLSI Circuits, 2012





Macau univ.

Summary: RF

- **60GHz CMOS Transceiver has been realized**
- **Technology scaling increases operation frequency to several 100GHz**
- **Accurate device modeling is very important**
- **Wide band width with proper matching and low phase noise of high frequency oscillator are required for high speed data transfer.**
- **Injection locking method is very innovative method to generate low phase noise high frequency signals and to realize frequency divider.**
- **Accurate phase control, address the HCI issue are next challenge.**

Summary: ADC

- **Flash ADC**
  - **Smaller is the better for Low FoM**
  - **Digital mismatch compensation tech. should be used**
- **SAR ADC**
  - **Concern the comparator noise**
  - **Remind the tradeoff (Noise, speed, power)**
  - **Take care of reference circuits**
- **Pipelined ADC**
  - **Proposed interpolated pipeline ADC offers good solution**
- **Future of ADC**
  - **ADCs will be unified by SAR ADC.**