A PVT-robust Feedback Class-C VCO Using an Oscillation Swing Enhancement Technique

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Abstract - This paper presents a feedback class-C VCO with PVT-robustness and enhanced oscillation swing. The proposed VCO starts oscillation as a differential LC-VCO for robust startup, and automatically adapts to an amplitude-enhanced class-C VCO in steady-state for lower phase noise. The proposed VCO is implemented in a 0.18μm CMOS process. The measured phase noise at room temperature is -125 dBc/Hz @ 1MHz offset with a power dissipation of 3.4-mW, from a carrier frequency of 4.84-GHz. The figure-of-merit is -193 dBc/Hz.

I Introduction

Recently, a class-C harmonics VCO (as shown in Fig. 1 (a)) is proposed in [1]. For a given power budget, phase noise of class-C VCO achieves significant improvement due to the efficient generation of MOS currents. However, the present class-C VCO suffers from the trade-off between oscillation amplitude and robust start-up condition over PVT variations [2]. Thus, this paper [3] proposes a feedback class-C VCO to address the above-mentioned issues.

II. Design Considerations of Proposed VCO

A. Issues of standard class-C VCO

As it is known, the phase noise of class-C VCO can be improved by increasing oscillation swing A_t. Unfortunately, according to the operation condition of class-C VCO, the oscillation amplitude is limited by the following equation.

$$A_t < \frac{V_{DD}-V_{gbias}+V_{th}}{2} \quad (1)$$

where V_{DD} is the supply voltage, V_{gbias} is the bias voltage of differential transistors, V_{th} is the threshold voltage.

To improve the oscillation amplitude of class-C VCO, the authors in [1] pointed out that V_{gbias} can be set slightly lower than V_{th}, if the sub-threshold gm of cross-coupled transistors is large enough to satisfy the startup condition. However, it is extremely sensitive to PVT variations. To guarantee robust startup to PVT variations, V_{gbias} cannot be set lower than V_{th} under the worst case, resulting in limited oscillation amplitude as discussed previously.

B. Proposed VCO using amplitude feedback

Fig.1 (b) shows the simplified diagram of proposed feedback VCO derived from a conventional class-C VCO. Fig.2 shows the detailed schematic of proposed VCO with negative feedback mechanism. There are three stages in the feedback loop. The first stage, which serves as a negative amplitude detector, consists of two NMOSs (M1, M2) and two capacitors. The second stage is a voltage follower formed by an operational amplifier (OA1). The purpose of OA1 is to provide a necessary isolation between V_{ref} and RC charging circuit in stage 1. The final stage is a voltage summing circuit, that is:

$$V_{gbias} = V_{ref} + V_c \quad (2).$$

At the initial state, the gate and drain voltage of M1 and M2 in stage 1 is initially at V_{DD}. Thus, M1 and M2 are both turned on, V_{gbias} (=V_{ref} + V_c) is high enough to ensure the startup condition. Consequently, the proposed VCO will start oscillation as the differential LC VCO with robust startup, which is illustrated in Fig.3. As the VCO starts to oscillate, the amplitude detector detects the negative amplitude of VCO, V_c becomes slightly higher than the negative amplitude of VCO but much lower than V_{DD}. As a result, V_{gbias} (=V_{ref} + V_c) also becomes lower along with the commencement of oscillation. Here, with the properly selection of V_{ref}, the proposed VCO can steadily operate at class-C condition. Therefore, the proposed feedback VCO solves the robust startup issue over the PVT variation.

The second significance of the proposed VCO is amplitude enlargement. With the robust startup provided by the feedback mechanism, the VCO could start oscillation steadily. Once stable oscillation has been built up, the voltage across tail capacitor increases rapidly due to the rectifying action of tail capacitor itself. Consequently, V_{gbias} can automatically become lower with sustainable class-C operation, which, in turns, increases the oscillation swing, thereby improving phase noise.

Note that conduction angle $2\phi_n$ is defined as $\cos(\phi_n)=(-V_{gbias}+V_{th})/A_t$, Fig. 4 shows current waveforms of conventional class-C with conduction angle $2\phi_0$ and proposed feedback class-C VCO in the initial state with conduction angle $2\phi_1$, and in the steady-state with conduction angle $2\phi_2$, respectively. Initially, ϕ_1 is 0.5π for robust startup condition. In the steady state, ϕ_2 is 0.3π for oscillation swing enhanced class-C operation with lower phase noise.

III. Measurement Results

Fig.5 shows the microphotograph of the proposed VCO fabricated in a 0.18μm CMOS process. The core chip area is 490μm×300μm. A conventional class-C VCO with identical parameters and layout, but with no feedback mechanism, is also fabricated as a reference on the same die. As illustrated in Fig.6, the proposed (conventional) VCO achieves -125 (-122) dBc/Hz phase noise at 1-MHz offset from a 4.84-GHz carrier, with a total power dissipation of 3.4-mW including 2 OAs (3.5-mW for V_{gbias}=0.65-V) from 1.2-V power supply. The corresponding FOM is -193 (-190 for V_{gbias}=0.65-V) dBc/Hz. The measured tuning range is 2.1%. Fig.7 shows the measured phase noise over temperature variation[-20^{o}C, 100^{o}C] for the conventional VCO at various V_{gbias}, and the proposed VCO. The phase noise of conventional VCO decreases significantly or even fails to oscillate due to the degradation of gm along with the increasing of temperature. Table I summarizes the performances comparison to other published VCOs [1][2][4-6].

IV. Conclusion

This paper [3] proposes a feedback class-C VCO with PVT- robustness and enhanced oscillation swing. With carful design, the proposed VCO can be suited for the PVT-robustness PLLs in wireline and wireless systems.

Acknowledgements

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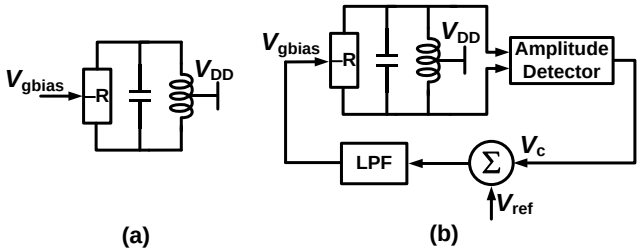


Fig.1. Simplified diagram of (a) conventional class-C VCO, and (b) proposed feedback class-C VCO.

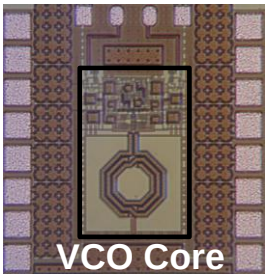


Fig.5. Chip microphotograph.

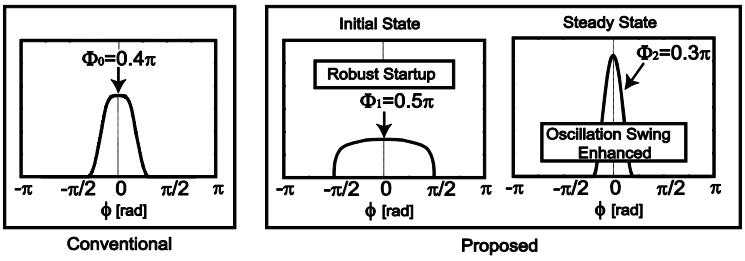


Fig.4. MOS current waveform of conventional class-C VCOs (left), proposed VCO at initial state (middle), and at steady state (right).

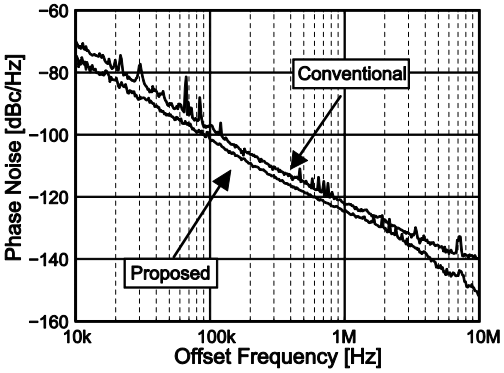


Fig.6. Measured phase noise characteristic: conventional class-C VCO and proposed VCO @ 4.84-GHz.

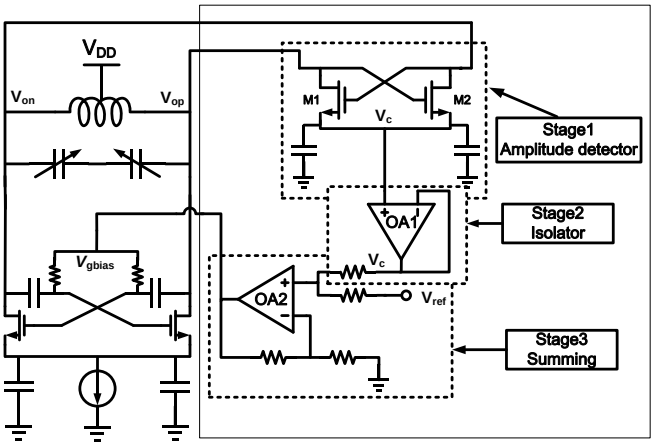
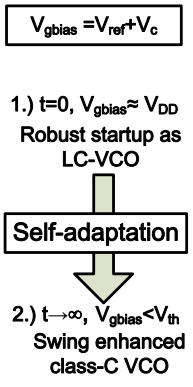


Fig.2. Detailed schematic of proposed feedback class-C VCO.



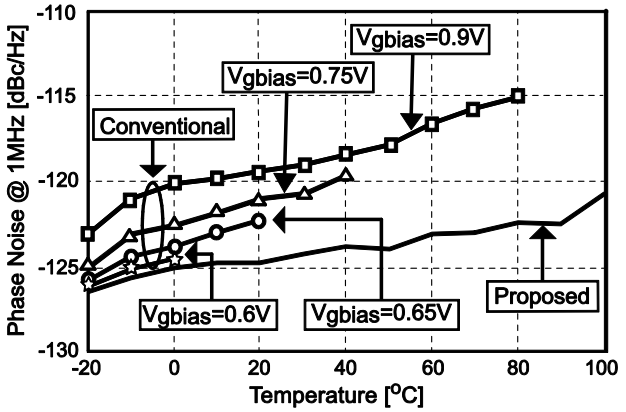


Fig.7. Measured phase noise characteristic over temperature for the proposed and conventional class-C VCOs at different V_{gbias}.

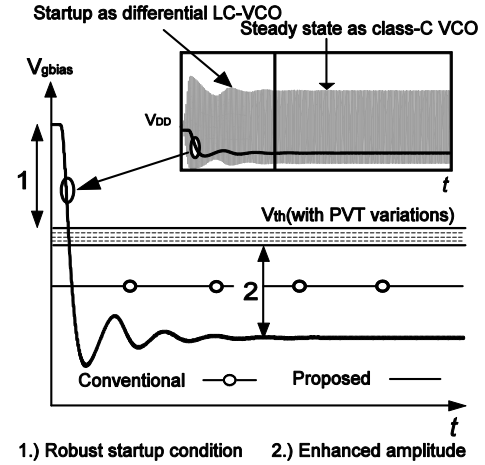


Fig.3. Graphical analysis and comparison of gate bias voltage in the conventional and proposed class-C VCOs.

TABLE I PERFORMANCE COMPARISON BETWEEN THE-STATE-OF-THE-ART VCOS.

	CMOS Process	Topology	Freq./Offset Freq. [GHz/MHz]	Phase Noise [dBc/Hz]	Pdc [mW]	FOM [dBc/Hz]
[1]	0.13μm	class-C[single]	4.9/3	-130	1.3	-196
[2]	0.18μm	class-C[dual]	4.5/1	-109	0.16	-190
[4]	0.18μm	Transformer	3.8/1	-119	0.57	-193
[5]	0.13μm	LC	28/1	-119	12	-191
[6]	0.18μm	Colpitts	1.86/1	-128	1.6	-191
Conventional	0.18μm	class-C[single]	4.84/1	-122	3.5	-190
Proposed		class-C[**feedback**]	4.84/1	-125	3.4	-193