A Progressive Mixing 20GHz ILFD with Wide Locking Range for Higher Division Ratios

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Abstract— This paper proposes Progressive Mixing Injection Locked Frequency Divider (PMILFD) technique that enhances the locking range for higher division ratios. As this technique uses lower and much stronger harmonics in the mixing process, it results in a stronger injection effect and a much wider locking range. Two 20GHz PMILFDs were designed based on this approach to divide by 4 and 8 using a 65nm CMOS process. The former achieves a 7.9GHz(31.4%) locking range and the later achieves a 3.4GHz(15.5%) while consuming 3.9mW and 7.1mW, respectively.

I. Introduction

Modern high frequency PLL systems employ high frequency dividers in the initial division stage. They are usually implemented as Current Mode Logic (CML) dividers and Injection Locked Frequency Dividers (ILFD). CML dividers are more robust but consume high power. ILFDs on the other hand consume much less power and can divide by higher than 2 which further save power. However, they suffer from narrow locking range especially for division ratios higher than 2. Most ILFDs use the same principle of direct mixing to generate the correct harmonic to be injected into the oscillator for locking as shown in Fig.1(a). As this method is not suitable for higher division ratios, progressive mixing [1] is proposed to enhance the locking range. It performs a multistep mixing that uses a much stronger harmonics in the mixing process to widen the locking range.

II. Progressive Mixing ILFD

The proposed PMILFD uses a multistep conversion model. In this model the injected signal at the N^{th} harmonic mixes with the $(\frac{N}{2})^{th}$ harmonic of the oscillator fundamental frequency and then again by the $(\frac{N}{4})^{th}$ and so on $\log_2 N$ times until a harmonic that is close to the oscillator fundamental is generated. For a divide-by-4 configuration as shown in Fig.1(b), the injected signal mixes with the second harmonic and fundamental to generate the injection signal whereas for a divide-by-8 it mixes with the fourth, second and finally with the fundamental as shown in Fig.1(c). The main advantage is that the injected signal mixes first with the $(\frac{N}{2})^{th}$ harmonic instead of the conventional $(N-1)^{th}$ since the former is much stronger than the later and thus will produce a stronger injection signal. A feature of such architecture is that intermediate stages can also be used as injection points for lower division ratios.

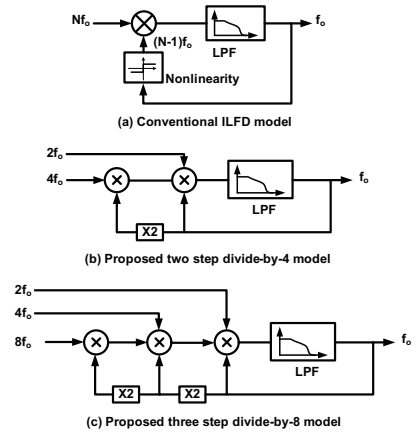

Fig. 1. ILFD models: (a) Conventional (b) Proposed two-step divide-by-4 (c) Proposed three-step divide-by-8

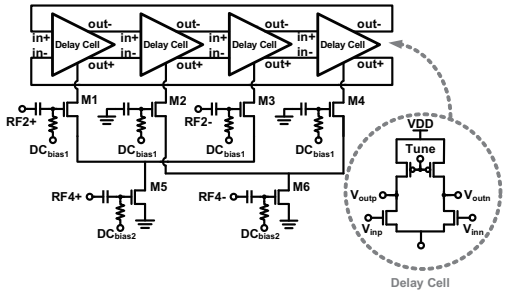

Fig. 2. Proposed PMILFD divide-by-4 circuit

The divide-by-4 circuit consists of a 4-stage ring oscillator as shown in Fig.2. PMOS transistors are used for the delay cell to facilitate frequency tuning. Tail transistors of each stage were connected as shown in the figure to form a 2-stage ring oscillator running at twice the fundamental frequency. Additional tail transistors M5 and M6 are used to facilitate injection and to act as current sources. The gates of transistors M1 and M3 are used as

TABLE I
PERFORMANCE COMPARISON BETWEEN PROPOSED WORK AND SIMILAR STATE-OF-THE-ART ILFDS

		PMILFD4	**PMILFD8**	**[2]**	**[3]**	**[4]**	**[5]**
CMOS Process		65nm	65nm	90nm	65nm	130nm	180nm
Supply [V]		1.2	1.2	0.5	1.2	1.2	18
Division Ratio		2, 4	4, 8	2, 4	2, 4	4	2, 4, 6, 8
Lock Range [GHz] (w.o. tuning)	÷2	**11.6 (92.1%)**	–	23 (34.3%)	12.1 (15.3%)	–	2 (55.6%)
	÷4	**7.9 (31.4%)**	**4 (31.8%)**	6.5 (7.3%)	1.9 (2.4%)	5.4 (21.7%)	1.6 (22.2%)
	÷8	–	**3.8 (15.1%)**	–	–	–	0.25 (1.7%)
Power [mW]		3.9	7.1	3.0	12.4 (÷4)	6	6.8
Area [mm^2]		0.003	0.006	0.064	0.978	0.140	0.007

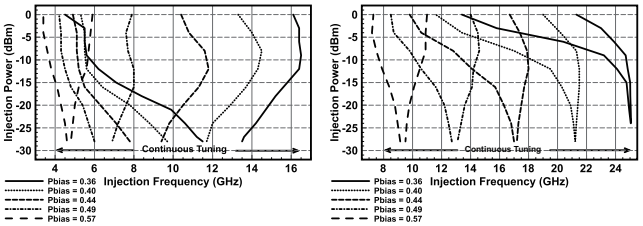

Fig. 3. Divide-by-2 locking and operation range with input applied to RF2 terminals (left) and divide-by-4 locking and operation range with input applied to RF4 terminals (right) of the divide-by-4 PMILFD

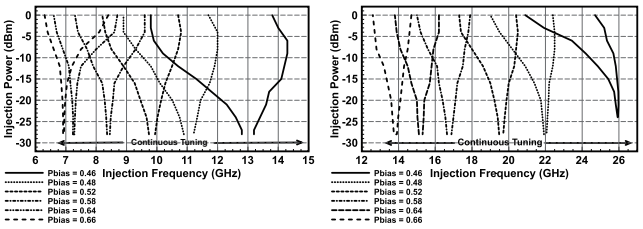

Fig. 4. Divide-by-4 locking and operation range with input applied to divide-by-4 terminals (left) and divide-by-8 locking and operation range with input applied to devide-by-8 terminals of the divide-by-8 PMILFD

a second input (RF2) if the PMILFD is to be used as a divide-by-2 circuit. The divide-by-8 PMILFD is designed in a similar fashion. However, for the intermediate points of injection, only divide-by-4 (RF4) inputs are used due to measurement setup limitations though it can have three inputs for division by 8,4, and 2.

III. Measurement Results

The two PMILFD were fabricated in 65nm CMOS process. The divide-by-4 PMILFD consumes a 3.9mW from a 1.2V supply and has a free-running tuning range from 2GHz to 8GHz. Fig.3 shows the locking range for divide-by-2 operation with 2.5GHz (53.7%) and up to 11.6GHz (92.1%) locking range at the highest frequency. The divide-by-4 input (RF4) has a 3.7GHz (39.7%) and up to 7.9GHz (31.4%) at the highest frequency as shown in Fig.3. The divide-by-8 PMILFD consumes a 7.1mA from a 1.2V supply and has a free-running tuning range from 1.6GHz to 5.3GHz. Locking range for divide-by-4 input, as given in Fig.4, is 2.1GHz (30.4%) and up to 4GHz (31.8%) at the highest frequency. Fig.4 plots

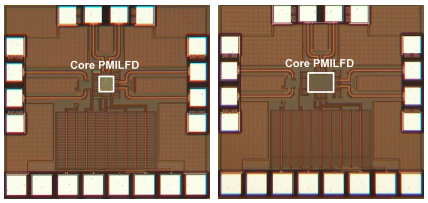

Fig. 5. Divide-by-4 PMILFD (on the left) and divide-by-8 PMILFD (on the right) chip photos

the locking range for the divide-by-8 input which shows a 2.1GHz (15.2%) and up to 3.8GHz (14.6%) locking range at the highest frequency. Chip photos are given in Fig.5 where the divide-by-4 PMILFD active area occupies 52μm×48μm and 66μm×86μm for the divide-by-8. Table I gives a comparison between this work and recently published ILFDs showing that both PMILFDs achieve the widest locking range in their class.

IV. Conclusion

This paper proposes the concept of Progressive Mixing ILFD (PMILFD) that widens the locking range of higher division ratios through a multistep downconversion of the injected signal. Using this concept, two 20GHz PMILFDs were designed and achieved the widest locking range reported to date for a division by 4 and 8.

Acknowledgment

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