

A 60-GHz 16QAM 11Gbps Direct-Conversion Transceiver in 65nm CMOS

Ryo Minami, Hiroki Asada, Ahmed Musa, Takahiro Sato, Ning Li, Tatsuya Yamaguchi,
Yasuaki Takeuchi, Win Chiavipas, Kenichi Okada, and Akira Matsuzawa

Dept. Physical Electronics, Tokyo Institute of Technology

Tel: +81-3-5734-3764, Fax: +81-3-5734-3764, E-mail: minami@ssc.pe.titech.ac.jp

Abstract— This paper presents a 60-GHz direct-conversion transceiver using 60-GHz quadrature oscillators. The 65nm CMOS transceiver realizes the IEEE802.15.3c full-rate wireless communication for every 16QAM/8PSK/QPSK/BPSK mode. The maximum data rates with an antenna built in a package are 8 Gbps in QPSK mode and 11 Gbps in 16QAM mode within a BER of $< 10^{-3}$. The transceiver consumes 186 mW while transmitting, and 106 mW while receiving. The PLL also consumes 66 mW.

I. INTRODUCTION

60-GHz wireless communication has become a very important research subject, because it is capable of achieving multi-Gb/s wireless communication [1–4]. The IEEE 802.15.3c standard defines four 2.16GHz-bandwidth channels around the 60-GHz frequency, and 3.5 Gb/s in QPSK and 7 Gb/s in 16QAM can be achieved by using the 2.16-GHz frequency bandwidth in raw data rate.

II. PROPOSED TRANSCEIVER

Fig. 1 shows the block diagram of the proposed transceiver, which realizes a direct-conversion architecture by using a quadrature injection-locked oscillator (QILO). One of the most stringent requirements for mmW direct-conversion transceivers is the phase noise. The proposed transceiver achieves very low phase-noise characteristics by the combination of 60-GHz QILO and 20-GHz PLL. Fig. 2 shows the QILO design, and the QILO works as a frequency tripler with a 20-GHz injection-lock input. Fig. 3 shows the circuit schematic, and it has an injection path and a tail I/Q coupling. The 20-GHz PLL is used for the injection-locking signal. The PLL has a two-stage divide-by-4 CML divider, a divide-by-5 static divider, and a programmable divider, $/27$, $/28$, $/29$, and $/30$, to generate 58.32 GHz, 60.48 GHz, 62.64 GHz, and 64.80 GHz with a 36 MHz reference, respectively.

The transmitter consists of a 4-stage PA, I/Q mixers, and a quadrature oscillator. The PA is implemented with a low-loss transmission line, which has a loss of 0.8 dB/mm. Transistors in the PA have the finger width of $2 \mu\text{m}$, and the total gate width of the final stage is $80 \mu\text{m}$. The double-balanced Gilbert mixer is used.

The receiver consists of a 4-stage LNA, I/Q passive mixers, and a quadrature oscillator. The LNA has a CS-CS topology to improve the noise figure, and the passive mixer is connected through a parallel-line transformer and a two-stage differential amplifier.

III. MEASUREMENT RESULTS AND CONCLUSION

The transceiver is fabricated in 65nm CMOS technology. Fig. 4 shows a die photo. The core areas of the transmitter and the receiver including all matching blocks are 3.5 mm^2 and

3.8 mm^2 , respectively. The core area of the PLL is 1.2 mm^2 . The antenna built in a package is used, which has a 2.2-dBi gain. The transmitter consumes 186 mW, and the receiver consumes 106 mW. The PLL also consumes 66 mW.

The measured free-running frequency of QILO is from 54 to 61 GHz, and two quadrature oscillators are used for each Tx and Rx to avoid insertion loss in 60-GHz LO distribution, which also contributes to maintain I/Q phase balance. The measured frequency range of the PLL is from 17.9 GHz to 21.2 GHz. The overall phase noise is $-94.2 \text{ dBc/Hz}@1\text{MHz}$ -offset at 60.48 GHz, which is 20 dB better than the conventional 60-GHz quadrature oscillator.

Fig. 5 shows the measured conversion gains of transmitter and receiver. The conversion gain of transmitter is 18.3 dB, and the output power is 9.5 dBm at 1 dB-compression. The LNA realizes a gain control, and the conversion gain of receiver is 17.3 dB in a high-gain mode and 4.7 dB in a low-gain mode. The entire noise figure is less than 6.8 dB in the high-gain mode. Fig. 6 shows a measured spectrum with the IEEE802.15.3c spectrum mask. The input I/Q signal for QPSK is generated by AWG with a symbol rate of 1760 Msps and a roll-off factor of 25 %.

Table I shows the measured constellation and performance summary. Two test boards are used as Tx and Rx. AWG is used to generate an I/Q modulated signal for 16QAM/8PSK/QPSK/BPSK mode, and an oscilloscope is used to evaluate the constellation, EVM, and BER with a built-in software. The full-rate communication is capable for the channel 1 (57.24 GHz to 59.40 GHz) and the channel 2 (59.40 GHz to 61.56 GHz) of IEEE802.15.3c within a BER of $< 10^{-3}$. Table I also shows the communication distance range using the 2.2-dBi antenna, and the low-gain mode of LNA is used for short-distance receiving. The maximum data rates in QPSK and 16QAM with a 25 % roll-off are at least 8 Gbps and 11 Gbps within a BER of $< 10^{-3}$.

Table II shows a performance comparison with 60-GHz transceivers. The proposed transceiver is the first 16QAM direct-conversion transceiver. It achieves full-data rates for every modulation scheme determined by the IEEE802.15.3c standard within the 2.16 GHz bandwidth. It was evaluated with the in-package antennas. Both the transmitter and receiver are driven by a quadrature oscillator, which allows high-quality modulation.

ACKNOWLEDGEMENTS

This work was partially supported by MIC, MEXT, STARC, NEDO, Canon Foundation, and VDEC in collaboration with Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd.

REFERENCES

- [1] K. Okada, *et al.*, *IEEE ISSCC*, pp. 160–161, 2011.

- [2] C. Marcu, et al., *IEEE JSSC*, vol. 44, no. 12, pp. 3434–3447, Dec. 2009.
- [3] A. Siligaris, et al., *IEEE ISSCC*, pp. 162–163, 2011.
- [4] S. Emami, et al., *IEEE ISSCC*, pp. 164–165, 2011.

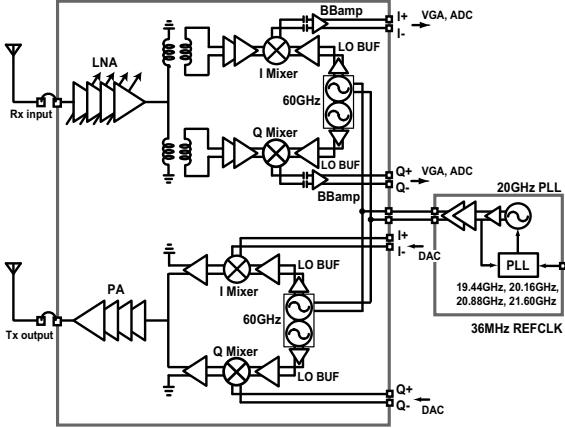


Fig. 1. Block diagram of the 60-GHz direct-conversion transceiver.

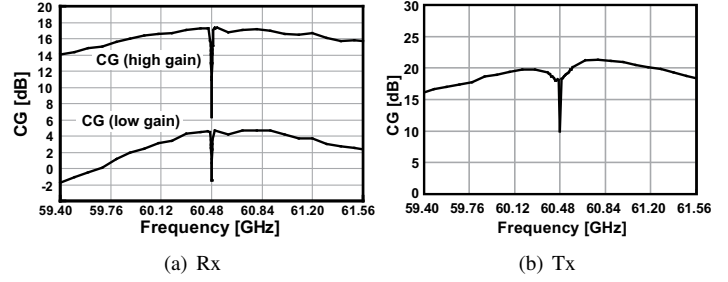


Fig. 5. Measured conversion gain.

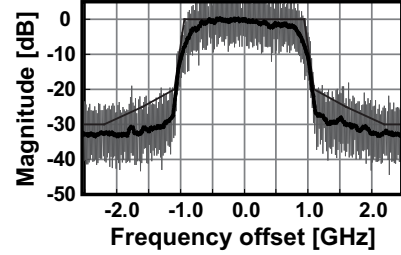


Fig. 6. Measured modulated spectrum at Tx output for 16QAM.

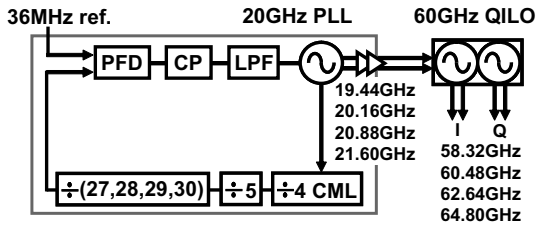


Fig. 2. Block diagram of the 60-GHz quadrature local synthesizer.

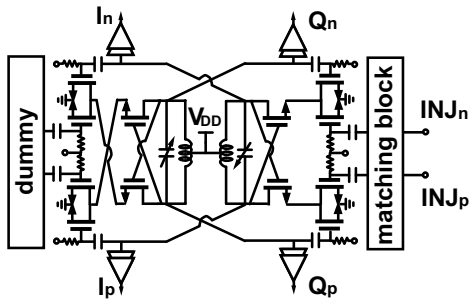


Fig. 3. Schematic of the quadrature injection-locked oscillator.

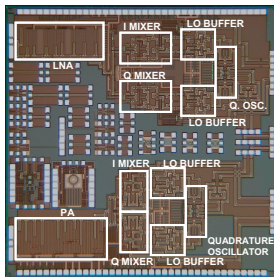


Fig. 4. Die micrograph of the transceiver and receiver.

TABLE I
MEASURED CONSTELLATION, DATA-RATE, EVM, AND COMMUNICATION DISTANCE.

Constellation		
Modulation	QPSK	16QAM
Data rate within 2.16 GHz-BW	3.52 Gb/s (max 8 Gb/s)	7.04 Gb/s (max 11 Gb/s)
EVM	-18 dB	-17 dB
Max communication distance with 2.2-dBi package antenna	2.70 m	0.17 m

TABLE II
PERFORMANCE COMPARISON WITH 60-GHz TRANSCIEVERS

	Data rate / Modulation	Architecture	Power consumption
NEC	2.6 Gb/s-QPSK	Heterodyne	133 mW (Tx) 206 mW (Rx)
[2] UCB	4 Gb/s-QPSK	Direct-conversion	170 mW (Tx) 138 mW (Rx)
[3] CEA-LETI	3.8 Gb/s-16QAM	Heterodyne	1.357 W (Tx) 454 mW (Rx)
[4] SiBeam	3.8 Gb/s-16QAM	Heterodyne	1.82 W (Tx) 1.25 W (Rx)
This work	8 Gb/s-QPSK 11 Gb/s-16QAM	Direct-conversion	186 mW (Tx) 106 mW (Rx) 66 mW (PLL)