A 60 GHz Power Amplifier Using High Common-Mode Rejection Technique

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***Abstract*—This paper proposes the method of realization of high common-mode rejection ratio(CMRR) at 60 GHz. High CMRR can compensate the differential mismatch. In the proposed method, virtual ground for differential-mode and LC peaking for common-mode are utilized. To confirm the effect of this technique, the 2-stage differential power amplifier is fabricated in a 65 nm CMOS process. It achieves a CMRR of 26 dB, a power gain of 12.1 dB, a peak PAE of 11.1 %, a $P_{\rm sat}$ of 9.0 dBm, a power consumption of 45.8 mW from a 1.0 V power supply.**

***Index Terms*—60 GHz, CMRR, Power amplifiers, CMOS.**

I. Introduction

Recently, high-speed wireless communication at 60 GHz is attracted. This is because the very wide bandwidth around 60 GHz can be used without license in many countries, and high speed wireless communications can be realized. Thus, considering the costs, we can use the CMOS technology instead of compound semiconductors for 60 GHz RF front-end[1]. Fig. 1 shows the block diagram of the transceivers which is presented in [1]. This transceiver is used direct-conversion architecture for reducing chip area and costs. Direct-conversion architecture requires high isolation between RF and LO ports. At 60 GHz, so many parasitic capacitance effects to the circuit design. Thus if common-mode signal of differential amplifier is large, it transfers from the RF port to LO port through parasitic capacitances. Moreover, signal-to-noise ratio(SNR) is reduced because of common-mode signal. In this work, to avoid these unfavorable problems, high CMRR technique for 60GHz differential amplifier is used.

Section II describes the conventional technique of common-mode rejection(CMR), section III shows the proposed technique of CMR, and section IV presents the measurement result of the differential power amplifier(PA) and performance comparison.

II. Conventional Method of CMR

One of the most common techniques of CMR is use of tail current source for up-to-5 GHz amplifiers. It performs as virtual ground for a differential signal, and as infinite impedance for a common signal. However, this technique is difficult to use at 60 GHz because of parasitic capacitance of current source. It decreases the impedance of current source and CMRR. Moreover the voltage headroom is reduced and

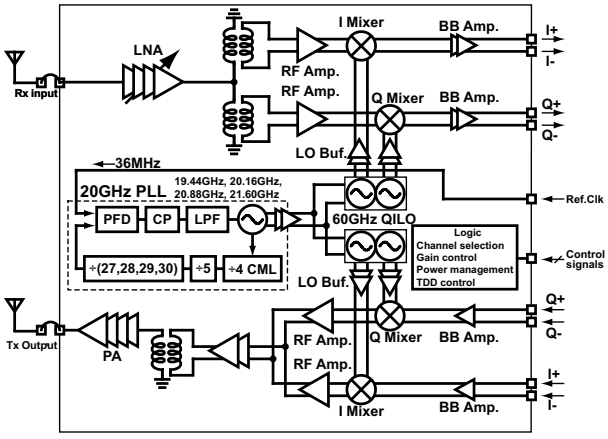

Fig. 1. Block diagram of the 60 GHz transceiver[1].

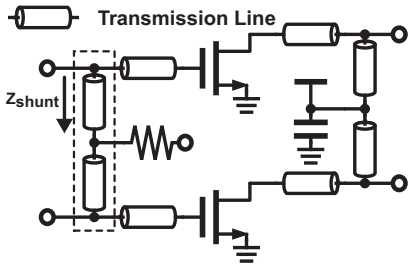

Fig. 2. Conventional method of CMR.

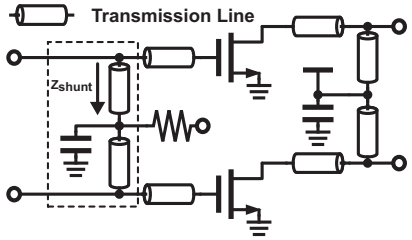

Fig. 3. Proposed method of CMR.

affect the linearity of amplifier. Thus, CMR technique using virtual ground in matching block is preferable at 60 GHz amplifier.

Fig. 2 shows the simplified differential circuit to explain a conventional CMRR technique at 60 GHz. At 60 GHz, the length of component cannot be ignored compared with the wavelength. Thus it needs to be considered by distributed constant not lumped constant and use transmission line(TL). The centor point of shunt matching works as virtual ground for differential-mode and open matching for common-mode. When we design good matching for differential-mode, common-mode matching is shifted from best matching point because the characteristic of short stub and open stub are different.

However, it is not sufficient to reduce common-mode signal because it is impossible to adjust the characteristic of common-mode only on the smith chart.

III. Proposed High CMR Technique

Fig. 3 shows the proposed method of realization of high CMRR at 60 GHz. The proposed method inserts the capacitance at the center point of matching block to achieve the impedance matching for a differential-mode signal and the reflection for a common-mode signal. TL of $Z_{\rm shunt}$ part works as an inductance. Thus this method can realize the variable short stub for common-mode signal by designing arbitrary value of capacitance. Moreover, this capacitance cannot effect for differential-mode. Therefore, we design the good matching for differential signal using virtual ground, and we can realize matching shift for common-mode arbitrary.

It is possible to estimate the optimal value of capacitance for CMR by calculation. Usually, the impedance equation of lossless TL is given by the following equation.

$$Z_{\rm in} = Z_0 \frac{Z_{\rm L} + jZ_0 \tan\beta\ell}{Z_0 + jZ_{\rm L} \tan\beta\ell} \tag{1}$$

where $Z_{\rm L}$ is the load impedance, Z_0 is the characteristic impedance of TL, β is the phase constant, and ℓ is the length of TL. Moreover, Eq. (1) is transformed because $Z_{\rm L}$ is equal to $1/j\omega C$.

$$\begin{aligned} Z_{\rm in} &= Z_0 \frac{\frac{1}{j\omega C} + jZ_0 \tan\beta\ell}{Z_0 + j\frac{1}{j\omega C} \tan\beta\ell} \\ \Longleftrightarrow C &= \frac{1}{\omega Z_0 \tan\beta\ell} \end{aligned}$$

In this work, we use the same transmission line of [2]. Thus we can calculate the optimal capacitance value to reduce shunt impedance for common-mode signal. In this work, the setting values are as follows. $Z_0 = 50\,[\Omega], \beta = 2.48\,[\mathrm{rad/mm}], \omega = 2\pi \times 60\,[\mathrm{GHz}], \ell = 140\,[\mu\mathrm{m}]$. ℓ means the length of shunt TL of the 1st stage. Therefore we can estimate the optimal value of capacitance is about 147 fF for the 1st stage.

Fig. 4 shows the change of shunt impedance and input impedance. Using the proposed technique, shunt impedance becomes almost zero for common-mode signal because of LC peaking. The right graph shows the input impedance. Owing to LC peaking, the length of shunt TL is seemed to be reduced and short stub is realized instead of open stub. Thus input impedance is shifted to inductance area on smith chart. This technique makes it possible to adjust common-mode characteristic only on the smith chart.

Fig. 5 shows the simulation result of CMRR. From this figure, it is found that impedance matching shift for common-mode is clearly effective for CMRR. To validate this technique, we designed the 2-stage differential amplifier using a 65 nm CMOS process.

IV. Measurement Results

Fig. 6 shows the schematic of 2-stage differential amplifier using the proposed technique. This technique is used every stage. We need very small capacitor such as 12 fF for the 2nd stage because ℓ is equal to 540 μm, however it is difficult to design such a small capacitance. Thus we use open stub, which works like a capacitance.

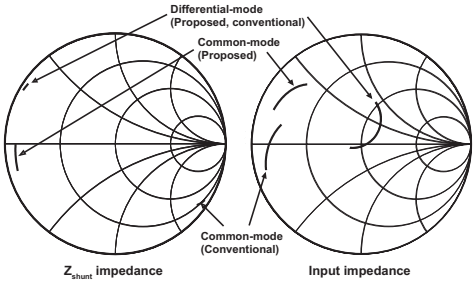

Fig. 4. Comparison of conventional and proposed methods.

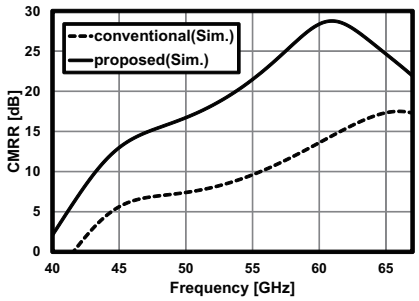

Fig. 5. The effect of proposed method.

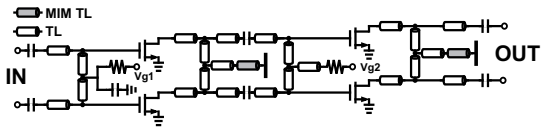

Fig. 6. The 2-stage differential amplifier using the high CMRR technique.

TABLE I
PERFORMANCE COMPARISON.

	Technology	Power Gain[dB]	P_{1dB}[dBm]	P_{sat}[dBm]	Peak PAE[%]	CMRR[dB]	Power[mW]	Stage	V_{DD}[V]
[3]	65 nm	23.2	10.0	14.6	16.3	11.8	135	3	1.2
This Work	65 nm	12.1	4.52	9.0	11.1	**26**	45.8	2	1.0

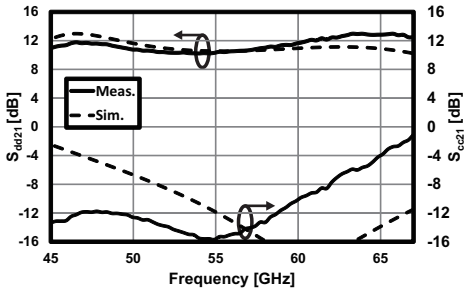

Fig. 7. Transfer characteristic.

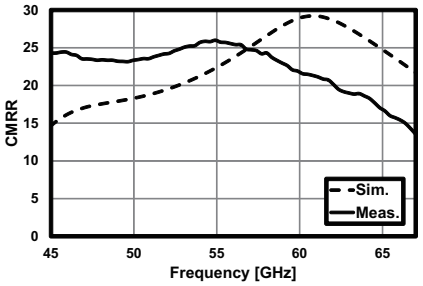

Fig. 8. Common-mode rejection ratio.

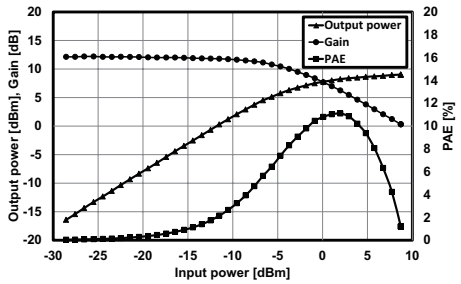

Fig. 9. Large signal characteristic.

In this figure, MIM TL means decoupling. This is the TL which is placed MIM capacitor around signal line and realize low characteristic impedance.

Fig. 7 shows the transfer characteristic. The solid line is measurement and dotted line is simulation. It achieves a 12.1 dB gain at 60 GHz and suppresses the common-mode by -8 dB. Moreover, very wide band gain flatness can be acheived. 3-dB bandwidth is 23 GHz.

Fig. 8 shows the CMRR. It achieves 26 dB CMRR. Comparing to the simulation result, measurement peak of CMRR is slightly shifted from 60 GHz. This is because the actual value of capacitance became large comparing to the design value. At 60 GHz, so many parasitic capacitance should be considered and it is difficult to consider all of them. Thus we need to improve the accuracy of models, such as capacitance, and TL. Fig. 9 shows the power gain, output power, and PAE. It achieves a power gain of 12.1 dB, a $P_{\rm sat}$ of 9.0 dBm, and a peak PAE of 11.1 %. Fig. 10 shows the die photo of the chip. The chip area is 815 μm$\times$750 μm.

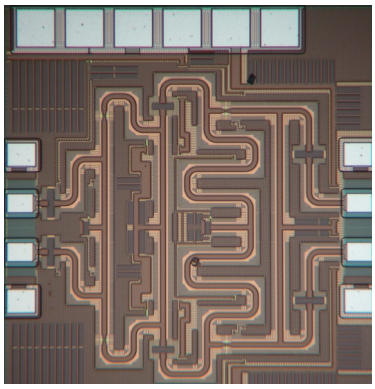

Fig. 10. Chip photograph.

V. CONCLUSION

In this work, the technique of high CMRR for 60 GHz differential amplifier is presented. Moreover, the effect of this technique is investigated by using 2-stage differential amplifier in 65 nm CMOS process. As a result, it achieves a power gain of 12.1 dB, a $P_{\rm sat}$ of 9.0 dBm, a peak PAE of 11.1 %, a power consumption of 45.8 mW , and a CMRR of 26 dB at 60 GHz, which is better than the conventional research.

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