A 20 GHz Push-Push Voltage-Controlled Oscillator for a 60 GHz Frequency Synthesizer

Teerachot Siriburanon, Takahiro Sato, Ahmed Musa, Wei Deng, Kenichi Okada, and Akira Matsuzawa

Department of Physical Electronics, Tokyo Institute of Technology,
2-12-1-S3-27, Ookayama, Meguro-ku, Tokyo, 152-8552, Japan
tee@ssc.pe.titech.ac.jp

***Abstract* — This paper proposes a push-push 20 GHz VCO realized by a 10 GHz QVCO for a quadrature 60GHz Local Oscillator. The proposed VCO is implemented in a 65nm CMOS process. It achieves tuning range of 3.0 GHz from 16.3 to 19.3 GHz with a phase noise of –105 dBc/Hz at 1MHz offset. The power consumption of core oscillators is 7.5 mW and an FoM of -182 dBc/Hz is achieved.**

***Index Terms* —CMOS, injection locking, low phase noise, low power, tail-current modulation, Impulse sensitivity function, Push-push voltage-controlled oscillator.**

I. Introduction

To cope up with demands for data-hungry applications, utilizing 57 – 66 GHz millimeter-wave unlicensed bandwidth is one of the most attractive solutions, as it can provide high-speed short-range data communication. Recently, an 11-Gb/s wireless communication has been achieved using a 60 GHz CMOS direct-conversion transceiver for the IEEE802.15.3c [1]. In the design of RF front-ends of the above architecture, a low-power 60 GHz local oscillator (LO) with quadrature outputs is necessary. More importantly, a phase noise of at least -90 dBc/Hz is required for a 60 GHz frequency synthesizer utilizing a 16QAM modulation scheme [1]-[2].

A number of publications for quadrature 60 GHz LO have already been proposed. Typical methods to generate 60GHz quadrature signals are summarized in Fig. 1. The author in [3] proposes a direct 60 GHz quadrature voltage-controlled oscillator (QVCO) oscillating at its fundamental frequency as shown in Fig. 1(a). Unfortunately, the degradation of quality factor of varactor at 60 GHz limits low phase noise performance. An alternative solution shown in Fig. 1(b) is proposed by utilizing a 30 GHz differential VCO in a push-push operation to generate 60 GHz signal followed by a polyphase filter to generate 90° phase difference outputs [4]. However, this technique has undesirably large I/Q mismatch due to the use of polyphase filter. Because of its better phase noise performance, the approach in [5] is more preferable, in which a sub-harmonic 20 GHz PLL is used to inject a super-harmonic 60 GHz quadrature Injection Locked Oscillator (ILO). One of the problems of this approach relates to reliability over process - voltage - temperature (PVT) variations. A calibration of ILOs in 60 GHz frequency synthesizer has recently been implemented in [6].

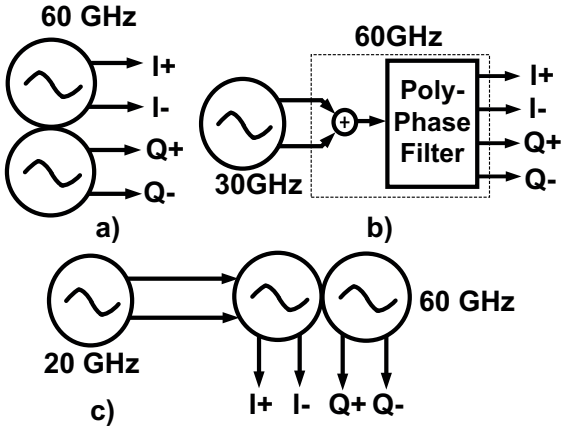

Fig. 1. Conventional approaches for 60 GHz Quadrature LO. (a) 60 GHz QVCO (b) push-push 30 GHz VCO + polyphase filter, (c) 20 GHz sub-harmonic VCO + QILO

According to [7], parasitic capacitances are more influential on the performance of VCO at higher frequency. For a given technology, the best overall quality factor of oscillator tank falls in the range of 5 – 15 GHz as shown in Fig. 2. Therefore, a novel approach for a 60 GHz LO generation is proposed in Fig. 3 using a push-push 20 GHz VCO as a sub-harmonic VCO. Differential phase of I and Q 10 GHz oscillators are connected in a push-push configuration to cancel the first harmonic and enhance second harmonic (20 GHz) component.

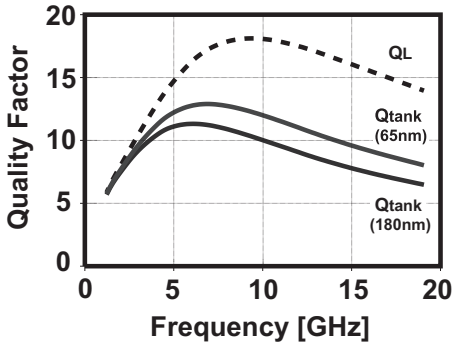

Fig. 2. Overall quality factors of tank for 65nm and 180nm CMOS technology presented in [7]

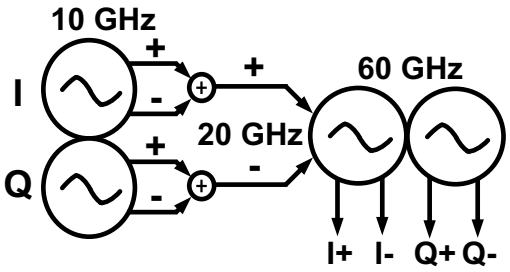

Fig. 3. Proposed 60 GHz Quadrature LO using a 20 GHz push-push VCO and QILO

As a result, a differential 20 GHz VCO is obtained. The phase noise of 20 GHz is 6 dB higher than phase noise of 10 GHz QVCO according to the injection locked characteristics. Since the main oscillators (10 GHz QVCO) operate in the desired frequency range where quality factor of tank is maximum, an improvement in phase noise can be expected. Alternatively, higher quality factor of overall tank can maintain same phase noise at lower power consumption.

II. Circuit Implementation

The proposed schematic of 20 GHz VCO is shown in Fig. 4 which is composed of two 10 GHz VCOs, 20 GHz resonator and cross coupling transistors. Two 10 GHz LC-VCOs are designed using NMOS cross-coupled architecture as shown in the top portion of Fig. 4. PDK inductors with an inductance of 650 pH and a quality factor of 15.7 are utilized. 3-bit capacitor bank and a varactor are implemented in both VCOs for wide tuning range. The common nodes of each oscillator (node X and Y) are forced by cross-coupling transistors to have 180° phase different. As a result, 10 GHz VCOs are superharmonically coupled and operate as a QVCO.

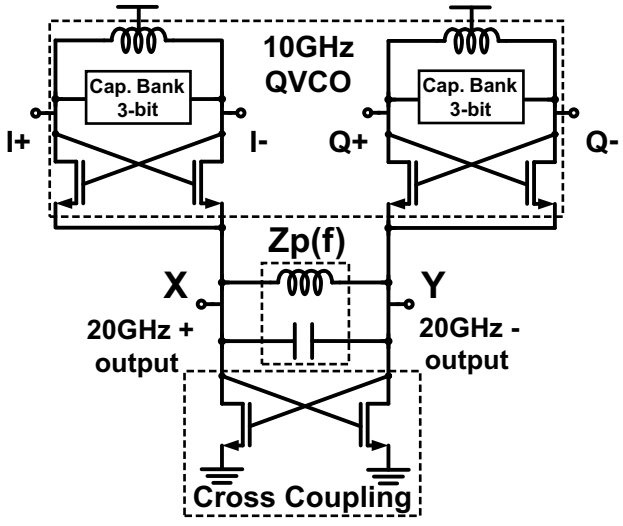

Fig. 4. Schematic of proposed 20 GHz VCO

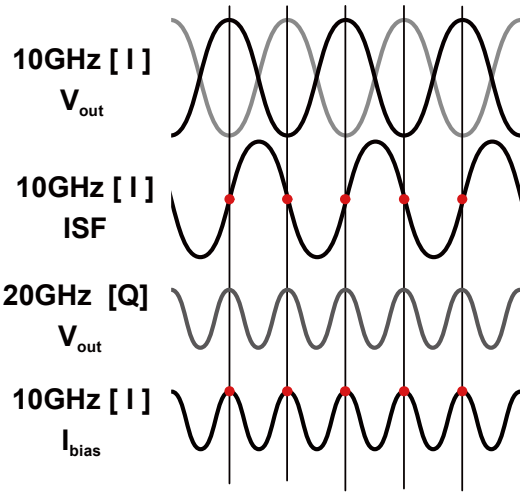

Fig. 5. Tail current modulation as an effect of cross-coupling transistor and a bottom LC resonator

The second component is the resonator which is composed of an inductor and 2-bit capacitor bank. The impedance of this resonator $Z_p(f)$ can be manually tuned to provide high impedance at the second harmonic of the main QVCO throughout the tuning range. As a result, this attenuates the first harmonic components and enhances the second harmonic output at node X and Y. In addition to an enhancement in gain, an improvement in phase noise can be achieved from second harmonic resonator since it acts like a tail filtering [8]. Two-bit capacitor bank and a varactor are adopted for an ability to tune the impedance. In this design, an inductance of 330 pH with a quality factor of 7.9 is used for the second harmonic resonator. Two common source stages are provided as buffers for 20 GHz output.

As proposed in [9], tail feedback is used to lower the phase noise by modulating the tail current. Similarly, this technique has the same characteristic as shown in Fig. 5. In this figure, the first waveform shows the output of main oscillator at 10 GHz. The second waveform shows its approximated impulse sensitivity function (ISF). The third waveform shows 20 GHz output waveform. The last waveform shows the tail current modulation due to the effect of cross-coupling transistors. The tail current is maximized during the period where the amplitude ISF is at its minimum and minimized when it is at maximum. Consequently, this technique can improve phase noise.

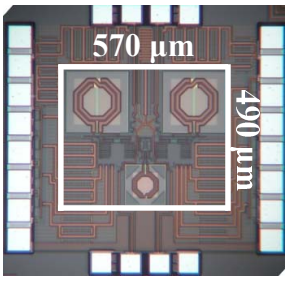

Fig. 6. Chip micrograph of the proposed VCO

TABLE I
PERFORMANCE COMPARISON

	Features	CMOS Tech.	Frequency [GHz]	Phase noise [dBc/Hz]	Power [mW]	FoM [dBc/Hz]	Output type
[3]	QVCO@60GHz	45nm	57-66	-75@1MHz	78	-	Quad.
[4]	Push-push VCO@30GHz + Polyphase filter	90nm	59.6-64	-73@1MHz	76	-	Quad.
[5]	VCO@20GHz	65nm	17.9-21.2	-106@1MHz	19	-179	Diff.
	Sub-harmonic Injection	65nm	58-63	-96@1MHz	80	-	Quad.
This work	Push-push VCO@10GHz	65nm	16.3-19.3	-105@1MHz	7.5	-182	Diff.
	Sub-harmonic Injection (based on calculation)	65nm	48.6-57.9	-95@1MHz	-	-	Quad.

III. MEASUREMENT RESULTS

The proposed 20 GHz VCO is implemented in a standard 65nm CMOS process. The microphotograph of the fabricated VCO is shown in Fig. 6. The total chip area is 570μm x 490 μm. The phase noise is evaluated using Agilent E5052B SSA signal source analyzer. As shown in Fig. 7, the measured phase noise at 19.1 GHz is -105 dBc/Hz@1MHz offset and FoM of -182 is achieved. Due to unaccounted layout parasitics and inaccuracy in modeling, the measured tuning range is from 16.3 GHz to 19.3 GHz. Even though the tuning range is wide enough, the measured tuning range cannot cover 7 GHz bandwidth around 60 GHz. For 1.0-V supply, an output power of -38 dBm is observed.

Table I compares the calculated performance of the proposed VCO for a 60 GHz LO generation with other state-of-the-art 60 GHz frequency synthesizer [3]-[5]. The normalized phase noise can be calculated by:

$$PN_{ILO} = PN_{OSC} + 20\log_{10}(N) \quad (1)$$

where N = 3 for a tripler 60 GHz ILO. By comparison with other publications, the phase noise of this work satisfies the requirement for 16QAM and considerably more than those in [3]-[4]. Comparing with [5], this work reduces power consumption of 20 GHz VCO from 19 mW to 7.5 mW.

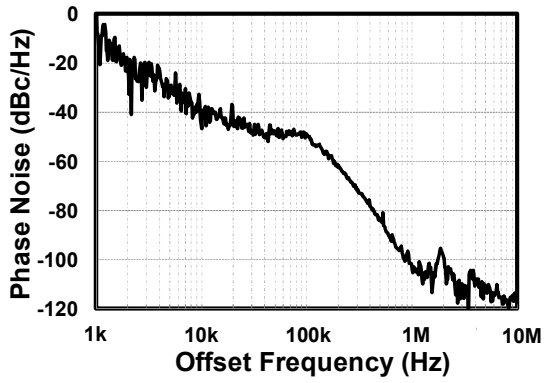

Fig. 7. Measured phase noise at 19.1 GHz

IV. CONCLUSION

By utilizing a combination of 10 GHz QVCO for 20 GHz push-push operation as a subharmonic VCO and a super-harmonic QILO [5], it shows a capability of maintaining low phase noise with a 14% reduction in power consumption of the previously-implemented 60GHz LO [5].

ACKNOWLEDGEMENT

This work was partially supported by MIC, SCOPE, MEXT, STARC, NEDO, Canon Foundation, and VDEC in collaboration with Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd.

REFERENCES

[1] K. Okada, *et al.*, "A 60-GHz 16QAM/8PSK/QPSK/BPSK Direct-Conversion Transceiver for IEEE802.15.3c," *IEEE Journal of Solid-State Circuits*, vol.46, no.12, pp.2988-3004, Dec. 2011.

[2] B. A. Floyd, "A 16–18.8-GHz Sub-Integer-N Frequency Synthesizer for 60-GHz Transceivers," *IEEE Journal of Solid-State Circuits,* vol.43, no.5, pp.1076-1086, May 2008

[3] K. Scheir, G. Vandersteen, Y. Rolain, and P. Wambacq, "A 57-to-66GHz Quadrature PLL in 45nm Digital CMOS," *IEEE ISSCC, Digest of Tech. Papers*, pp. 494–495, Feb. 2009.

[4] C. Marcu, *et al.*, "A 90 nm CMOS Low-Power 60 GHz Transceiver With Integrated Baseband Circuitry," *IEEE J. Solid-State Circuits*, vol. 44, no.12, pp.3434–3447, Dec. 2009.

[5] A. Musa, *et al*., "A Low Phase Noise Quadrature Injection Locked Frequency Synthesizer for MM-Wave Applications," *IEEE J.Solid-StateCir.*,vol.46, no.11,pp.2635-2649,Nov. 2011.

[6] W. Deng, T. Siriburanon, A. Musa, K. Okada and A. Matsuzawa, "A 58.1-to-65.0GHz Frequency Synthesizer with Background Calibration for Millimeter-wave TDD Transceivers," *IEEE European Solid-State Circuits Conference* (*ESSCIRC),* pp. 201-204, Sep. 2012.

[7] Rui Murakami, *et al.,* "Design Optimization of Voltage Controlled Oscillators in Consideration of Parasitic Capacitance" *IEEE MWSCAS*, Mexico, Aug. 2009.

[8] E. Hegazi, *et al.,* "The Designer's Guide to High-Purity Oscillators", *1st ed. New York: Springer*, 2004.

[9] S. Hara, *et al.,* "A 9.3 MHz to 5.7 GHz tunable LC-based VCO using a divide-by-N injection-locked frequency divider," in *Proc. 2009 IEEE A-SSCC.*, 2009, pp. 81–84.