



A 0.7 V-to-1.0 V 10.1 dBm-to-13.2 dBm 60-GHz Power Amplifier Using Digitally-Assisted LDO Considering HCI Issues

<u>Rui Wu</u>, Yuuki Tsukui, Ryo Minami, Kenichi Okada, and Akira Matsuzawa

Tokyo Institute of Technology, Japan





Outline

- Background
- 60-GHz field is attractive
- Hot-Carrier-Induced Issues
- HCI influence on circuit reliability
- Variable-Supply-Voltage PA using Digitally-assisted LDO
- Circuit design & Measurement results
- Conclusions

Background

- 9-GHz unlicensed bandwidth
- Several Gbps wireless communication e.g. IEEE 802.15.3c QPSK→3.5 Gbps/ch

16QAM→7 Gbps/ch





HCI Issues are Emerging at 60 GHz

60-GHz power amplifier

Ţ Ţ Ţ Standard

High f_{max}, suitable for 60-GHz amplifier

8 Bad HCI performance

2.4-GHz power amplifier



Good HCI performance
 Low f_{max}, can't be used
 for 60-GHz amplifier

Hot-Carrier-Induced (HCI) Effects



Degrade V_{th} , g_m , drain current, and lifetime

65 nm NMOSFET DC Stress Lifetime



[2] E. Takeda et al., IEDL 1983

65 nm NMOSFET RF Stress Lifetime



[3] L. Negre et al., JSSC 2012

Hot-Carrier Damage Mechanism [4]

- Single Vibrational Excitation (SVE) is related to high energetic carrier that has enough energy to break Si-H bond; (High energy)
- <u>Electron Electron Scattering (EES)</u> is caused by one carrier promotes the other into higher energy and allows Si-H breaking; (Medium energy)
- <u>Multiple Vibrational Excitation (MVE</u>) is due to a series of low energetic carriers that accumulate enough energy to break Si-H bond. (Low energy)

Hot-Carrier Physical Model [3]

$$\Delta I_{DSat}(t) = A(t) \cdot t^{n} = \left[\int_{0}^{t} A(\tau)^{\frac{1}{n}} d\tau\right]^{n}$$

$$A(t) = \left[K_{SVE} \left(\frac{I_{DS}(t)}{W}\right)^{\alpha_{1}} \left(\frac{I_{BS}(t)}{I_{DS}(t)}\right)^{m} + K_{EES} \left(\frac{I_{DS}(t)}{W}\right)^{\alpha_{2}} \left(\frac{I_{BS}(t)}{I_{DS}(t)}\right)^{m} + K_{MVE} V_{DS}^{\frac{\alpha_{3}}{2}}(t) \left(\frac{I_{DS}(t)}{W}\right)^{\alpha_{3}} exp(\frac{-E_{emi}}{kT})]^{n}$$

 $I_{DS}(t)$ is the time-varying drain current which is a function of $V_{GS}(t)$ and $V_{DS}(t)$;

K and α are damage mode dependent constants; m and n are process-related constants.

[3] L. Negre et al., JSSC 2012

Conventional Solutions



😊 Better lifetime

Begraded output power, efficiency, and linearity

[5] A. Siligaris et al., JSSC 2010[6] M. Tanomura et al., ISSCC 2008

Power combining [7]



Better lifetime, output power, and linearity
Sensitive to process variations

[7] J. Chen et al., ISSCC 2011 9

Application Scenario

S	ingle Carrier (SC) Mode o	f IEEE 802.	15.3c		
L	Mod 1+MCS 8	Mod 1+MCS 7 & Mod 2+MCS 8	1 Moc 3 Moc	od1 low power od2 high power		
0	0.56	m ć	lm d			
	MCS identifier	8	3	1		
	Data rate	2640	Mb/s	412 Mb/s		
	Rx sensitivity	-56 dBm		-61 dBm		
	Required CNR	17.5	5 dB	12.5 dB		
	Distance	0.56 m	1 m	1 m		
	Required P _{out}	5 dBm	10 dBm	5 dBm		

*NF=8 dB; Thermal noise=-81.5 dBm; Antenna gain=2 dBi; Implementation loss=-2 dB; freq.=60 GHz

Lifetime estimation



Time-Division Duplex (TDD) Operation

• TDD operation can eliminate the stringent requirement of filtering and extend the available bandwidth for transceivers.



is indicated to be 3μ s

The Proposed Power Amplifier



Transient Operation of the LDO



Transient Simulation Result



Differential PA Topology



The cross-coupling capacitor technique is adopted to improve the stability and power gain

Die Micro-photograph



Measured Small-Signal S-parameter



PA Performance vs V_{PA}@60 GHz



Measured Lifetime of the PA



Measured Output Spectrum



Spectrum centered at 62.64 GHz for QPSK modulation (a) V_{PA} =1.0 V, P_{out} =4 dBm; (b) V_{PA} =0.7 V, P_{out} =3 dBm

Measured EVM for QPSK Modualtion



60 GHz CMOS PA Performance Comparison

Ref.	Process	Vdd (V)	P _{1dB} (dBm)	P _{sat} (dBm)	PAE _{max} (%)	Lifetime (year)
	65 nm <u>SOI</u>	1.2	7.1	10.5	22.3	N/A
[5]		1.8	12.7	14.5	25.7	
		2.6	15.2	16.5	18.2	
[6]	90 nm	0.7	5.2	8.5	7.0	> 10 ⁵ *
[0]		1.0	10.5	11.5	8.5	> 10*
[7]	65 nm	1.0	15.0	18.6	15.1	N/A
[8]	65 nm	1.0	8.0	11.5	15.2	> 10*
This	65 nm	0.7 [†]	5.8	10.1	8.1	> 10 ²
work		1.0 [†]	10.2	13.2	15.0	> 0.2

[†] Only for the last stage V_{PA}

* Non-measured results

[5] A. Siligaris et. al, JSSC 2010[7] J. Chen et. al, ISSCC 2011

[6] M. Tanomura et. al, ISSCC 2008

23

[8] W. L. Chan et. al, JSSC 2010

 The lifetime of the proposed PA can be improved dramatically by dynamic operation.

 The tunable supply offers a possibility to meet different linearity, efficiency, output power and lifetime requirements in actual applications.

 The PA is insensitive to the process variations thanks to the tunable supply voltage.

Thank you for your attention!

Output Power Distribution [5]



[5] A. Siligaris et. al, JSSC 2010

Transistor Measurement Data



[9] Q. Bu et. al, SSDM 2012

Power Consumption

V_{PA}	Digital	Analog	I _{PA}
1.0 V	64 μA	312 μA	130 mA
0.7 V	64 μA	312 μA	120 mA

Lifetime Improvement of the PA



The Flow Chart of Dynamic Operation



Spectrum Measurement Setup



EVM Measurement Setup



Dynamic Comparator Schematic [9]



[9] M. Miyahara et. al, ASSCC 2008

•
$$V_{eff} = V_0 + V_{DS} - V_{dsat}$$

• $V_{dsat} = \frac{2(V_{GS} - V_{tat})/m}{1 + \sqrt{1 + \frac{2(V_{GS} - V_{tat})}{mE_cL}}}$

V_{eff} is the effective potential from the drain to channel pinch-off point;

 V_0 is a halo-based potential, E_c is the critical field for velocity saturation, and m is a coefficient related to the body effect. V_{GS} increases, I_{DS} and V_{dsat} increase which leads to V_{eff} decrease.

65 nm NMOSFET DC Stress Lifetime



65 nm NMOSFET RF Stress Lifetime



CMOS PA Performance Comparison

Ref.	Process	Freq. (GHz)	Vdd (V)	P _{1dB} (dBm)	P _{sat} (dBm)	PAE _{max} (%)
	05	60	1.2	7.1	10.5	22.3
[5]	SOI		1.8	12.7	14.5	25.7
	<u>501</u>		2.6	15.2	16.5	18.2
[6]	90 nm	60	0.7	5.2	8.5	7.0
[[0]			1.0	10.5	11.5	8.5
[7]	65 nm	60	1.0	15.0	18.6	15.1
[8]	65 nm	60	1.0	8.0	11.5	15.2
This	65 nm	60	0.7 [†]	5.8	10.1	8.1
work			1.0 ⁺	10.2	13.2	15.0

⁺ Only for the last stage V_{PA}

[5] A. Siligaris et. al, JSSC 2010[7] J. Chen et. al, ISSCC 2011

[6] M. Tanomura et. al, ISSCC 2008

38

[8] W. L. Chan et. al, JSSC 2010

CMOS PA Performance Comparison

Ref.	Process	Vdd (V)	P _{1dB} (dBm)	P _{sat} (dBm)	PAE _{max} (%)	Lifetime (year)
		1.2	7.1	10.5	22.3	N/A
[5]	65 nm SOI	1.8	12.7	14.5	25.7	
		2.6	15.2	16.5	18.2	
[6]	00 nm	0.7	5.2	8.5	7.0	> 10 ⁵ *
[[0]	90 mm	1.0	10.5	11.5	8.5	> 10*
[7]	65 nm	1.0	15.0	18.6	15.1	N/A
[8]	65 nm	1.0	8.0	11.5	15.2	> 10*
This	65 nm	0.7 [†]	5.8	10.1	8.1	> 10 ²
work		1.0 [†]	10.2	13.2	15.0	> 0.2

^{\dagger} Only for the last stage V_{PA}

* Estimation results

[5] A. Siligaris et. al, JSSC 2010[7] J. Chen et. al, ISSCC 2011

[6] M. Tanomura et. al, ISSCC 2008

[8] W. L. Chan et. al, JSSC 2010