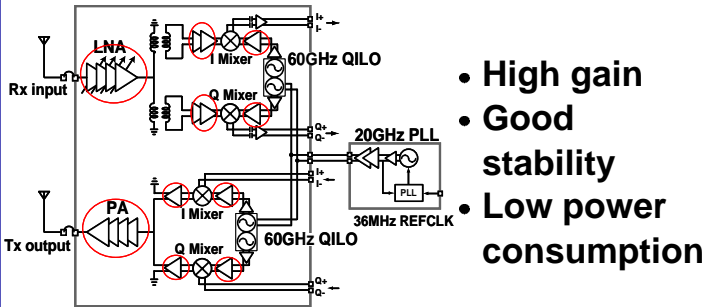
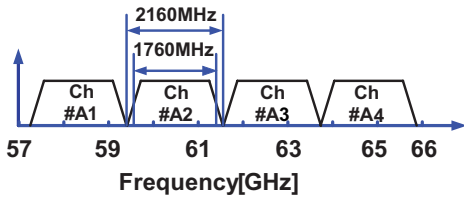


Analysis of Cascode Structure for 60GHz Amplifier Design in 65nm CMOS

Qinghong Bu, Ning Li, Hiroki Asada, Kenichi Okada and Akira Matsuzawa
Matsuzawa and Okada Laboratory, Tokyo Institute of Technology, Japan

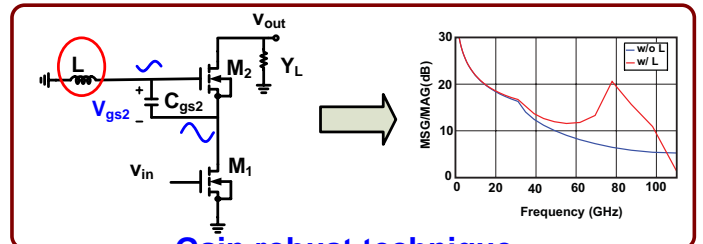
1 Background

- IEEE 802.15.3c specification
 - 9 GHz unlicensed bandwidth
 - 2.16 GHz/ch
 - Several Gbps data transfer
 - QPSK \Rightarrow 3.5 Gbps
 - 16QAM \Rightarrow 7 Gbps

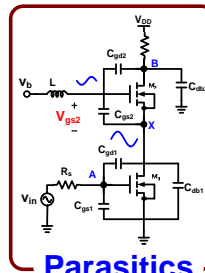


2 Cascode structure at mmW frequency

- Cascode structure at mmW frequency, a reduction of the reverse isolation S_{12} .
- ☺ Increase MSG
- ☺ Large K
- ☹ Larger parasitic capacitance

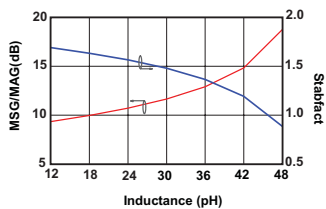


Gain robust technique

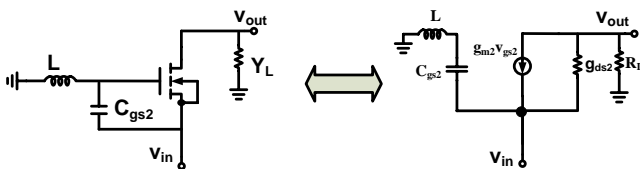


- A double zero and a double pole are added when using L
- The pole frequency is much lower than the zero frequency.
- At 60 GHz, only the poles have a significant effect.

3 Inductance optimization



- The trade-off between G_{max} and stability factor
- Inductance has to be optimized reasonably



$$A_v = -\frac{\frac{g_{m2}}{1 - \omega^2 LC_{gs2}} + g_{ds2}}{Y_L + g_{ds2}} \Rightarrow L = \frac{1}{\omega^2 C_{gs2}}$$

Gain calculation

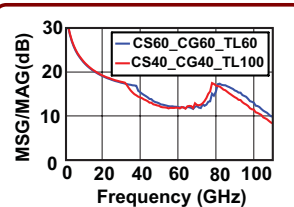
$$K = \frac{2g_{m2}(\frac{Y_L}{g_{ds2}} + 1) + 2(Y_L + g_{ds2})}{g_{m2} - g_{ds2}(1 - \omega^2 L C_{gs2})} - 1 > 1 \Rightarrow L = \frac{1 - \frac{g_{m2} Y_L}{(2Y_L + g_{ds2}) g_{ds2}}}{\omega^2 C_{gs2}}$$

Satibility calculation

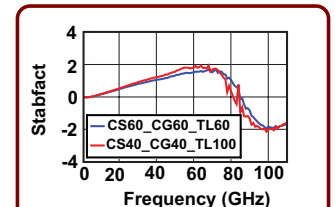
4 Measurement results

- Two cascode structure TEGs with difference sizes in 65 nm CMOS
- TLs which have about 0.3 pH per μm are utilized as inductance

- CS $W_f = 20 \times 2 \mu\text{m}$ ($N_f = 20$)
- CG $W_f = 20 \times 2 \mu\text{m}$ ($N_f = 20$)
- TL 100 μm
- CS $W_f = 30 \times 2 \mu\text{m}$ ($N_f = 20$)
- CG $W_f = 30 \times 2 \mu\text{m}$ ($N_f = 20$)
- TL 60 μm



Maximum gain



Stability factor

5 Conclusion

- The measurement results proved that the required inductance is inversely proportional to the transistor size
- The inductance can be optimized according to the theoretical equation