Analysis of Cascode Structure for 60GHz Amplifier Design in 65nm CMOS

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1. Introduction

The license free 60GHz radios with 9GHz bandwidth have a big attraction both in academia and in industry. Multi-Gbps wireless communication of 60GHz transceivers have been reported recently [1]. Although RF front-end amplifiers are implemented at low noise amplifiers and power amplifiers with different specifications due to the different functions they perform, sufficient gain and low power consumption are the general requirement. For the design consideration, the active device structure and models should be optimized at 60 GHz.

In recently reported papers, common source (CS) transistors are usually used for the amplifiers in 60GHz transceiver. A single CS stage cannot provide sufficient gain, so several cascaded stages are required to enhance the gain performance. The inter-stage matching network and the circuit stability become difficult.

Cascode structure is widely used in analog circuits for its high gain. Although at mm-wave frequency, cascode transistors have a larger parasitic capacitance which shorts the small signal current and reduce the gain. The good isolation between input and output of this structure is still attractive in mm-wave amplifier design. Also they can be made unconditionally stable at the operating frequency, making the design more robust and simplify network [2].

In this paper, a gain robust cascode structure which uses a transmission line (TL) at the gate of the common gate transistor will be analyzed.

2. Analysis of gain robust cascode structure

2.1 Gain robust analysis

Consider the small-signal voltage gain of the gain robust cascode structure using a model as shown in Fig. 1. Applying Miller's theorem on $C_{gd1,}$ new equivalent capacitance values can be combined at the gate source node and drain source node. In common gate (CG) transistor, there is no Miller multiplication of capacitances; the C_{gd2} has little effort to the whole voltage gain of cascode structure. The small-signal model of cascode circuit can be simplified as Fig. 1(b), where C_{GS1} represents the combination value of C_{gs1} and the value coming from C_{gd1}, Y_{ds1} is the combination value of g_{ds1}, C_{ds1} and the value coming from C_{gd1}, Y_{ds2} represents the combination value of g_{ds2}, C_{gd2}. Relating the voltage-current relationship in the circuit and apply Kirochoff's current law at note X, the voltage gain of the cascode structure can be expressed as

$$A_v = -\frac{g_{m1}}{Y_L + \dfrac{Y_{ds1}(Y_L + Y_{ds2})(1-\omega^2 L_{TL}C_{gs2}) + j\omega C_{gs2}(Y_L + Y_{ds2})}{g_{m2} + Y_{ds2}(1-\omega^2 L_{TL}C_{gs2})}}$$

To simplify the problem, assume that $g_{ds1} = g_{ds2}$, $C_{ds1} = C_{ds2}$. Because of $Y_{ds1} = g_{ds1} + j\omega(C_{ds1} + C'_{gd1})$, $Y_{ds2} = g_{ds2} + j\omega C_{ds2}$, $Y_{ds1} > Y_{ds2}$. In a 65nm CMOS process, C_{gs2} is about dozens of femtofarad (fF). 100 μm Micro-strip transmission line (MSTL) [3] which used in this paper is about several picohenry (pH), so $1-\omega^2 L_{TL}C_{GS2} < 1$. From the above equation, the rough estimation is that, the voltage gain become bigger than that $1-\omega^2 L_{TL}C_{GS2} = 1$ when there is no TL.

In the analysis, a TL added at the gate of CG transistor can improve the voltage gain. The inductance L_{TL} of TL is inversely proportional to G_{GS2} and ω^2. Specially, the exact value can be obtained from $1-\omega^2 L_{TL}C_{GS2} = 0$ if the operating frequency and G_{gs2} is given.

In a 65nm CMOS process, C_{gs2} is about dozens of femtofarad (fF). For comparison, three cascode-transistor TEGs are taped out. Two of them are 20-figure CS and 20-figure CG transistors (each with 2 μm unite figure length) with 60 μm and 100 μm TLs. One is 30-figure CS and 30-figure CG transistors (each with 2 μm unit figure length) with 60 μm TL.

2.2 Transistor layout consideration

Fig. 2 shows the schematic of the proposed cascode structure. MSTL is added in the CG transistor. De-coupling MIM capacitors and two 5 kilo-ohm resistors are used for AC ground and DC bias.

In conventional cascode structure layout, the CS transistor and CG transistor body terminals are tied to the bulk ground which makes the layout of cascode device (Fig. 3(a)) simply and compact. However the effort between devices in the same bulk substrate will reduce the performance of the whole structure. Also the body effect increases the threshold voltage V_{TH} of the CG transistor which decreases the gain of a cascode structure. In order to circumvent this issue, the body terminal of CG tired its own source terminal and deep wells are used in both CG and CS as shown in the side view of cascode structure in Fig. 3(b).

3. Measurement results

The measurement results of the cascode TEGs are shown in Fig. 4. The maximum available gain is shown in Fig. 4(a). It is observed that the 20-figure CS and

20-figure CG transistors with 100 μm MSTL exhibits 12 dB MSG at 60GHz, which is much higher than the 20-figure CS and 20-figure CG transistors with 60 μm MSTL. The 30-figure CS and 30-figure CG transistors with 60 μm MSTL also exhibits a high gain as well as the 20-figure CS and 20-figure CG transistors with 100 μm MSTL. Fig. 4(b) and Fig. 4(c) show the measurement results of the stability factor and reverse isolation separately. At 60 GHz, all the TEGs are unconditional stability and the reverse isolation is about -30dB.

4. Conclusion

After analysis the voltage gain of cascode structure, a transmission line (TL) at the gate of the CG transistor in cascode can improve the gain obviously. There cascode TEGs are taped out for comparison. The measurement results show that, the variation tendency of cascode TEGs' maximum available is in accord with the analysis. Above 12dB MSG is obtained at 60GHz using the gain robust method. And all the TEGs are unconditional stability and reverse isolation are about -30dB at 60GHz.

Acknowledgements

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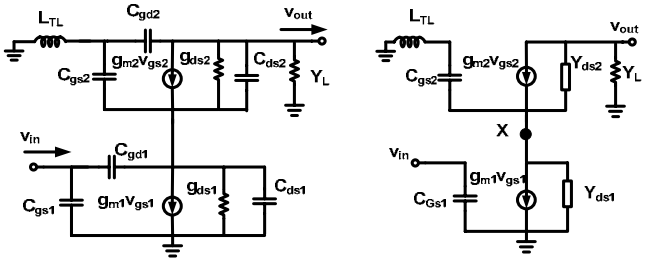


(a) (b)

Fig. 1 (a) Small-signal model of cascode structure. (b) Simplified small-signal model of cascode structure

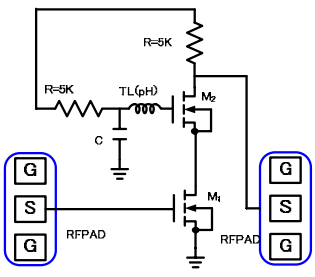
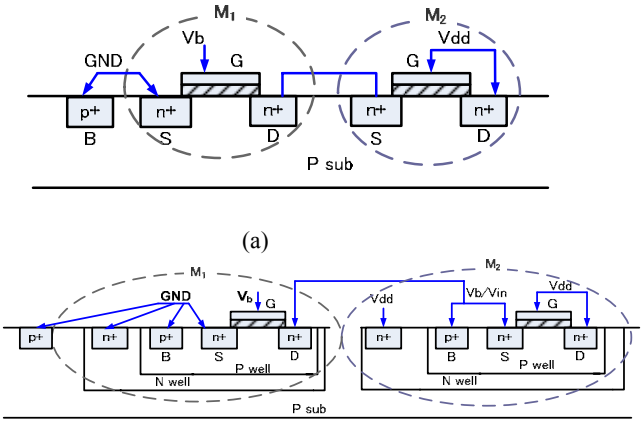


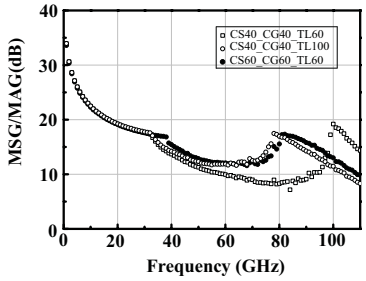
Fig. 2 Schematic of proposed cascode structure



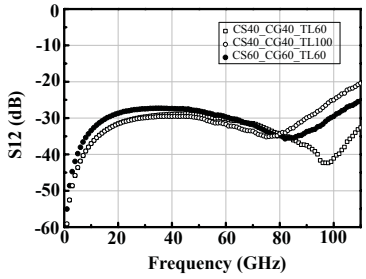
(a)

(b)

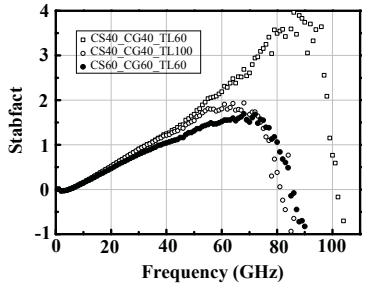
Fig. 3 (a) Conventional layout of cascode structure. (b) Deep n-well used cascode structure.



(a)



(b)



(c)

Fig. 4 Measure results of casocde TEG. (a) MSG/MAG. (b) Reverse isolation S_{12}. (c) Stability factor.

References

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