A 83-dB SFDR 10-MHz Bandwidth Continuous-Time Delta-Sigma Modulator Employing a One-Element-Shifting Dynamic Element Matching

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Matsuzawa & Okada Lab.

Outline

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- Background
- Proposed one-element-shifting (OES) DEM method
- Implementation and measurement results
- Conclusion

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- **Conclusion**

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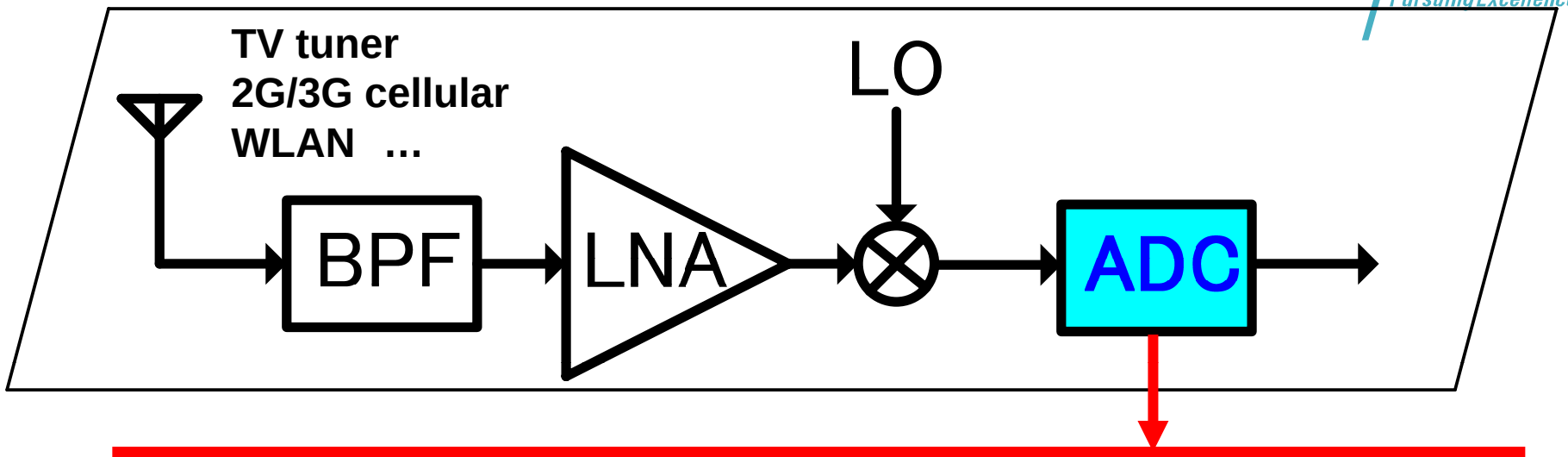
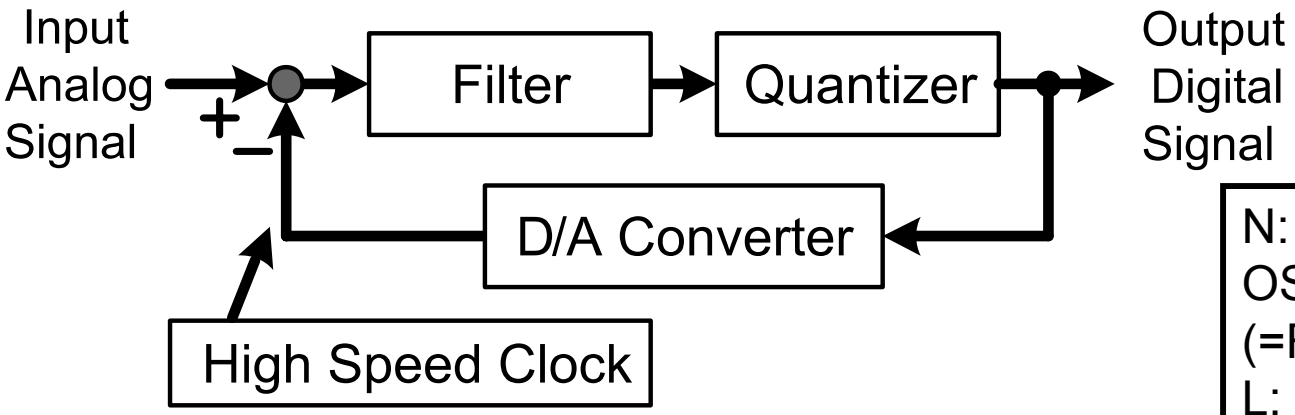
Receiver architecture



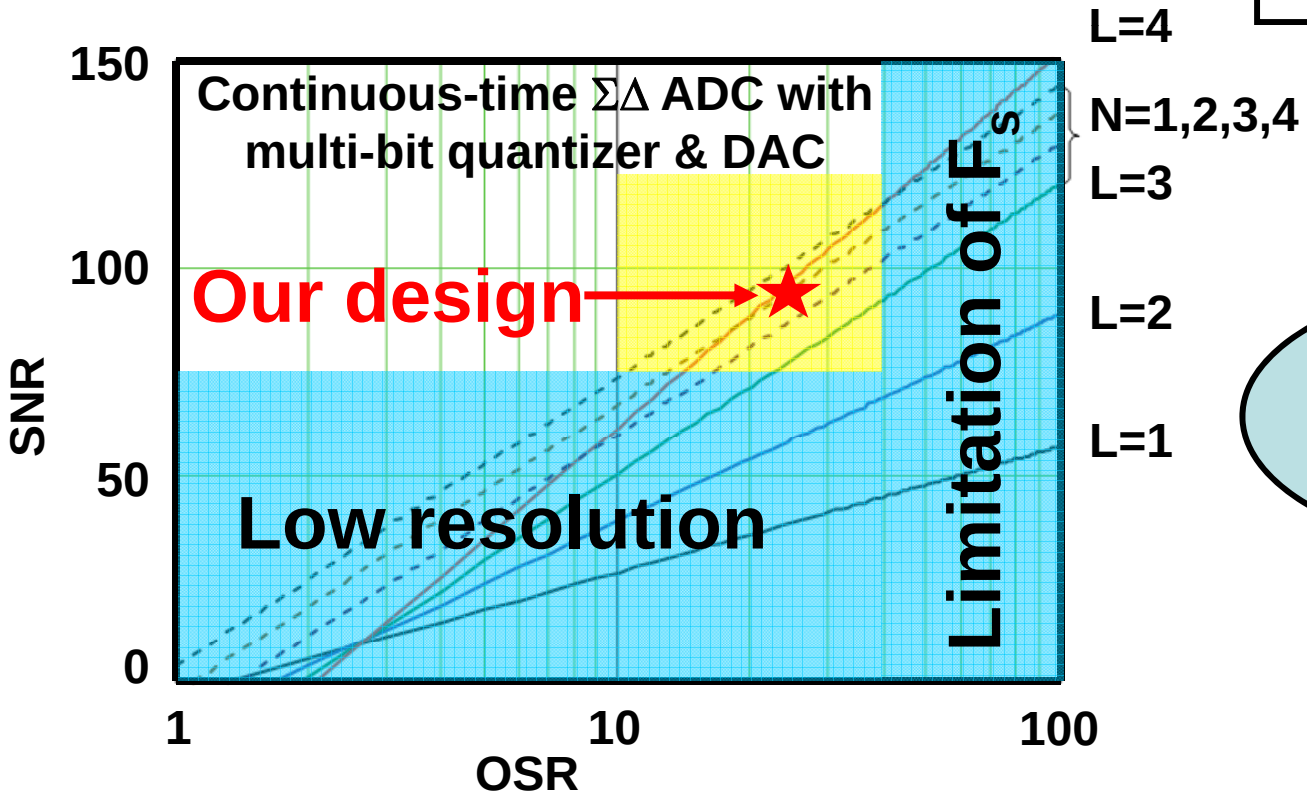
***10 MHz bandwidth (our target design)**
***High Dynamic Range (DR)**
***High Spurious-Free Dynamic Range (SFDR)**

ΣΔ ADC is a hopeful solution to achieve high DR & SFDR

ΣΔ ADC architecture



N: Quantizer resolution
OSR: oversampling ratio (=Fs/2/BW)
L: filter order



DAC linearity is an issue

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Linearity issues of feedback DAC

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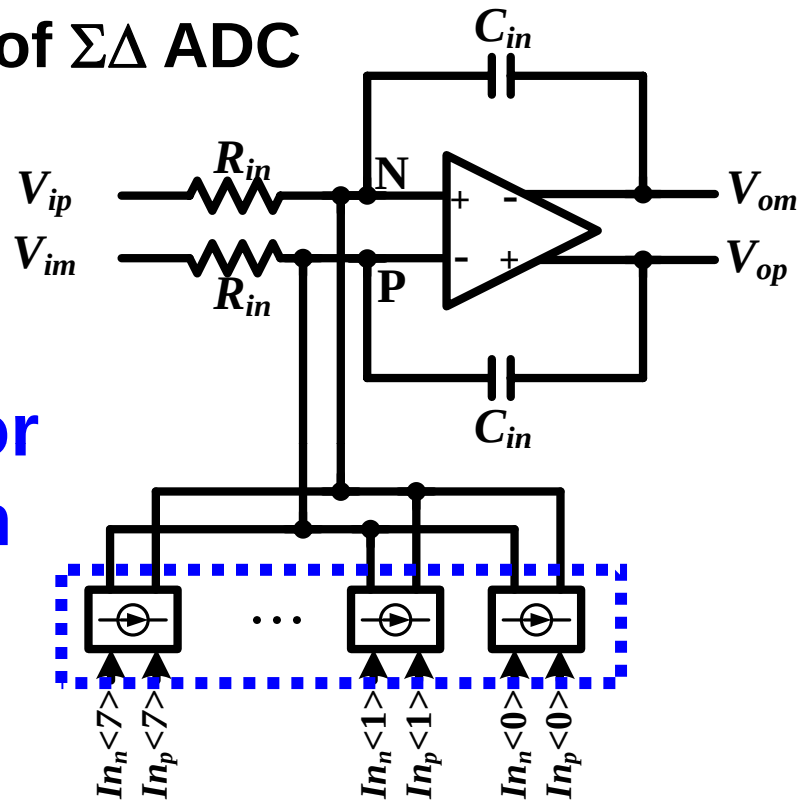
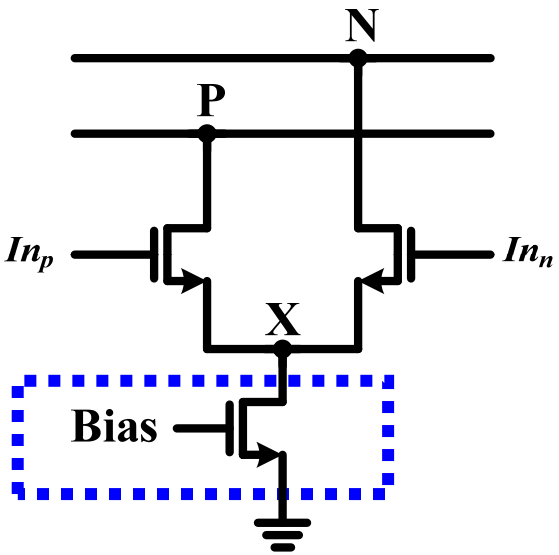
Input stage of ΣΔ ADC



Unity cell



Static error
Mismatch

Ex: 1.05 1.02 0.98

Mismatch deviation ⟺ Transitor size

For simplicity, a 3bit DAC is considered

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Linearity issues of feedback DAC

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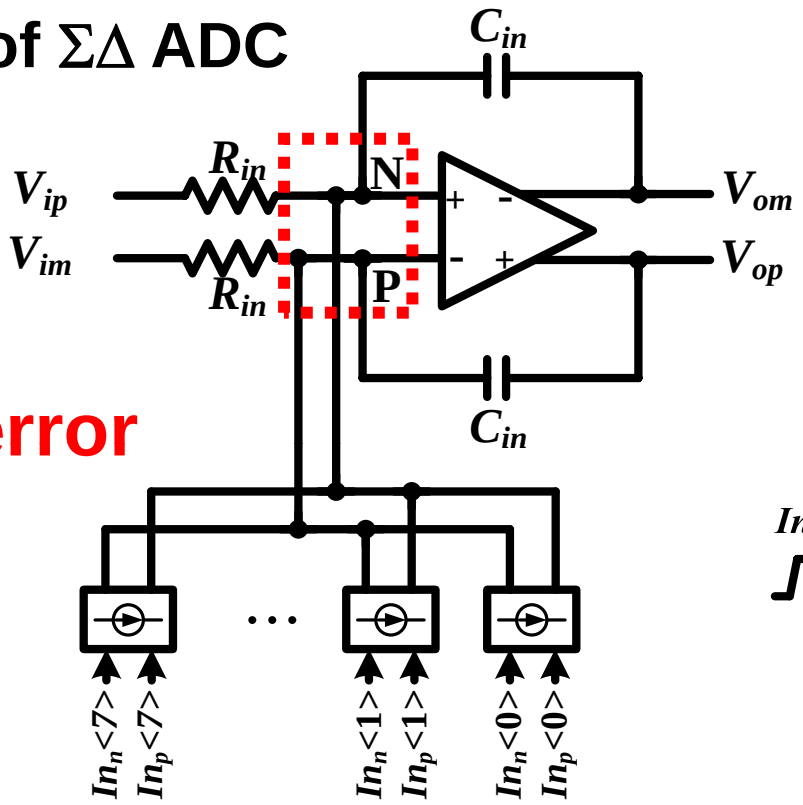
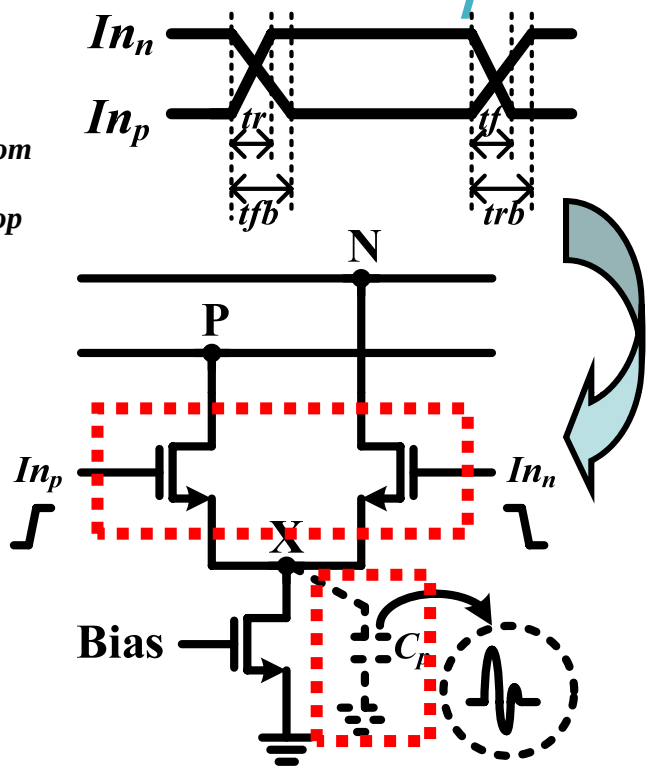
Input stage of ΣΔ ADC





Dynamic error
Glitch

Normalized glitch energy ⟺ **Parasitic capacitance Non-ideal switching**

For high speed operation, dynamic error becomes more critical

What is glitch energy?

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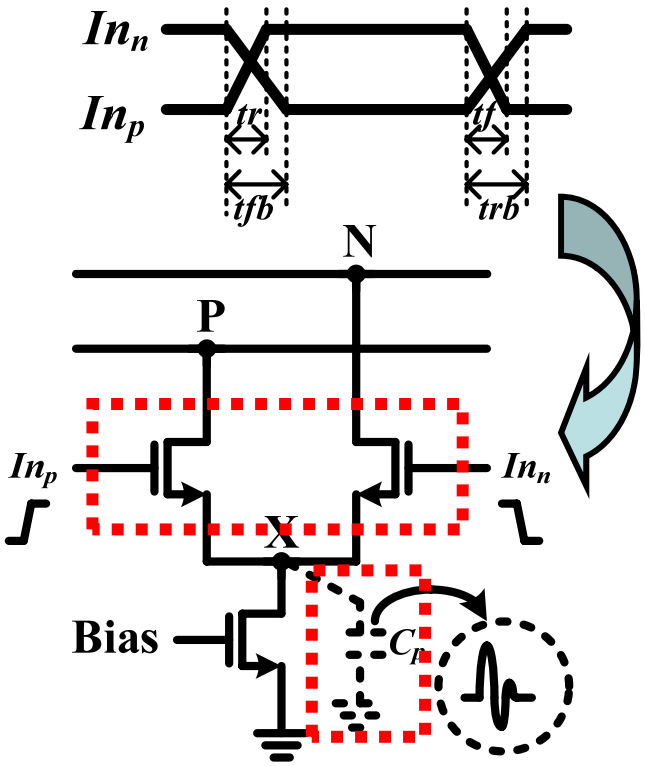
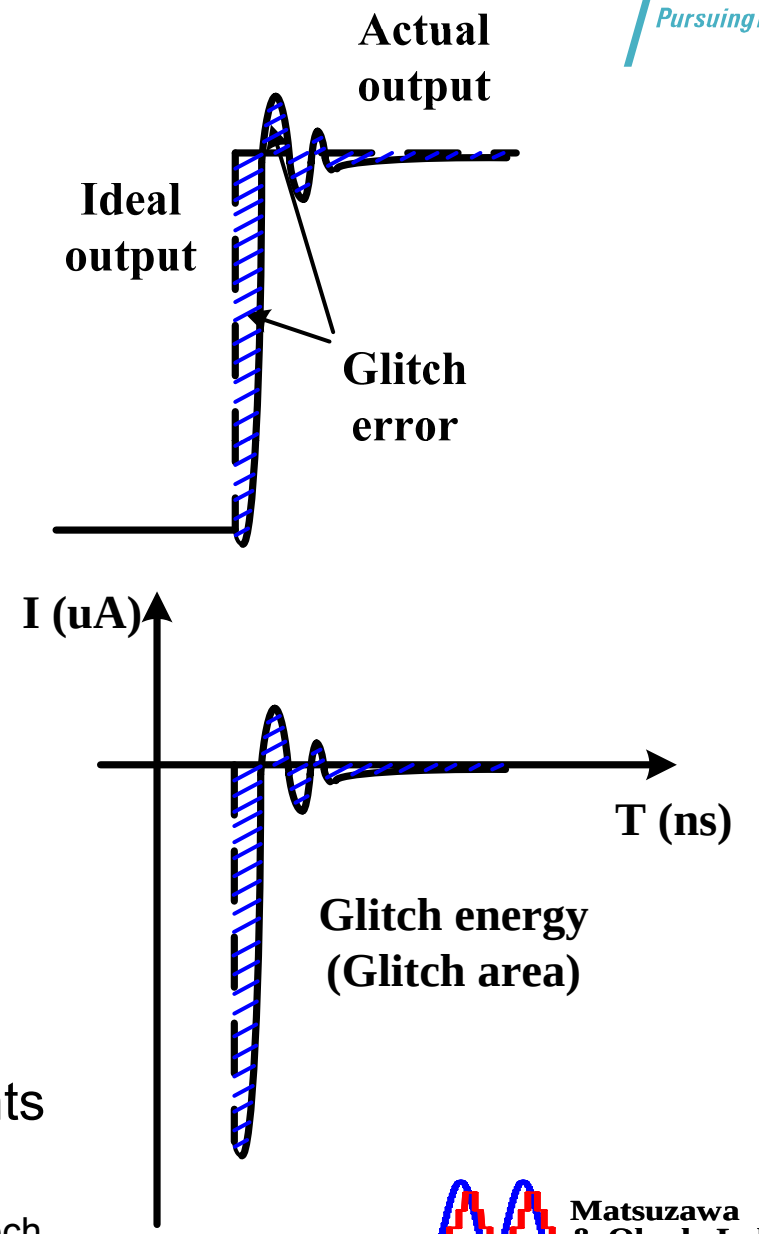
Switching asymmetry





Glitch energy: average of 8192points

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Requirements of DAC linearity

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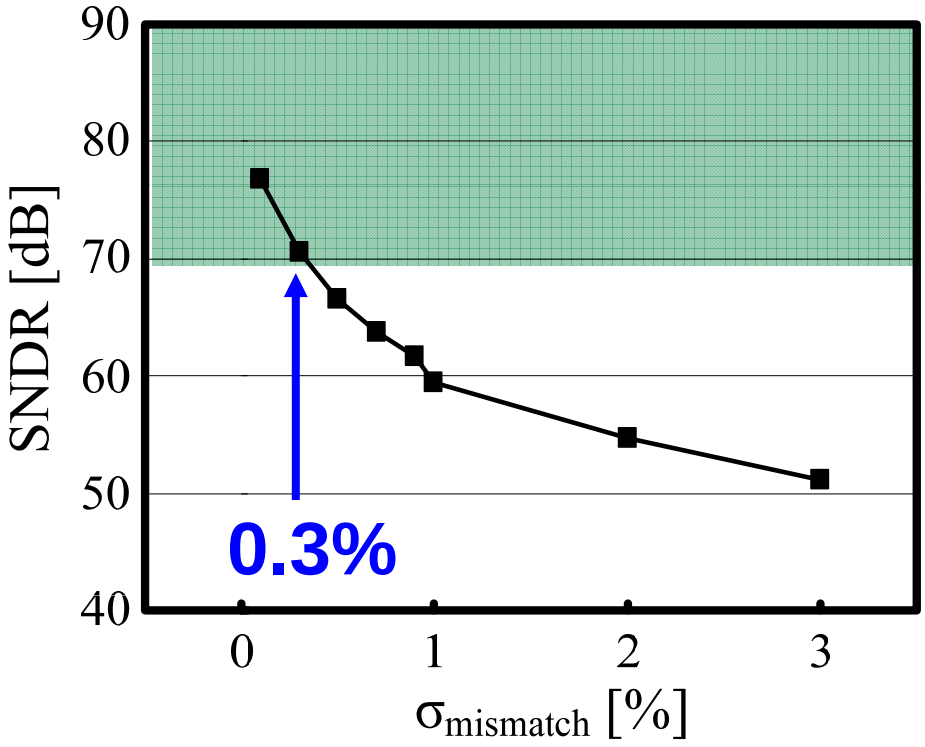
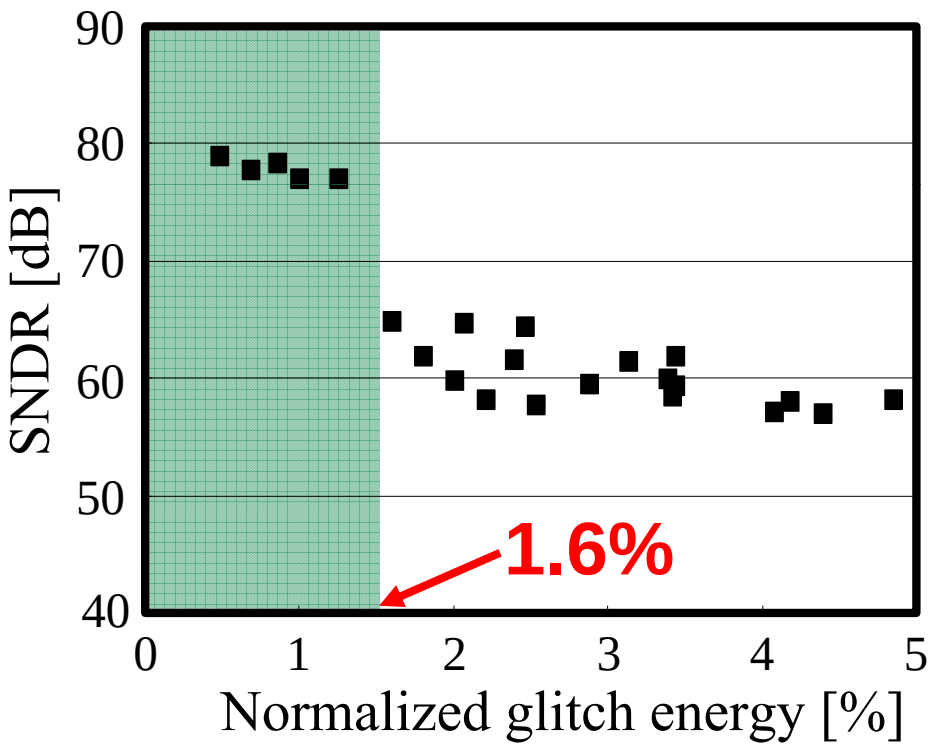
Static error
Mismatch

Dynamic error
Glitch





Requirement for SNR>70dB
(BW=10MHz, Fs=500MHz)

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DEM topology summary

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	Prop. OES	DWA-group (ADWA, Bi-DWA)	TC-group (RTC, RSTC)
Glitch	Good	Bad	Excellent
Mismatch	Good	Excellent	Bad

(DEM: to improve DAC linearity)

***Data Weighted Averaging (DWA) [1]**
***Advanced Random DWA (ADWA) [2]**
***Bi-directional DWA (Bi-DWA) [3]**
***Thermometer Coding (TC, w/o DEM)**
***Randomized Thermometer Coding (RTC) [4]**
***Restricted Swapping Thermometer Coding (RSTC) [5]**

[1] R. T. Baird *et al.*, *IEEE Trans. Circuits Syst. II,*, Dec. 1995.
[2] I. Fujimori *et al.*, *IEEE J. Solid-State Circuits*, Dec. 2000.
[3] D. H. Lee *et al.*, *IEEE Trans. Circuits Syst. II,* Oct. 2007.
[4] D. H. Lee *et al.*, *IEEE Trans. Circuits Syst. II,* Feb. 2009.
[5] M. H. Shen *et al.*, *IEEE Trans. Circuits Syst. II,* May. 2010.

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OES: Eliminating Effect of Glitch

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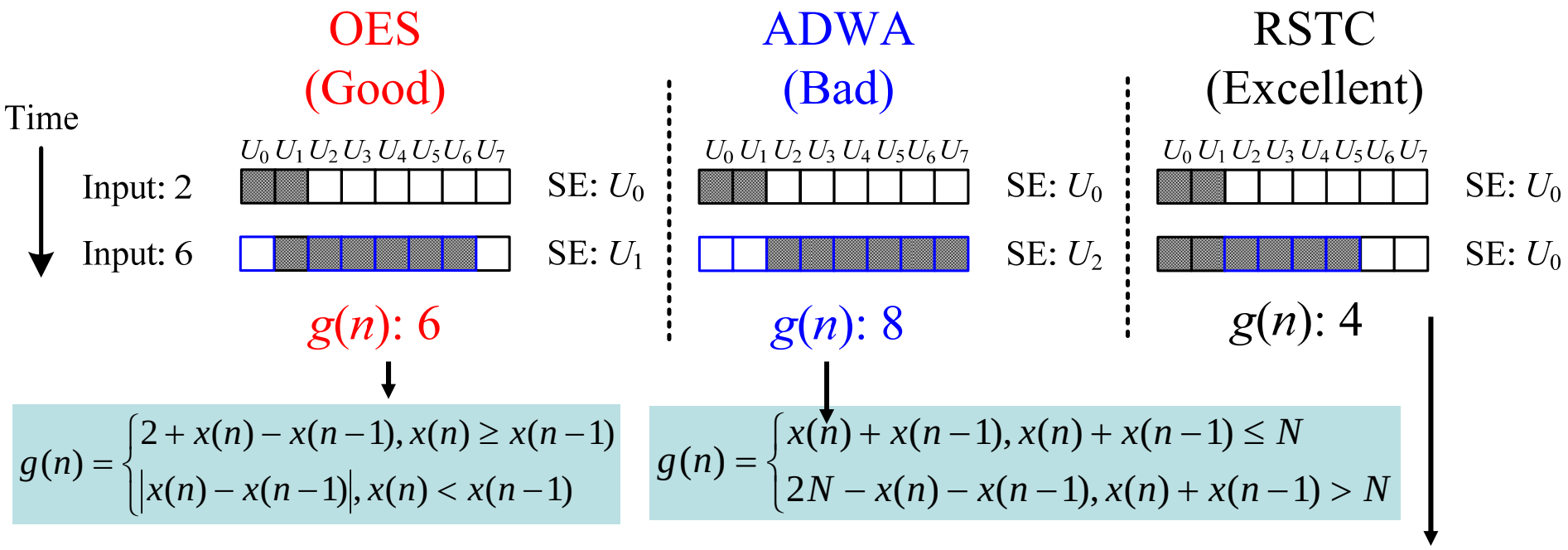
By reducing the number of switched elements *g*(*n*)
(w/ same other glitch conditions)

***g*(*n*)** ↑ ⟺ **Glitch energy** ↑



$$g(n) = \begin{cases} 2 + x(n) - x(n-1), x(n) \geq x(n-1) \\ |x(n) - x(n-1)|, x(n) < x(n-1) \end{cases}$$

$$g(n) = \begin{cases} x(n) + x(n-1), x(n) + x(n-1) \leq N \\ 2N - x(n) - x(n-1), x(n) + x(n-1) > N \end{cases}$$

$$g(n) = |x(n) - x(n-1)|$$

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Glitch Energy

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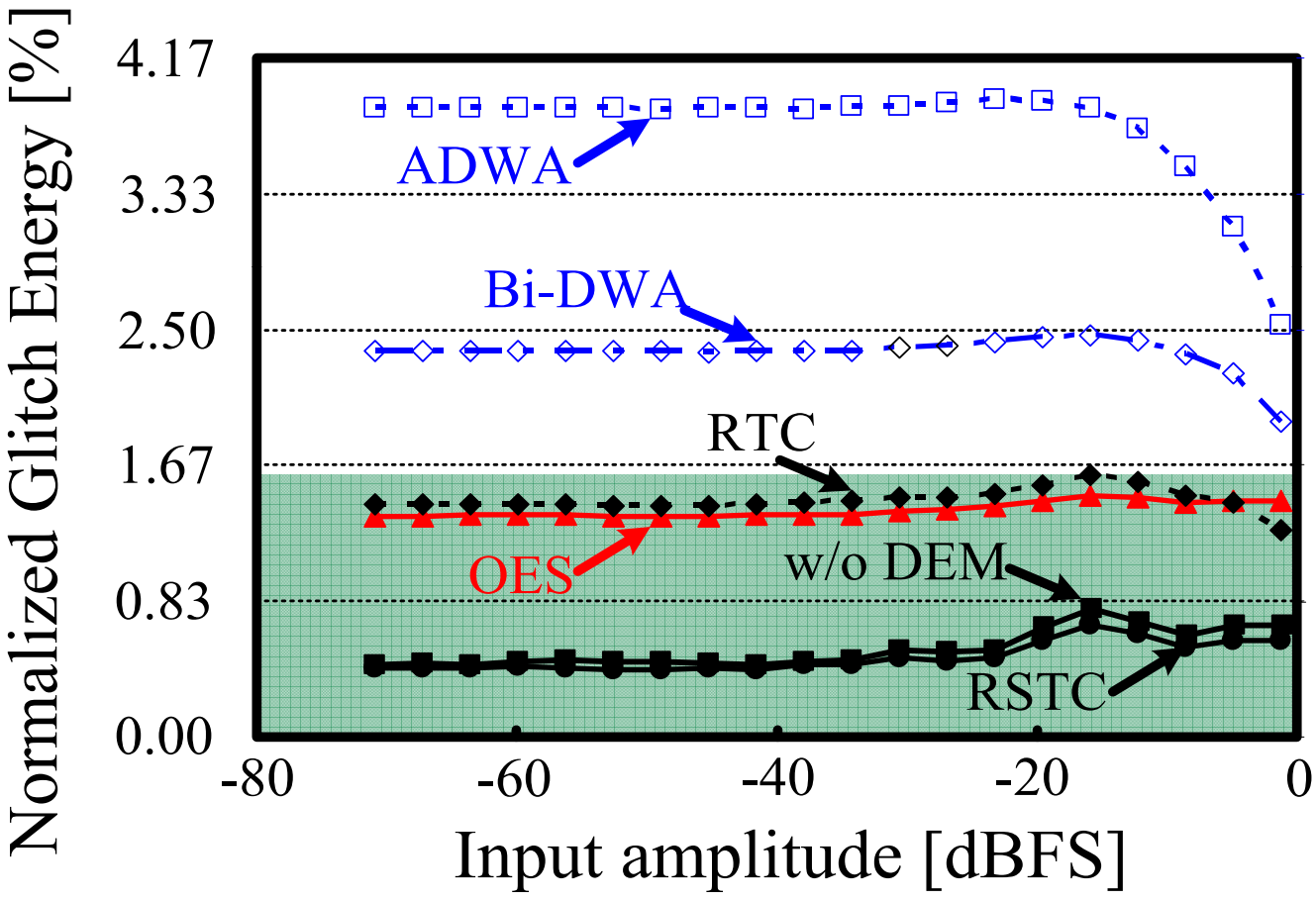
$g(n)$ ↑ ⟺ Glitch energy ↑



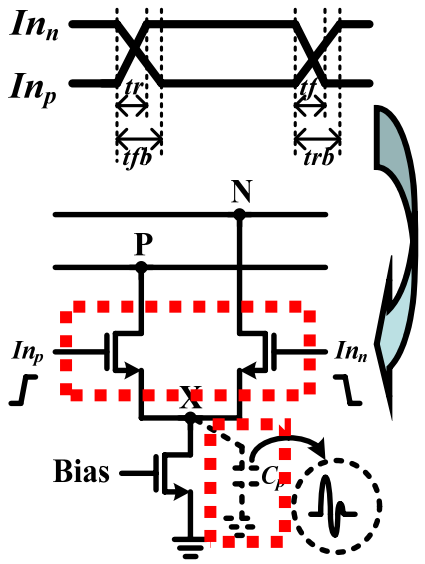
Sim condition

**tfb-tf=trb-tr=20ps*

*Cp=10fF

*3bit DAC

(w/o mismatch)



Requirement for SNR>70dB (BW=10MHz, Fs=500MHz)

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OES: Preserve Reduction of Mismatch Effect

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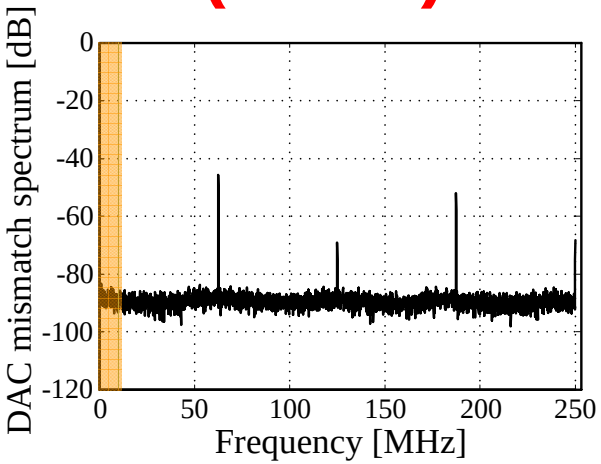
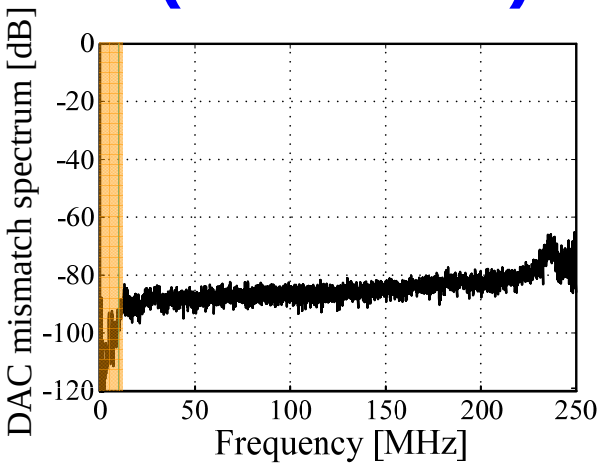
By reducing the mismatch error spectrum in the interesting bandwidth
(w/ same mismatch deviation)

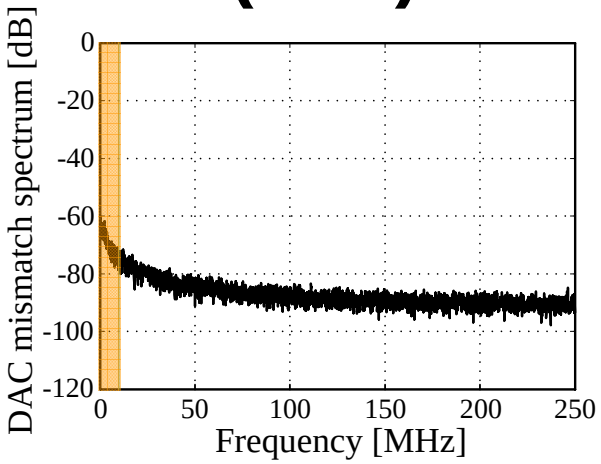
OES (Good)



ADWA (Excellent)



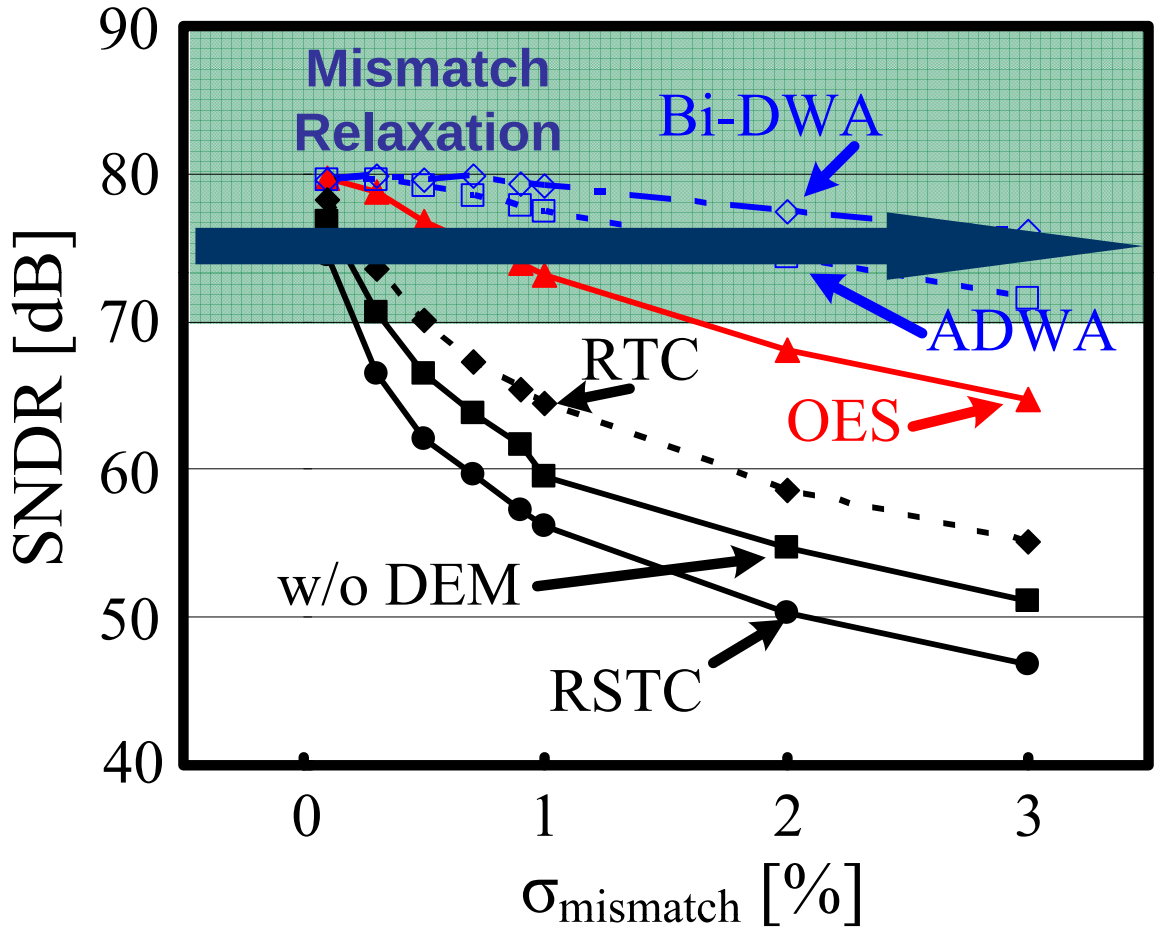
RSTC (Bad)



(1%mismatch, input: 1MHz@-30dBFS)

Mismatch requirement

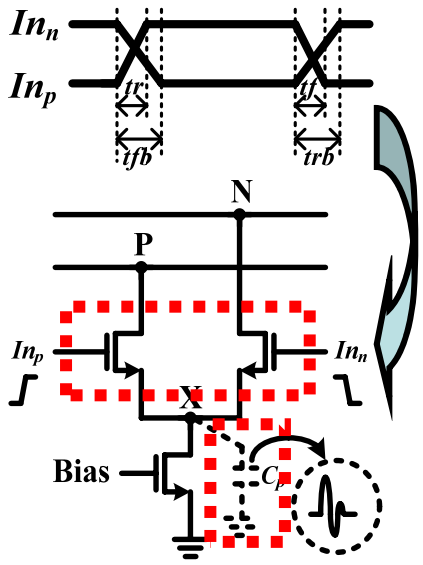
Mismatch ↓ ⟺ DAC area ↓



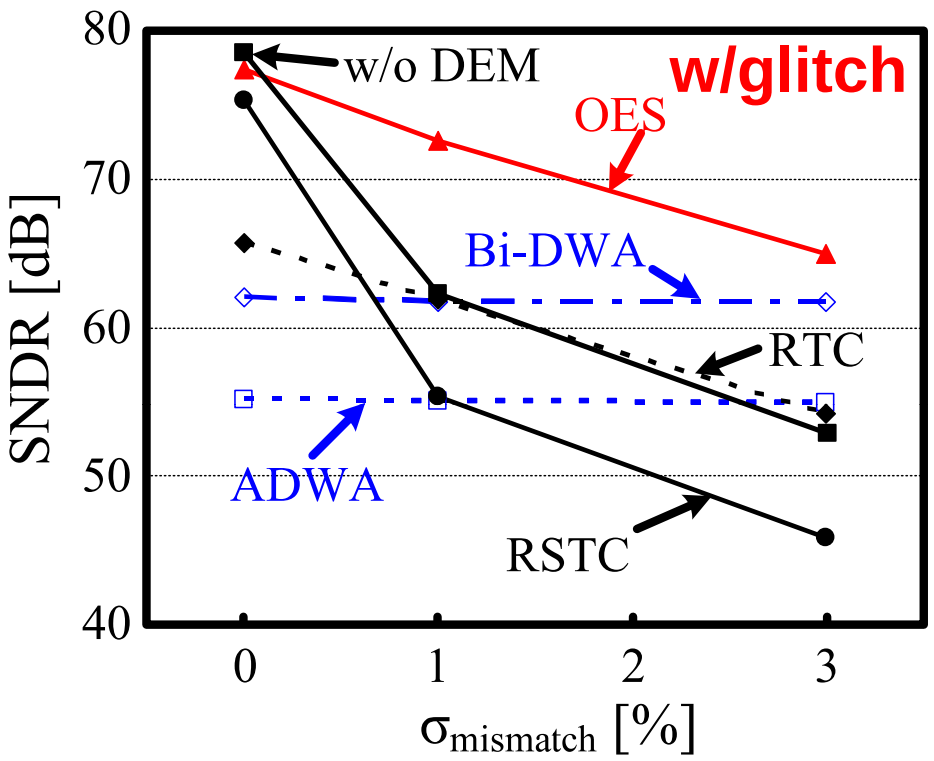
Requirement for SNR>70dB (BW=10MHz, Fs=500MHz)

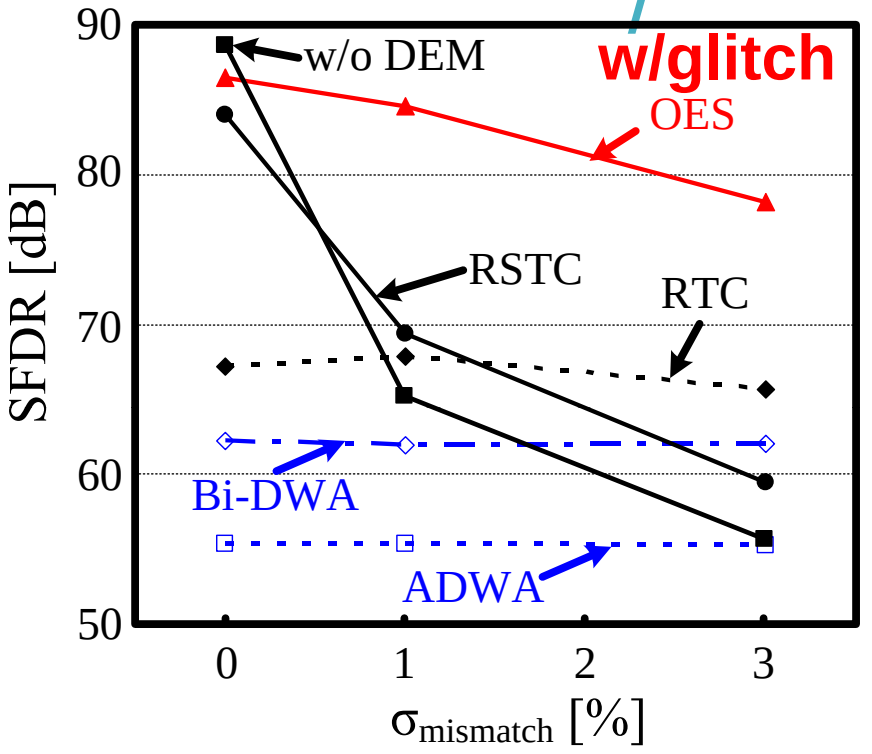
Sim condition

**tfb-tf=trb-tr*=0ps
*Cp=10fF
*3bit DAC
(w/o glitch)



With Both of Glitch and Mismatch





OES achieves better SNDR & SFDR performance over the published DEM methods

Sim condition
*tfb-tf=trb-tr=20ps *Cp=10fF
*3bit DAC (w/ mismatch)

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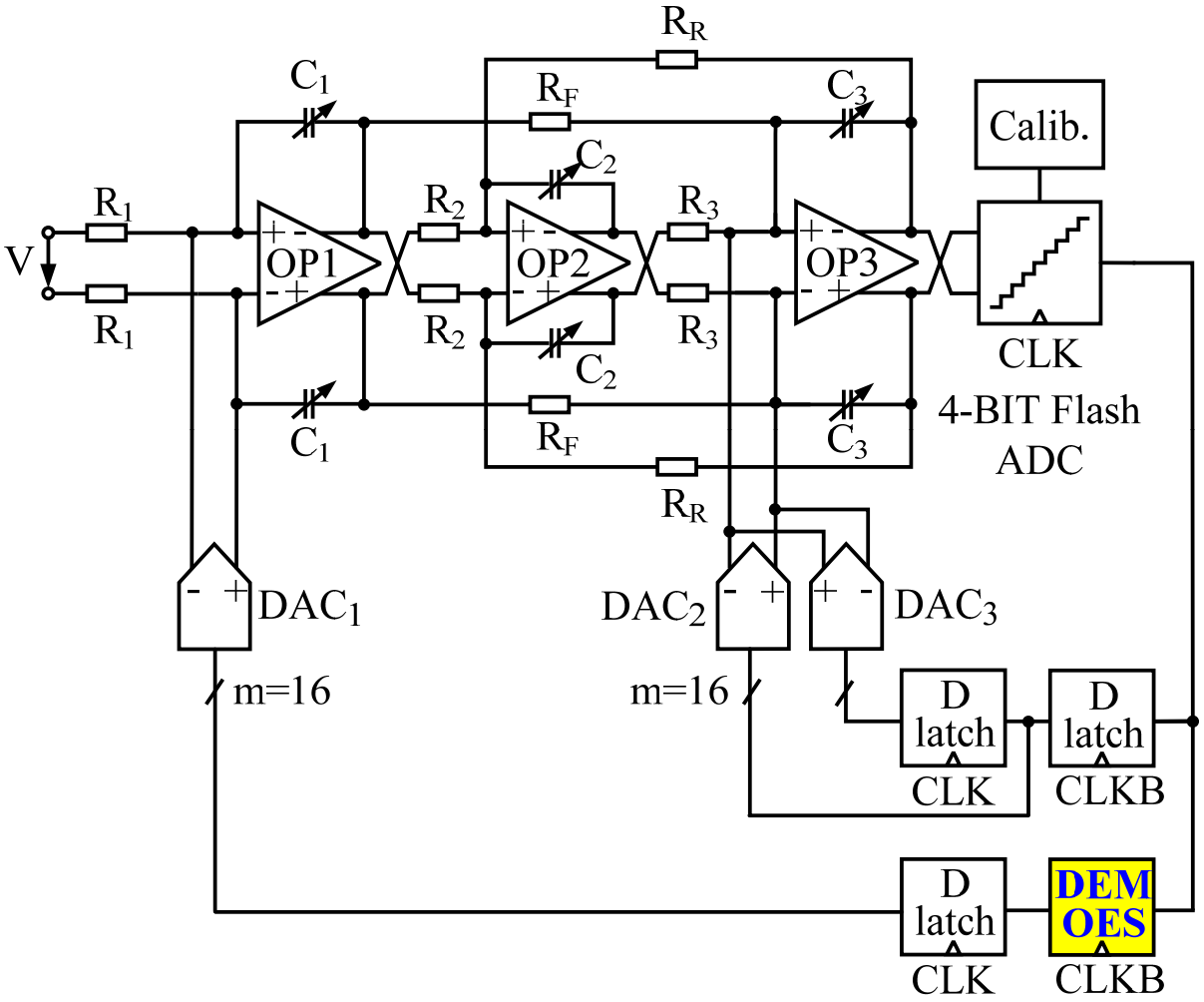
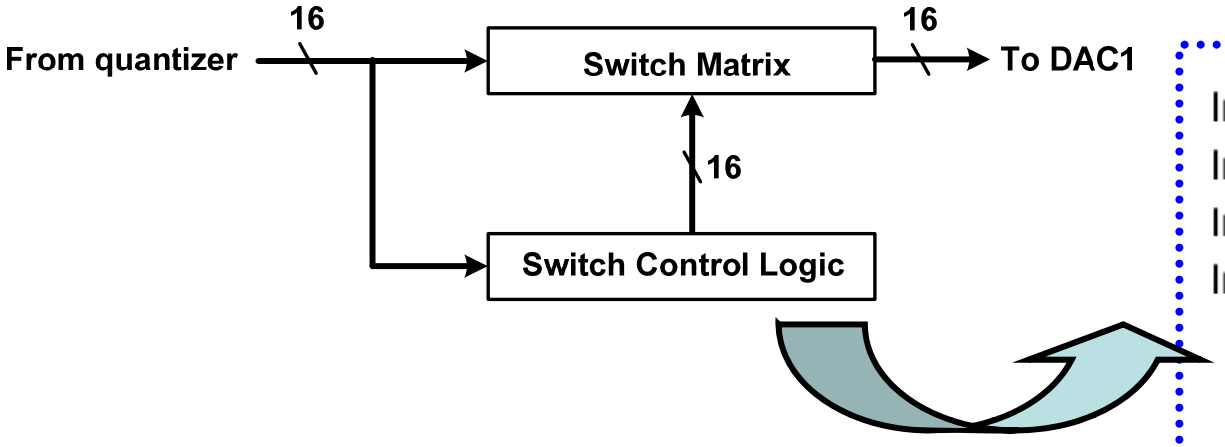
System architecture

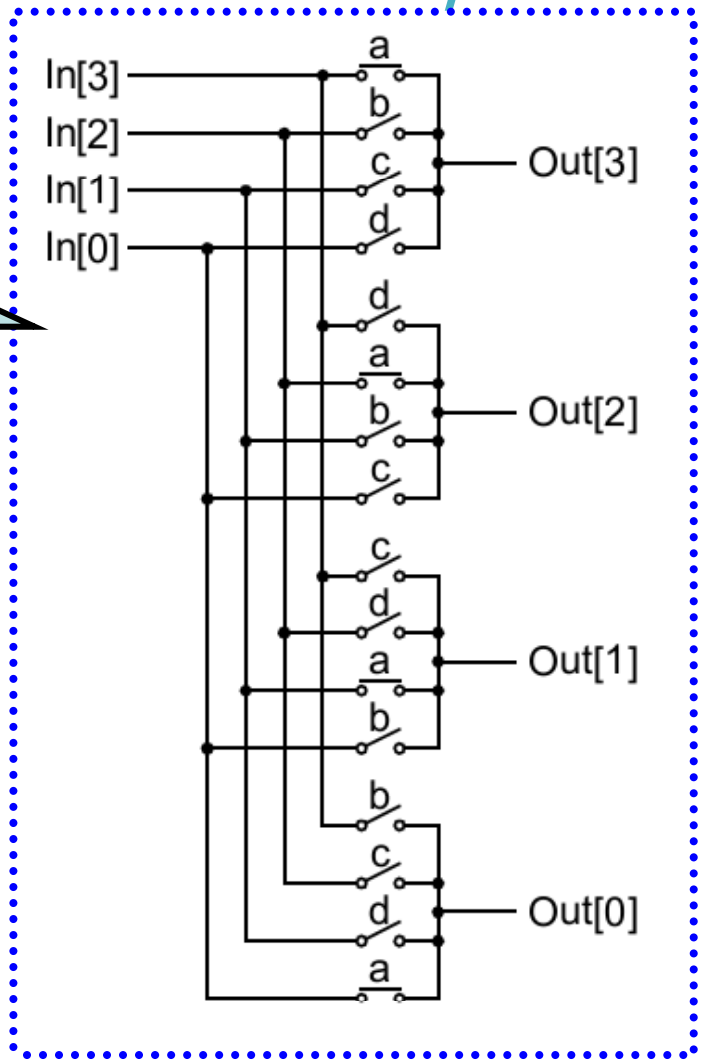


Modulator Spec

FF+FB, 3rd order
4bit AD/DA
BW: 10MHz
Fs: 500MHz
$SNDR_{req}$: 70dB
90nm CMOS process

OES DEM architecture





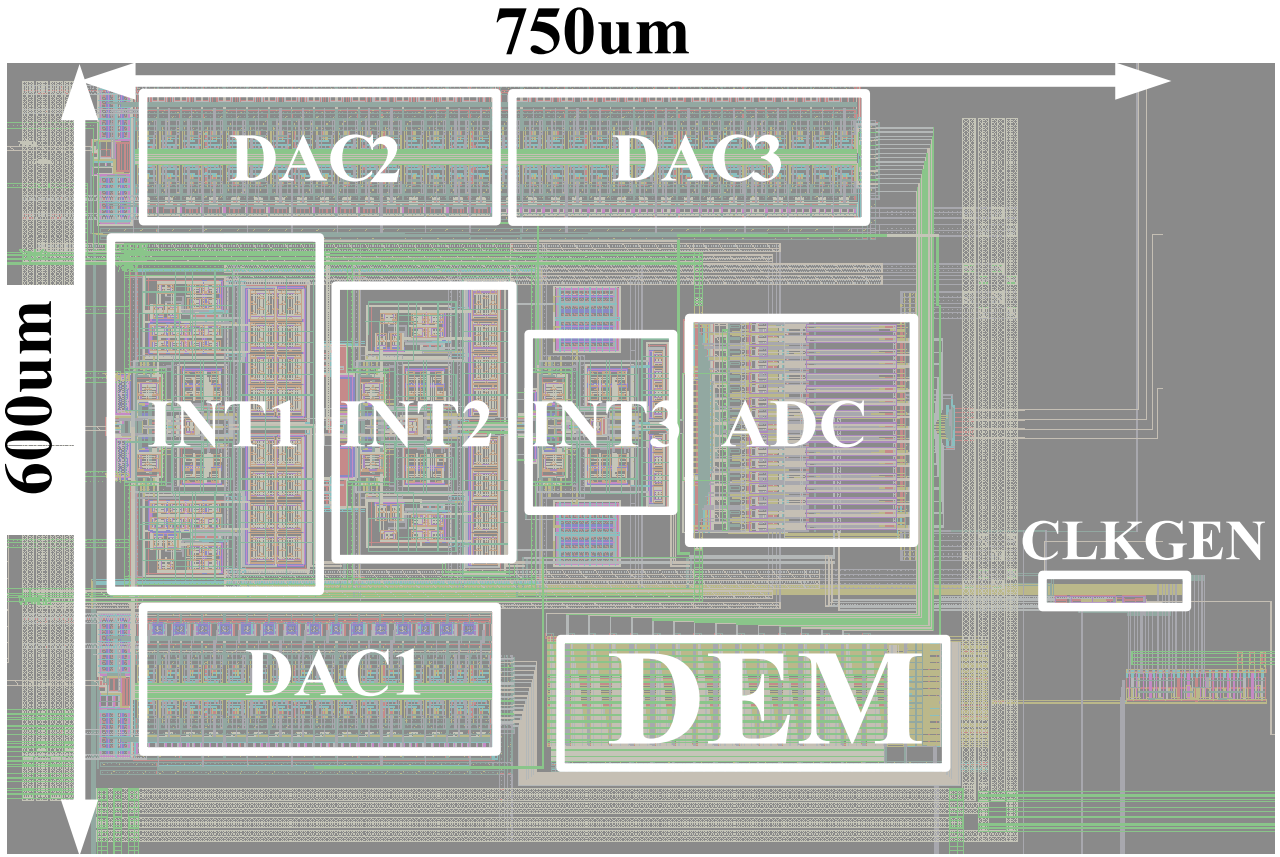
Example for 4 elements DAC

OES DEM

***Simplicity (no extra pointer, no register)**

***Relax timing requirement for feedback DAC**

Modulator layout

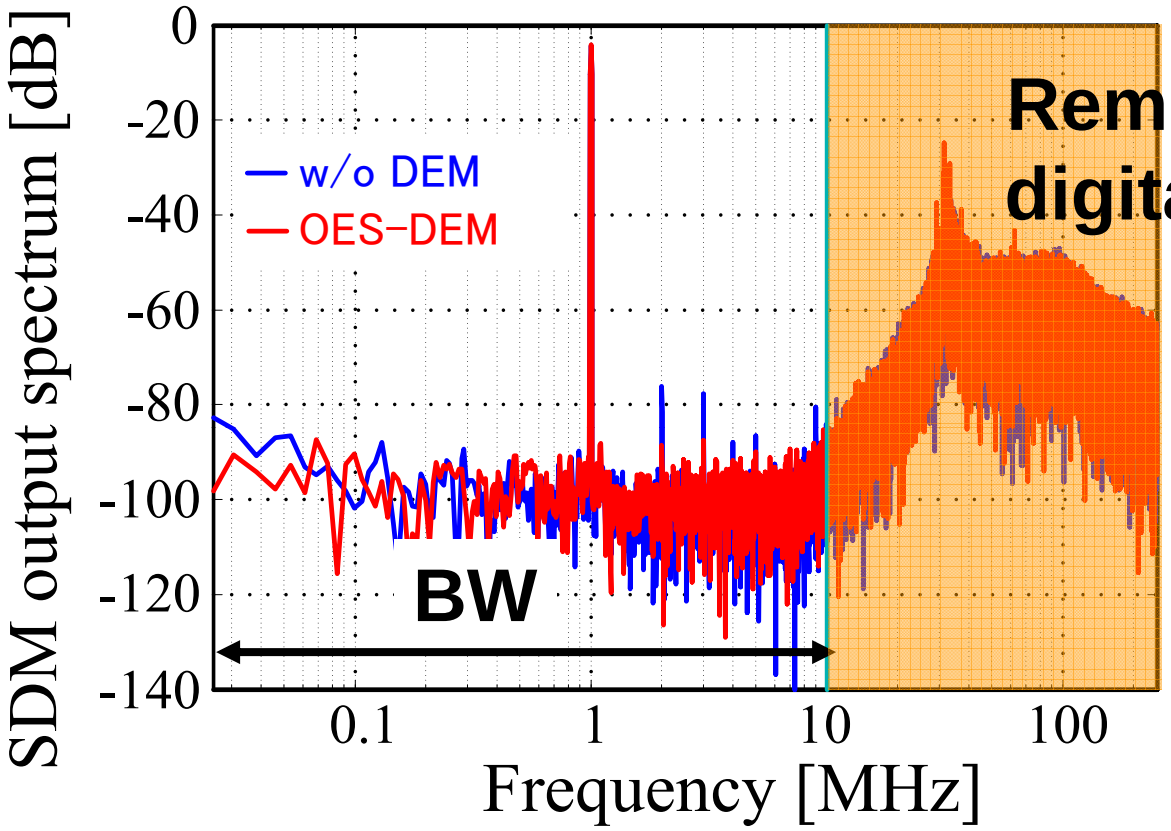


OES DEM

Core area: 9%

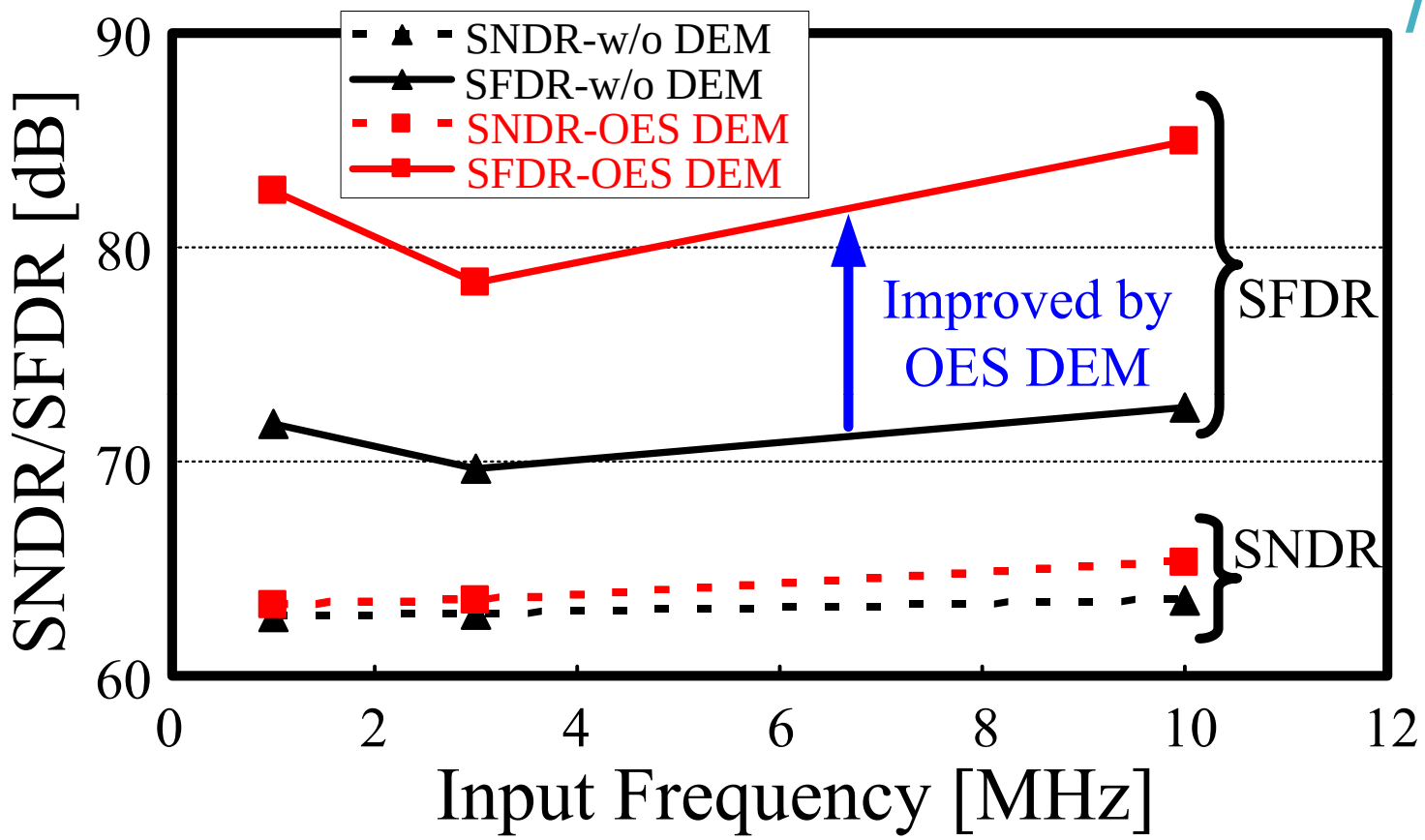
Power consumption: 6%

Measurement Results



	W/o DEM	OES DEM
SNDR	62.8	63.3
SFDR	71.8	**82.6**

Measurement Results



Average of 10dB SFDR improvement are achieved

Performance Comparison

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	Unit	This work	[6]	[7]	[8]
Type/ DEM		CT/OES	CT/DWA	DT/DEM	CT/DWA
Bandwidth	MHz	10	20	5	10
Samp. freq.	MHz	500	640	80	300
SFDR	dB	83	77*	85	64*
SNDR	dB	65	63.9	75.4	62.5
DR	dB	66	68	-	70.2
Power	mW	15.7	58	36	5.31
CMOS proc.	nm	90	130	180	110
FoM	fJ/conv	530	1130	750	240

***Better SFDR (compared with conv. DEM method)**

***Less power (w/ same SFDR)**

[6]J. G. Jo *et al.*, *ASSCC Dig. Tech. Papers*, Nov. 2010.
[7]O. Rajaee *et al.*, *IEEE J. Solid-State Circuits*, Apr. 2010.
[8]K. Matsukawa *et al.*, *IEEE Symp. on VLSI Circuits*, Jun. 2009.

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Conclusion

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- **Proposed OES DEM** method substantially suppresses the both effects of mismatch and glitch.
- $\Sigma\Delta$ modulator using OES DEM achieves **83dB SFDR and 10dB improvement** compared to no DEM.
- **Simplicity and effectiveness** of the OES technique makes it very attractive and prefer for cost and power considerations.

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Acknowledgments

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[1] R. T. Baird and T. S. Fiez, “Linearity enhancement of multibit ΔΣ A/D and D/A converters using data weighted averaging,” IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 42, no. 12, pp. 753–762, Dec. 1995.

[2] I. Fujimori, L. Longo, A. Hairapetian, K. Seiyama, S. Kosic, J. Cao, and S. L. Chan, “A 90-dB SNR 2.5-MHz output-rate ADC using cascaded multibit delta-sigma modulation at 8X oversampling ratio,” IEEE J. Solid-State Circuits, vol. 35, no. 12, pp. 1820–1828, Dec. 2000.

[3] D. H. Lee, and T. H. Kuo, “Advancing data weighted averaging technique for multi-bit sigma–delta modulators ,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 54, no. 10, pp. 838–842, Oct. 2007.

[4] D. H. Lee, T. H. Kuo, and K. L. Wen, “Low-cost 14-bit current-steering DAC with a randomized thermometer-coding method,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 56, no. 2, pp. 137–141, Feb. 2009.

[5] M. H. Shen, J. H. Tsai, and P. C. Huang, “Random swapping dynamic element matching technique for glitch energy minimization in current-steering DAC,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 57, no. 5, pp. 369–373, May. 2010.

[6] J. G. Jo, J. Noh, and C. Yoo, “A 20MHz bandwidth continuous-time ΣΔ modulator with jitter immunity improved full-clock period SCR (FSCR) DAC and high speed DWA,” ASSCC Dig. Tech. Papers, pp. 1-4, Nov. 2010.

[7] O. Rajaee, T. Musah, N. Maghari, S. Takeuchi, M. Aniya, K. Hamashita, and U. K. Moon, “Design of a 79 dB 80 MHz 8X-OSR Hybrid Delta-Sigma Pipelined ADC,” IEEE J. Solid-State Circuits, Vol. 45, No. 4, pp. 719-730, Apr. 2010.

[8] K. Matsukawa, Y. Mitani, M. Takayama, K. Obata, S. Dosho and A. Matsuzawa, “A 5th-Order Delta-Sigma Modulator with Single-Opamp Resonator,” IEEE Symp. on VLSI Circuits, pp. 68-69, Jun. 2009.

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Thank you!!!

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