A 83-dB SFDR 10-MHz Bandwidth Continuous-Time Delta-Sigma Modulator Employing a One-Element-Shifting Dynamic Element Matching

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***Abstract* — This paper proposes a new dynamic element matching (DEM) method referred to as one-element-shifting (OES) for the implementation of high spurious-free dynamic range (SFDR) multi-bit Delta-Sigma modulators (DSMs). Generic DEM techniques are successful at suppressing the mismatch error and increasing the SFDR of data converters. However, they will induce additional glitch energy in most cases. Some recent DEM methods achieve improvements in minimizing glitch energy but sacrificing their effects in harmonic suppression due to mismatches. OES technique proposed in this paper can suppress the effect of glitch while preserving the reduction of element mismatch effects. Hence, this approach achieves better SFDR performance over the published DEM methods. With the proposed OES, a 3rd order, 10 MHz bandwidth continuous-time DSM is implemented in 90 nm CMOS process. The measured SFDR attains 83 dB for a 10 MHz bandwidth. The measurement result also shows that OES improves the SFDR by higher than 10 dB.**

***Index Terms* — Delta-sigma modulator, dynamic element matching, glitch energy, mismatch.**

I. Introduction

The rapid growth in wireless communication systems has stimulated the development of data conversion interfaces that can be integrated in standard CMOS technologies. For wireless communication applications, such as TV tuner, mobile phone and wireless LAN, analog-to-digital converters (ADCs) with 10MHz bandwidth are required. Moreover, the reduction of cross-modulation is also needed to improve the quality of communication. This leads to increasing the requirements for the high SFDR ADC design in 10MHz bandwidth. Among the wide variety of ADC architectures, multi-bit DSMs are the most suitable candidates to meet the needs of high SFDR. The major limitation of DSMs employing multi-bit quantization is the nonlinearity of the internal multi-bit digital-to-analog converter (DAC) caused by mismatch. DEM technique [1] is usually used to reduce the effects of random component mismatches in DAC's. Among the DEM algorithms, data weighted averaging (DWA) is widely used to achieve first-order mismatch shaping but it causes baseband tones for the certain input amplitudes [2]. In recent years, several DWA-like techniques (Bi-DWA, ADWA) [3-4] have attempted to circumvent the DWA tone problem. However, generic DWA techniques will induce additional glitch energy and decrease the SFDR. In [5-6], some DEM methods with glitch minimization (RTC, RSTC) are introduced, but they are weak in harmonic suppression caused by mismatch. In this work, we present a new DEM technique named OES that can preserve the reduction of element mismatch effects while eliminating the effect of glitch. Hence, a better SFDR can be achieved with the OES method.

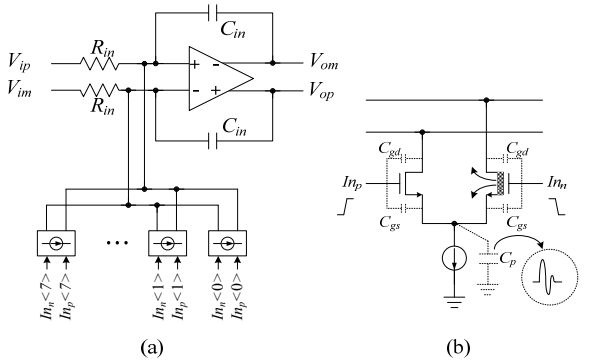

Fig. 1. (a) Block schematic of input stage of DSM with internal non-return-to-zero current-steering DAC, (b) DAC unity cell with nonideal switches.

This paper is organized as follows: Nonlinear distortion from glitch is described in Section II. In Section III, the proposed OES method, analysis and verification of OES are presented. Section IV shows the implementation and experimental results of DSM using OES. The conclusions are given in section V.

II. Nonlinear Distortion by Glitch

Fig. 1 shows block schematic of input stage of DSM with internal non-return-to-zero (NRZ) current-steering DAC and its corresponding DAC unity cell. Glitch or spike is generated when the internal DAC output changes from one value to a new value. The major causes for the glitches include signal feedthrough through the gate–drain capacitance, static timing uncertainty between different current cells, and asymmetry up-and-down characteristics

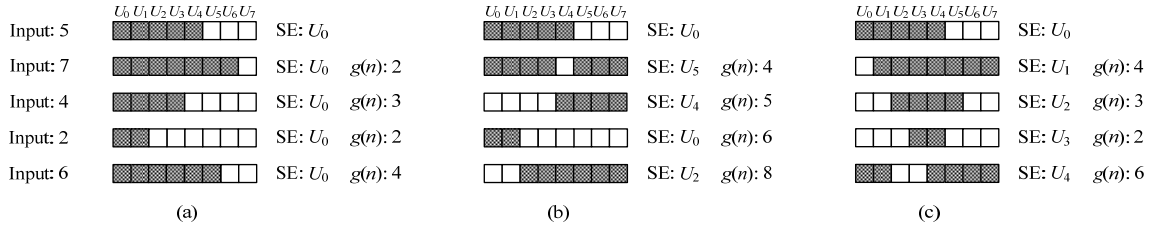

Fig. 2. Example of element selection for (a) conventional thermometer coding, (b) conventional DWA coding and (c) proposed OES.

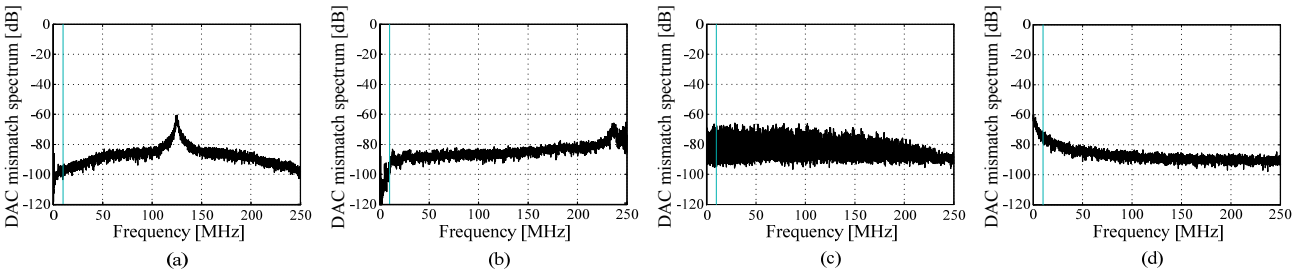

Fig. 3. DAC mismatch spectra of DSM at -30dB input employing (a) Bi-DWA. (b) ADWA. (c) RTC. (d) RSTC.

for the output [6], as shown in Fig. 1(b). Among these effects, the latest one, non-ideal switching behavior between two consecutive update steps causes the most critical dynamic error which results in degradation of the SFDR [7]. The glitch energy (also called glitch area), a widely used factor to evaluate the effect of the glitch, is defined as the time integral of the analog value of a spike compared with a reference pulse shape [6]. This phenomenon is severe for the high-speed DSM since the glitch area in one sampling period increases with the sampling frequency.

A 3rd-order DSM with a 3-bit quantizer, a 9-level internal current-steering DAC, a 25x OSR, a 10-MHz conversion bandwidth, and a 500-MHz sampling frequency, resulting in an SNDR of 80 dB in the ideal case is used for the analysis in different DEM coding schemes. A non-ideal switching behavior is also modeled to investigate the glitch effect, and it is assumed that all unity cells exhibit exactly the same switching imperfections (no dynamic mismatches). In glitch model, for simplification, C_{gd} and C_{gs} will be neglected and value of C_p is set to 10fF. This value of C_p is estimated from DAC design where its element mismatch error of current source is suppressed to 1% standard deviation.

The glitch energy is proportional to $g(n)$, which is the total number of switched unit current sources for the input from $x(n-1)$ to $x(n)$. Actually, there are two kinds of switching states depending on the previous state of each current cell, i.e. the current cell has been connected to the output node P (or N) before the word transition. However, thanks to differential architecture of DAC and large gain of the integrator, the difference between two states can be ignored and the glitch energy can be considered proportional to $g(n)$. Fig. 2(a), (b) shows examples of element selection for conventional thermometer coding (TC), conventional DWA coding, respectively. For TC, starting element (SE) of the subsequent selection cycle is unchanged all the time, so $g(n)$ can be expressed briefly as follows:

$$g(n) = |x(n) - x(n-1)| \tag{1}$$

On the other hand, SE of DWA is updated for each selection cycle and $g(n)$ can be obtained as follows:

$$g(n) = \begin{cases} x(n) + x(n-1), x(n) + x(n-1) < N \\ 2N - x(n) - x(n-1), x(n) + x(n-1) > N \end{cases} \tag{2}$$

where N is the number of DAC element. According to Eq. (1) and (2), a much larger number of switched unit current sources, as well as glitch energy, can be predicted when DWA is used. In [5-6], some DEM methods with glitch minimization (RTC, RSTC) are introduced. RSTC method is successful in keeping $g(n)$ as small as TC, but their weak harmonic suppression ability to the mismatch is a draw back. This conclusion can be verified by using the DAC mismatch spectra for an input level of -30 dB, frequency of 1 MHz with a 1% standard deviation of element mismatch error in internal DAC, as shown in Fig. 3. For DWA groups (Bi-DWA, ADWA), the first-order mismatch shaping is preserved while the DAC mismatch tones can be shifted away from $f_s/2$, as shown in Fig. 3(a)-(b), where f_s is the sampling frequency. On the other hand, for the RTC and RSTC method in Fig. 3(c)-(d), the noise floor in the interesting bandwidth of the modulator is raising, especially for the RSTC. Hence, a large degradation in SNDR when applied these coding methods to the DSM can be predicted. Simulation results show that an average of 13dB (for RTC) and 22dB (for RSTC) degradation in SNDR compared to DWA groups are obtained respectively when the element mismatch error with a 1% standard deviation is applied to the DAC. The degradation of RTC and RSTC method can be understood because they were firstly proposed for DAC operating at

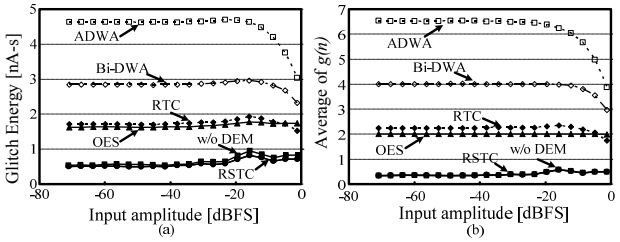

Fig. 4. (a) Glitch energy of internal 3-bit DACs in DSM with different coding schemes for different input level. (b) Its corresponding number of switched element.

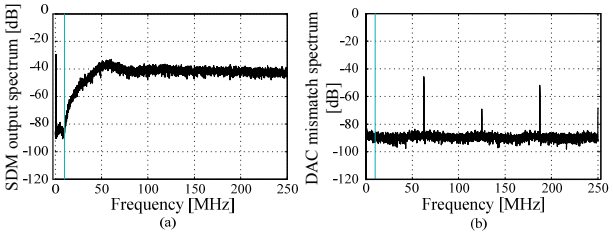

Fig. 5. (a) Output spectrum of DSM employing OES for input level of -30dB. (b) Its corresponding DAC mismatch spectrum.

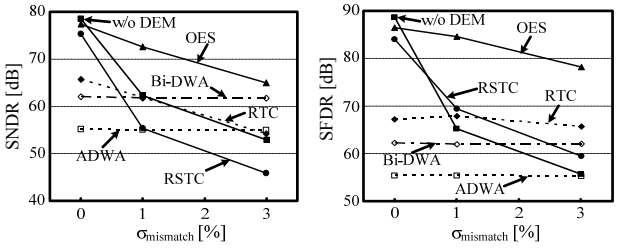

Fig. 6. Simulated (a) SNDR and (b) SFDR with effect of glitch and different mismatch level.

Nyquist frequency, and not suitable for the oversampling operation.

To overcome these problems, we present a new DEM technique named OES that can preserve the reduction of element mismatch effects while eliminating the effect of glitch by keeping $g(n)$ as small as possible. Its operation will be explained in the next section.

III. Proposed OES Method

A. Operation Principle of OES Method

Fig. 2(c) shows the element sequence in a 3-bit DAC example using proposed OES coding method. In OES, SE of the subsequent selection cycle is determined by advancing a fixed one step from the SE of the previous selection cycle. Its operation is demonstrated in Fig. 2(c).

B. Eliminating Effect of Glitch

From Fig. 2(c), the number of switched unit current sources $g(n)$ can be obtained as follows:

$$g(n)=\begin{cases}2+x(n)-x(n-1), x(n)\ge x(n-1)\\ \left|x(n)-x(n-1)\right|, x(n)<x(n-1)\end{cases} \quad (3)$$

For $x(n)<x(n-1)$, OES has the same value of $g(n)$ compared to TC method. In DSM with a certain input (DC or a sinusoidal input), value of $x(n)$-$x(n-1)$ is usually belongs to {-1, 0, 1}, Eq. (3) can be expressed equally to

$$g(n)=2+x(n)-x(n-1) \quad (4)$$

Fig. 4(a) shows glitch energy of internal 3-bit DAC in DSM with different coding schemes for different input level, and Fig. 4(b) shows its corresponding number of switched element. The glitch model and simulation conditions are described in Section II. With 2^{13} samples per run, the glitch energy and its corresponding number of switched element are calculated by averaging the results of $2^{13}-1$ code transitions instead of the midcode transition only. According to Eq. (4), it can be understood that the average of g(n) in OES is about 2 over the full range of input signal amplitudes in Fig. 4(b). The characteristic of the number of switched element in DWA groups also shows good agreement with (2) and can be explained as follows: For small input signals modulator output mostly consists of code 3, 4, and 5 with code 4 having the highest density. As a result, the higher average of g(n) can be obtained. When the input signal increases, the other codes will appear and according to Eq. (2), the existence of the lower value of g(n) will reduce the average value of g(n).

Glitch energy shows good agreement with the number of switched element. From Fig. 4 it can be noticed that, our proposed OES shows smaller glitch energy compared with other DEM structures except the RSTC and TC (without DEM) method.

C. Preserve Reduction of Element Mismatch Effect

Fig. 5(a) shows the output spectrum of the DSM employing the OES for an input level of -30 dB with a 1% standard deviation of element mismatch error in internal DAC, and Fig. 5(b) shows the corresponding DAC mismatch spectrum. As shown in Fig. 5(b), large tones are observable at $f_s/8$, where f_s is the sampling frequency, and can be explained as followed. According to the characteristic of our proposed method, starting element will be re-chosen after 8 clock cycles, independent on the input DAC value. Compared with the DWA case where the first tone was at $f_s/2$ and caused aliasing, in this case, only the fourth harmonic is at $f_s/2$ and the aliasing caused by $f_s/2$ will be smaller. It is required that DAC error tones should not be allowed in the vicinity of the baseband, and considering a two times margin, the *OSR* should satisfy the condition $OSR > 8$. For the common case, $OSR > N$, where N is the number of DAC element.

Simulation results show that the degradation in SNDR compared to DWA groups is within 6dB over the full range of input signal amplitudes. This value is 13dB for RTC and 22dB for RSTC respectively as explained in above section.

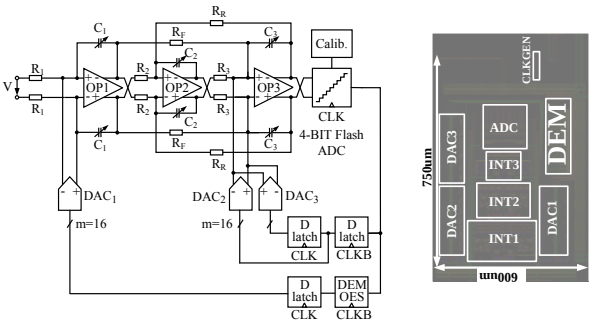

Fig. 7. 3rd order, 4-bit ΔΣ modulator and its chip layout

D. With Both of Glitch and Element Mismatch Effect

Fig. 6 shows simulated SNDR and SFDR with both of glitch and element mismatch effect. For small mismatch, RSTC and conventional TC (without DEM) show good performance on SNDR and SFDR but it degrades rapidly when the mismatch increases. In spite of that, the OES method always achieves better SNDR and SFDR performance over the other DEM structures. On average, a 10 dB SFDR improvement can be achieved by the OES technique.

IV. Implementation and Measured Results

In section III, our proposed OES method shows its effectiveness compared to the other coding schemes. With the proposed OES, a 3rd order, 10 MHz bandwidth and a 500 MHz sampling frequency continuous-time DSM is implemented in 90 nm CMOS process. The modulator architecture and its chip layout is shown in Fig. 7. Its core size is 750 μm x 600 μm. The OES can be implemented with no extra hardware cost, because no extra pointer or extra random number generator is needed. Hence, the shorter extra DEM delay will be added to the modulator, and is suitable for high speed operation.

Fig. 8 shows the DSM output spectrum at 1 MHz input without DEM and with the OES method enabled respectively. The measured SFDR exceeds 83 dB for a 10 MHz bandwidth, a 10dB improvement is obtained compared to without DEM. This characteristic was kept up to 10 MHz input frequency with an average of 10dB SFDR improvement, as shown in Fig. 9 The degradation of SFDR at 3 MHz input can be explained by non-linearity of opamp, not by the OES method. The peak SNDR, SFDR and DR are 65 dB, 66 dB and 83 dB respectively while consuming 15.7 mW from the 1.2 V voltage supply. The Figure of Merit (FoM) is 530 fJ/conv. The OES DEM occupied 9% of the core area and consumed 6% of the core power consumption. Hence, it is proven that the OES technique employed in this design is a very effective means for obtaining a high SFDR with lower power consumption and hardware cost thanks to its simplicity.

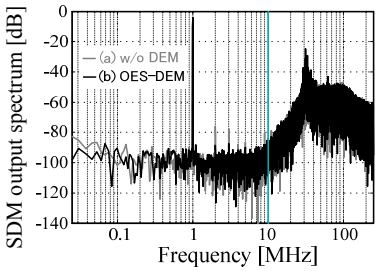

Fig. 8. Measured output spectrum of DSM with (a) w/o DEM, and (b) OES method

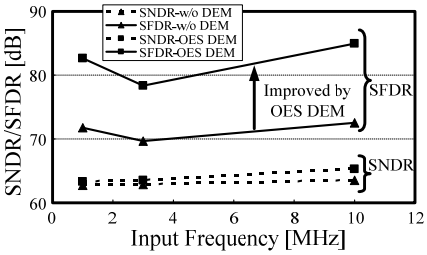

Fig. 9. Measured output spectrum of DSM with (a) w/o DEM, and (b) OES method

V. Conclusion

A proposed OES DEM has been presented in this paper. The measurement results shows that the OES substantially suppresses the both effects of the mismatch and glitch. Simplicity and effectiveness of the OED technique makes it very attractive and prefer for cost and power considerations, and is good enough for almost all the applications.

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