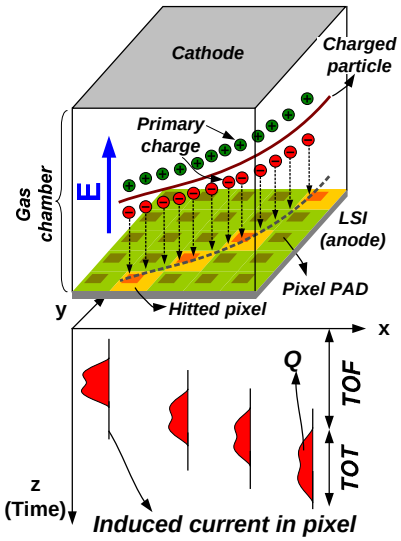
Background and Motivation

This research is supposed to implement the most precise CMOS readout LSI in the world for 3D charged particle tracking applications by using standard deep sub-micro CMOS process.

Functionality of pixel readout LSI

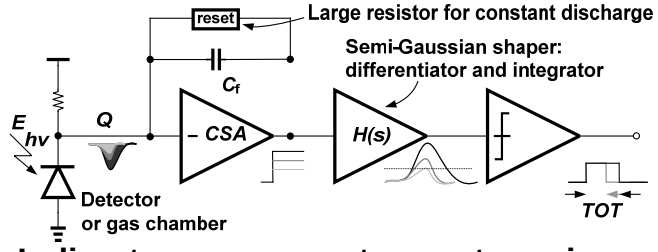


TOF : Time of Flight (drift time)

TOT : Time over Threshold (Density of electron in z direction)

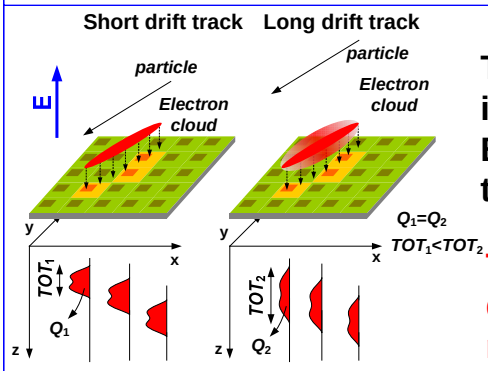
Q : total deposited charge

Conventional TOT method



- Indirect measurement → not precise
- large discharge time (> 500 ns ~ 1 μs)

→ Not suitable for fast imaging application

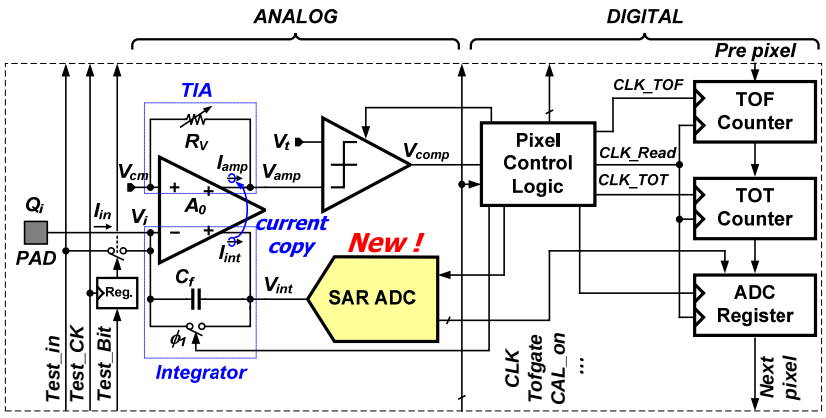


Total charge information is estimated from TOT But, TOT is affected by the flying angular

To improve the charge detecting precision, new methods are necessary

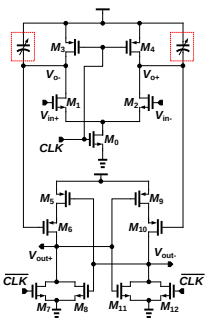
Pixel Schematic of Qpix v.1

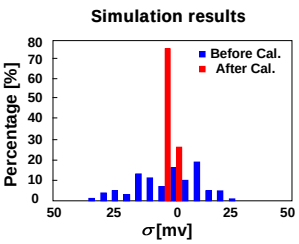
***QPIX*: *Q*uad information / *Q*uasi-3D / *Q* (Charge) information provided *PIX*el readout LSI**



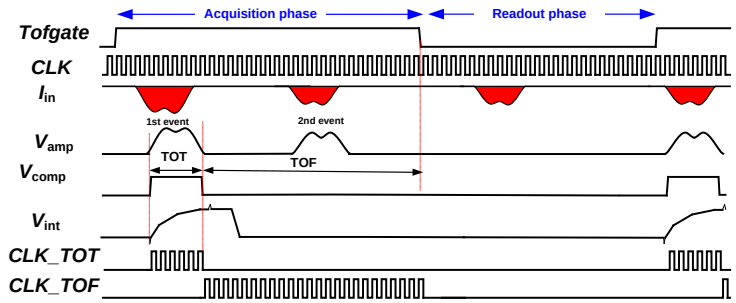
SAR (*Successive Approximation Register*) ADC provides direct and precise measurement of total charge Q

Dynamic comparator with capacitance calibration

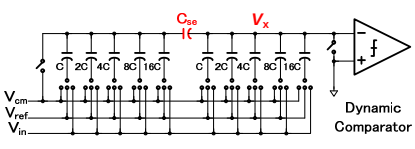


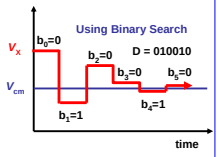


input offset voltage (σ): 13.5 mV → 1.5 mV improves the detecting sensitivity



SAR ADC

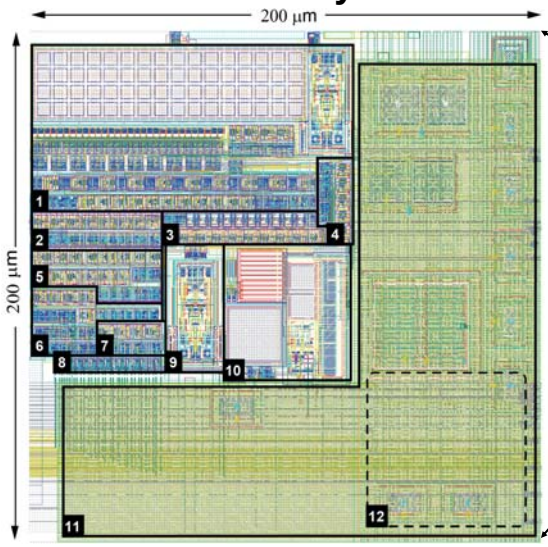




- 10 bit, 10 Msps
- Low power consumption: no DC current
- Small die size: compact structure

Chip Implementation

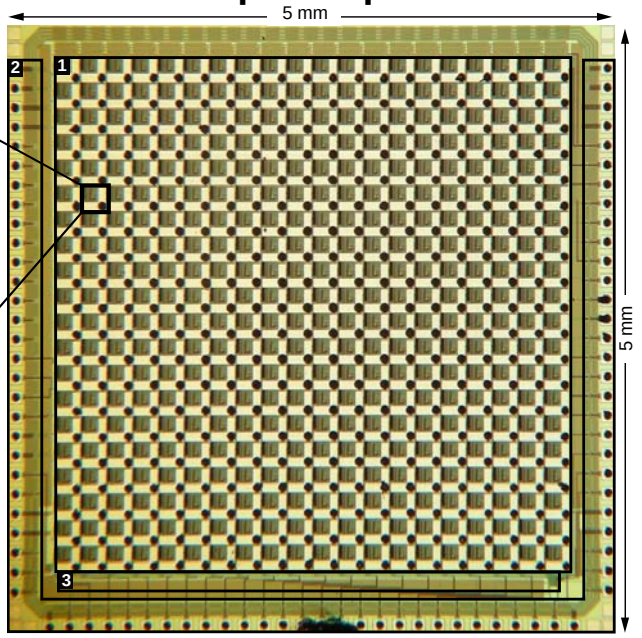
Pixel Layout



- 130 μm x 140 μm active circuitry
- large pixel pad
  - As an charge-collecting pad when used in gas chambers
  - As a bonding pad for flip-chip bump bonding with diverse sensors

(1) 10-bit SAR ADC; (2) TOT counter; (3) 10-bit register for ADC; (4) 5-bit calibration register for the amplifier; (5) TOF counter; (6) pixel control logic circuit; (7) 4-bit calibration register for comparator; (8) control signal buffers; (9) comparator; (10) the amplifier and the integrator; (11) pixel pad; (12) bonding point for flip-chip bump bonding.

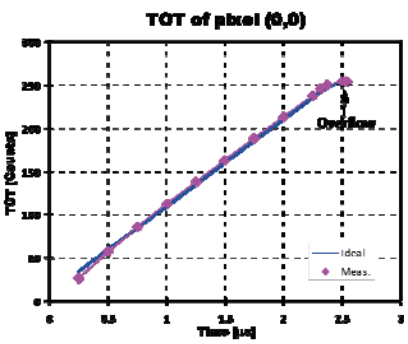
Chip Microphoto

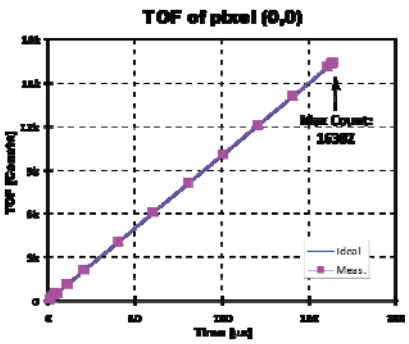


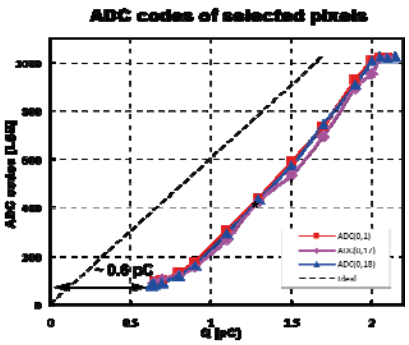
- 0.18 μm CMOS process, 400 pixels
- Compact high speed readout structure: 240 Mbps
- Suitable for large area applications
  - 16 mm² active detection area (64% of the total chip surface)

(1) 20 x 20 pixel matrix; (2) wire bonding pads and their ESD for power supplies and input/output signals; (3) periphery circuits including the chip control logic circuit, the bias circuit, and the 20-bit FSR.

Measurement Results

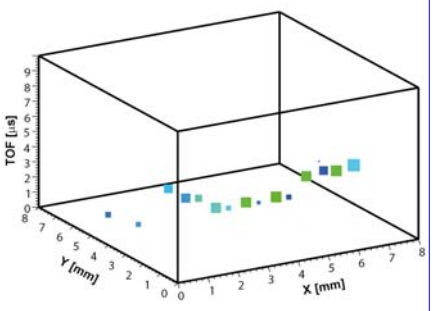






*Offset charge is caused by large paracitic capacitance in measurement system.

A sample 3D track by Qpix v.0



Demonstrates its ability in 3D tracking detector

	Qpix v.1	Qpix v.0	Timepix	Future work
Number of Pixels	20 x 20	2 x 8	256 x 256	20 x 20
Pixel dimensions	200 x 200 μm² (Pixel pad included)	140 x 200 μm² (No pixel pad)	50 x 50 μm²	200 x 200 μm² (Pixel pad included)
Dynamic range	10 fC ~ 1.5 pC	100 fC ~ 1.0 pC	0.1 fC ~ 12 fC	1 fC ~ 150 fC
Comp. threshold	35 fC	245 fC	0.1 fC	1 fC
Readout information	TOF: 14 bits, 10 ns	TOF: 14 bits,10 ns	14 bits, 10 ns (TOF or TOT or Photon counter)	TOF: 14 bits, 10 ns
	TOT: 8 bits, 10 ns	TOT: 8 bits, 10 ns		TOT: 8 bits, 10 ns
	ADC: 10 bits, 10MSps	ADC: 6 bits, 10MSps	None	ADC: 10 bits, 10MSps
Power/channel	187.5 μW	350 μW	6.5 μW + 7 μW	150 μW
Readout speed	240 Mbps	100 Mbps	100Mbps	240 Mbps
Readout mode	Serial/Parallel	Switched parallel	Serial/Parallel	Serial/Parallel Event driven