A 15.5 dB, Wide Signal Swing, Dynamic Amplifier Using a Common-Mode Voltage Detection Technique

James Lin, Masaya Miyahara and Akira Matsuzawa
Department of Physical Electronics
Tokyo Institute of Technology
2-12-1, O-okayama, Meguro-ku, Tokyo, 152-8552, Japan
james@ssc.pe.titech.ac.jp

***Abstract*—This paper presents a high-speed, low-power and wide signal swing differential dynamic amplifier using a common-mode voltage detection technique. The proposed dynamic amplifier achieves a 15.5 dB gain with less than 1 dB drop over a signal swing of 1.3 V_{pp} at an operating frequency of 1.5 GHz with a V_{DD} of 1.2 V in 90 nm CMOS. The power consumption of the proposed circuit can be reduced linearly with operating frequency lowering.**

I. INTRODUCTION

Amplifiers are one of the most crucial components in analog electronics [1], [2]. However, the key limitations with conventional amplifiers are the large power consumption compared with dynamic comparators and the narrow signal swing in low voltage operation. An effective way to minimize this power consumption is to remove the unnecessary static current. For many mixed-signal applications, amplification is only required during part of a clock cycle. In these cases, amplifiers operating dynamically provide the ideal solution in reducing the power dissipation.

Conventionally, dynamic amplifiers are often used as pre-amplifiers for dynamic comparators to reduce noise [3] and as receiver amplifiers in DRAM design [4]. They are rarely used independently as single-stage amplifiers due to the lack of techniques to provide a linear gain.

In this paper, a differential dynamic amplifier using a common-mode voltage detection technique is proposed. This architecture is suitable for a high-speed, low-power and wide signal swing dynamic amplifier. Furthermore, it is possible to realize ultra low-power and high-speed applications with the same circuit using this architecture.

II. CIRCUIT DESIGN

A. Common-mode Voltage Detection Technique

The schematic of the proposed architecture for a dynamic amplifier and its operation waveform are shown in Figures 1 and 2, respectively. The common-mode voltage detection circuit provides the logic required to terminate the load

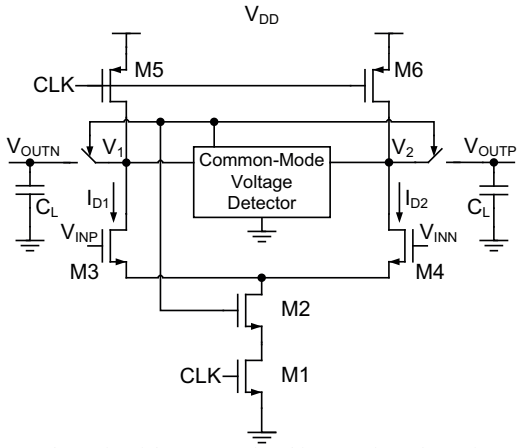

Figure 1: Schematic of the proposed architecture for a dynamic amplifier.

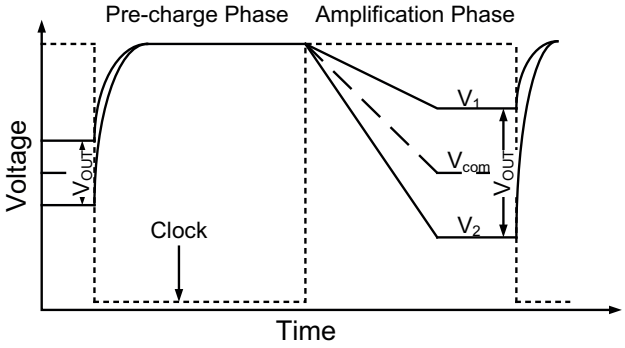

Figure 2: Operation waveform of the proposed dynamic amplifier.

capacitors from discharging thus allowing the dynamic amplifier to have a steady output voltage.

During the pre-charge phase when the clock is low, V_1 and V_2 are charged to the supply voltage, V_{DD}. When the clock turns high, the amplification phase begins and V_1 and V_2 start to discharge at rates depending on V_{INP} and V_{INN}, respectively.

B. Gain

To determine the gain of the proposed architecture, the voltages at V_{OUTP} and V_{OUTN} are

$$V_{\mathrm{OUTP}} \approx V_2 = V_{\mathrm{DD}} - \frac{I_{\mathrm{D0}} - \frac{g_{\mathrm{m}}}{2}\Delta V_{\mathrm{IN}}}{C_{\mathrm{L}} + C_{\mathrm{P}}} t \quad (1)$$

$$V_{\mathrm{OUTN}} \approx V_1 = V_{\mathrm{DD}} - \frac{I_{\mathrm{D0}} + \frac{g_{\mathrm{m}}}{2}\Delta V_{\mathrm{IN}}}{C_{\mathrm{L}} + C_{\mathrm{P}}} t$$

$$t = \frac{(V_{\mathrm{DD}} - V_{\mathrm{com}})(C_{\mathrm{L}} + C_{\mathrm{P}})}{I_{\mathrm{D0}}} \quad (2)$$

where V_{com} is the output common-mode voltage, C_{L} is the load capacitance, C_{P} is the parasitic capacitance, t is the time required to trigger the common-mode detector, g_{m} is the transconductance, and I_{D0} is the common-mode drain current. From equations (1) and (2), the differential gain, G_{diff}, can be represented as,

$$G_{\mathrm{diff}} = \frac{V_{\mathrm{OUTP}} - V_{\mathrm{OUTN}}}{\Delta V_{\mathrm{IN}}} \approx \frac{g_{\mathrm{m}}}{I_{\mathrm{D0}}}(V_{\mathrm{DD}} - V_{\mathrm{com}}) \quad (3)$$

If the MOS transistors act according to the square-law,

$$G_{\mathrm{diff}} = \frac{2(V_{\mathrm{DD}} - V_{\mathrm{com}})}{V_{\mathrm{eff}}} \quad (4)$$

and if the MOS transistors function in the velocity saturation region,

$$G_{\mathrm{diff}} = \frac{V_{\mathrm{DD}} - V_{\mathrm{com}}}{V_{\mathrm{eff}}} \quad (5)$$

where V_{eff} is the effective gate voltage of the transistor, which is the gate-source voltage minus the threshold voltage. Therefore, the differential gain of this dynamic circuit is determined by V_{DD}-V_{com} and V_{eff}. Since V_{eff} is determined by the biasing condition, the differential gain can be controlled by V_{DD}-V_{com}. This linear relationship between V_{DD}-V_{com} and the differential gain is shown in Figure 3 with various load capacitances.

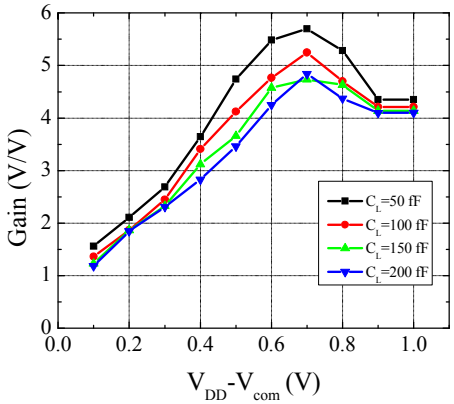

Figure 3: The proposed dynamic amplifier demonstrates a gain dependency on output common-mode voltage. Gain saturates when V_{DD}-V_{com} is around 0.7 V. Further increase in V_{DD}-V_{com} causes V_{OUTN} to clip resulting in the decreased gain. This is simulated at 500 MHz, 600 mV input common-mode voltage, 100 mV input differential-mode voltage with a 1.2 V supply.

C. *Signal Swing and Linearity*

The proposed circuit has a higher linearity owing to its wider output signal swing. A conventional self-biased differential amplifier generally has a narrower output signal swing due to its stacked architecture, as shown in Figure 4. In this case, a differential output voltage swing of 0.9 V_{pp} with less than 1 dB drop in gain is available, as illustrated in Figure 6.

Unlike conventional amplifiers, the proposed amplifier has a much wider output signal swing, as shown in Figure 5. The proposed design can attain an output voltage swing of 1.3 V_{pp} with less than 1 dB decrease in gain using a 1.2 V supply; thus, it has a better linearity performance.

The output voltage versus the gain for the conventional and the proposed designs are shown Figure 6. The proposed circuit offers a larger gain and a wider output signal swing.

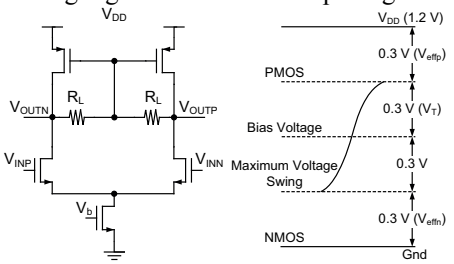

Figure 4: Conventional single-stage amplifier's available output swing.

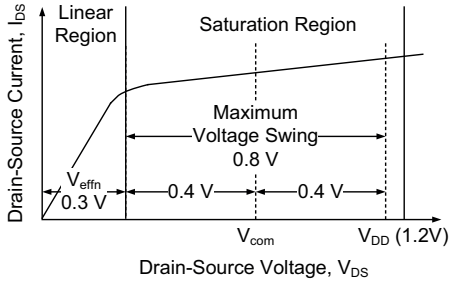

Figure 5: Proposed dynamic amplifier's available output swing.

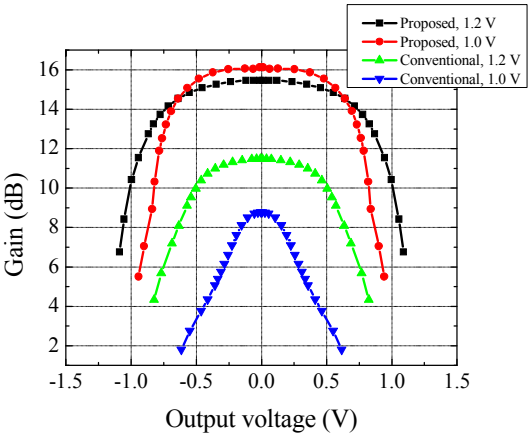

Figure 6: Simulation results show the proposed design offers better linearity performance, wider signal swing, and is less sensitive to supply voltage lowering than the conventional design. The simulation conditions are $V_{\mathrm{DD}}/2$ input common-mode voltage and 100 mV input differential-mode voltage with 100 fF load capacitance for the proposed design operating at 1.5 GHz.

D. Speed

Due to the CMOS technology scaling, transistors can operate at a very high frequency. This dynamic amplifier benefits from such technology scaling and operates in the GHz range. The delay time that determines the operating frequency of this circuit is described in equation (2). The key factor limiting the operating frequency of the proposed amplifier is the RC delay. Typically, to allow for high speed operation, a transistor with a larger size is more desirable. However, as the transistor size increases, the parasitic capacitance increases. The optimal operating point for this dynamic amplifier is when the parasitic capacitance is equal to the load capacitance. Further increase in transistor size has little effect on increasing the operating speed. Figure 7 shows the dynamic amplifier's performance with various load capacitances.

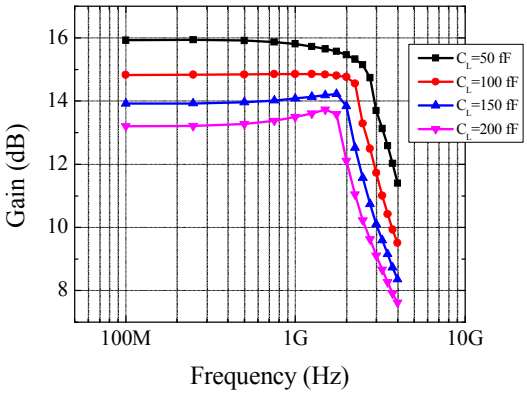

Figure 7: Operating frequency sweep with different load capacitances shows the effect of capacitance on the proposed design. The inputs are 600 mV for common-mode voltage and 100 mV for differential-mode voltage.

E. Power

The dynamic nature of this amplifier allows it to function using very little power. The power dissipation for a dynamic circuit is calculated by

$$P_{\mathrm{d}} = af(C_{\mathrm{L}} + C_{\mathrm{P}})V_{\mathrm{DD}}^2 \qquad (6)$$

where a is the activity factor and f is the operating frequency. In the case of this dynamic amplifier, a lies in the range around one as the common-mode voltage detector terminates the discharging of the two load capacitors in the region around half of V_{DD}. Consequently, operating at 1.5 GHz, the amount of power consumed by this dynamic amplifier is approximately half of a conventional single-stage amplifier.

Unlike conventional amplifiers, an additional merit in operating dynamically is the power-saving potential when the operating frequency is lowered. Due to its dynamic nature, the power consumption of this amplifier is directly proportional to the operating frequency, as illustrated in Figure 8. Therefore, for applications that may require low or variable frequency operation, the power dissipation is automatically reduced without any changes to the circuit. This allows for low-speed ultra low-power and high-speed applications to be realized using the same circuit.

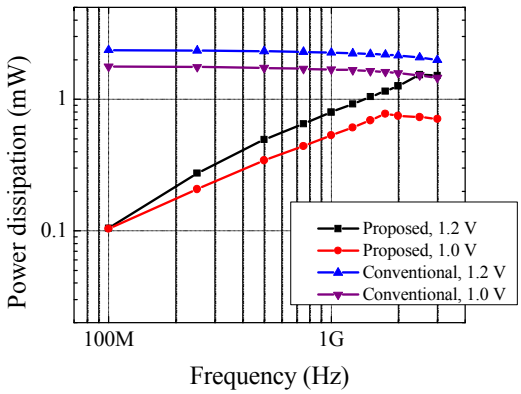

Figure 8: Power consumption comparison with the simulation conditions set as $V_{\mathrm{DD}}/2$ input common-mode voltage, 100 mV input differential-mode voltage and 100 fF load capacitance.

III. Circuit Implementation

A. Common-mode Voltage Detection Circuit

The proposed single-stage pseudo-differential dynamic amplifier with an inverter-based common-mode voltage detection circuit is shown in Figure 9.

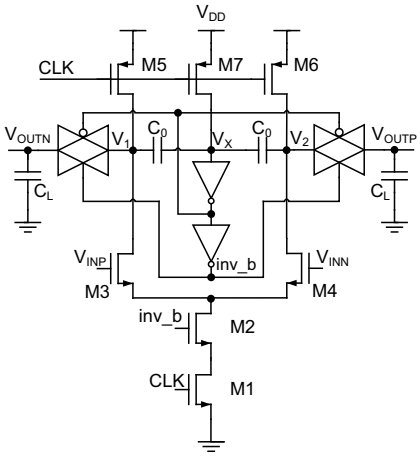

Figure 9: The proposed dynamic amplifier with an inverter-based common-mode voltage detector located in the centre.

The proposed circuit consists of a differential pair and a common-mode voltage detector. In the differential pair, transistors M3 and M4 are the input transistors while transistors M1, M2, and M5-7 all act as switches. The common-mode voltage detector uses V_{X} to provide the logic to determine when V_1 and V_2 should stop discharging. V_{X} is related to V_1 and V_2 by the following equation,

$$V_{\mathrm{X}} = \frac{1}{1+\dfrac{C_{\mathrm{PX}}}{2C_0}}\left(\frac{V_1+V_2}{2}\right)+\frac{C_{\mathrm{PX}}}{2C_0+C_{\mathrm{PX}}}V_{\mathrm{DD}} \qquad (7)$$

where C_0 is the capacitance used to detect the output common-mode voltage and C_{PX} is the parasitic capacitance at node V_{X}. Assuming that the parasitic capacitance at node V_{X} is small, V_{X} approximates to the common-mode voltage of V_1 and V_2. When V_{X} passes the region around half of V_{DD}, the logic from

the common-mode voltage detector is triggered switching off the transmission gates giving a steady differential output voltage between V_{OUTP} and V_{OUTN}.

B. Mismatch Correction and Gain Control Circuits

In addition to operating at a high speed while offering better linearity and consuming less power, the proposed design is suitable to use known techniques for the conventional amplifiers.

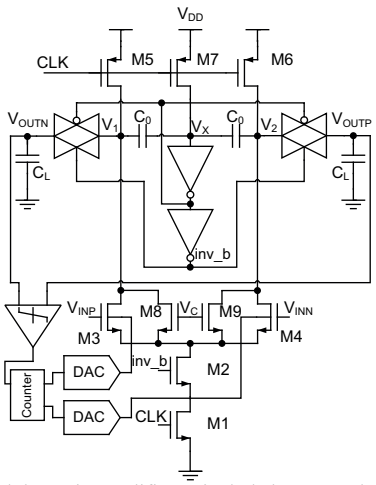

Figure 10: Modified dynamic amplifier to include known techniques in offset voltage calibration and gain control.

For example, with some slight modifications of Figure 9, a dynamic amplifier with offset voltage calibration and gain control can be realized, as shown in Figure 10. The modified calibration scheme, based on [5], [6] and [7] using a comparator from [8] with a digitally controlled back-gate bias generator, can reduce the input-referred offset voltage from 5.59 mV (σ) to 1.27 mV (σ), as illustrated in Figure 11. As indicated in Figure 12, with the gain control circuitry, the proposed amplifier has a monotonically decreasing range of 3.5 dB with M3 and M4's width/length sized to 8µm/0.1µm and M8 and M9 sized to 0.8µm/0.1µm.

IV. CONCLUSION

A high-speed and low-power dynamic amplifier using a common-mode voltage detection technique is proposed. Simulation results show the dynamic amplifier operating at 1.5 GHz with an open-loop gain above 15.5 dB over an output signal swing of 1.3 V_{pp} while consuming 1.05 mW from a 1.2 V supply in 90 nm CMOS. As this dynamic amplifier provides steady differential output signals, it can be used as a single-stage amplifier in mixed-signal circuits, such as pipelined analog-to-digital converters and sampling mixers.

TABLE I: PERFORMANCE SUMMARY

Frequency [GHz]	Gain [dB]	Supply [V]	Power Dissipation [mW]	Load Capacitance [fF]	Process
1.5	15.5	1.2	1.05	100	90 nm CMOS

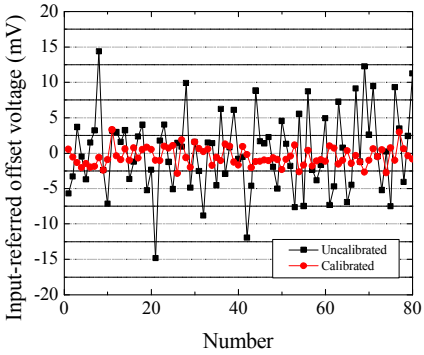

Figure 11: Monte Carlo simulation results show the proposed design can benefit from existing techniques to decrease its offset voltage.

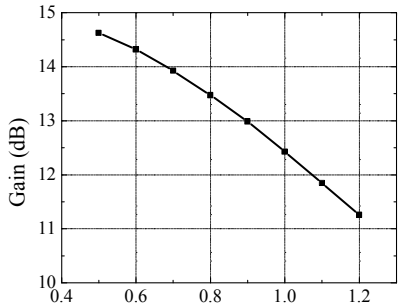

Figure 12: The gain control simulation show the proposed design can benefit from existing techniques to allow for variable gain.

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